XIAMEN OCULAR

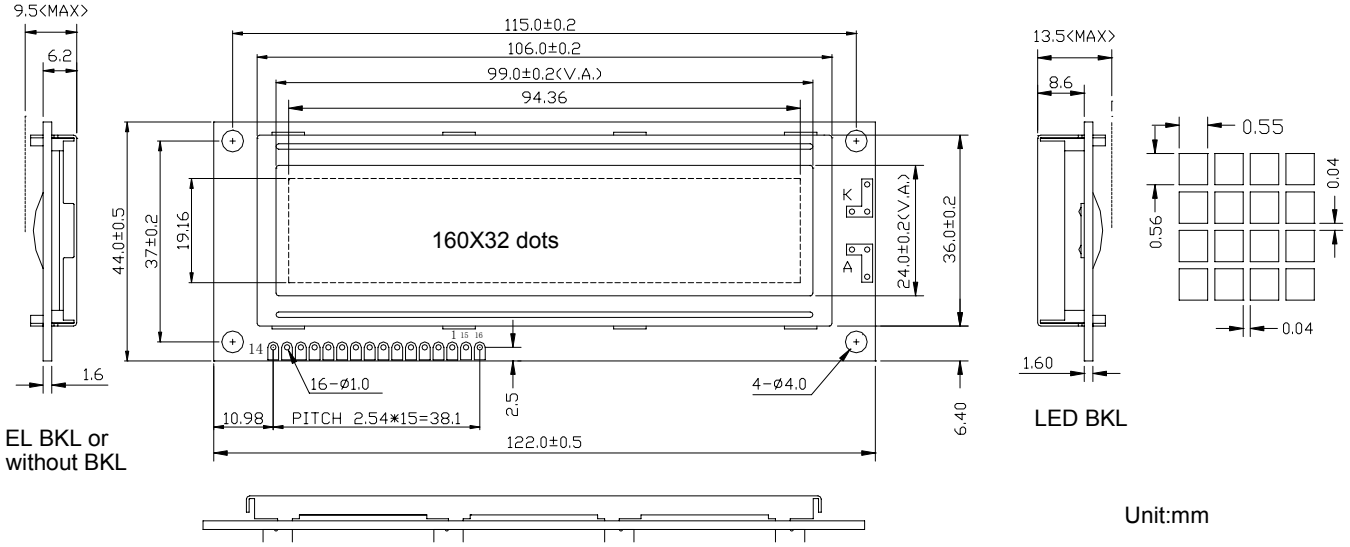
GDM16032B-FL-YBW

SPECIFICATIONS OF LCD MODULE

Features

1、 160x32 dots with 8192 Chinese character fonts (16x16)
2、 128 alpha-numerical fonts (16x8)
3、 64x256 bit graphic display RAM
4、 Strong display control functions: Vertical scroll, horizontal bit scroll, line reverse etc
5、 +2.7v~+5.5v power supply
6、 STN Yellow-Green mode, transflective
7、 Viewing angle: 6 O'clock
8、 1/32 duty
9、 Built-in voltage booster
10、4 bit, 8 bit, serial interface
11、LED backlight (yellow-green)optional

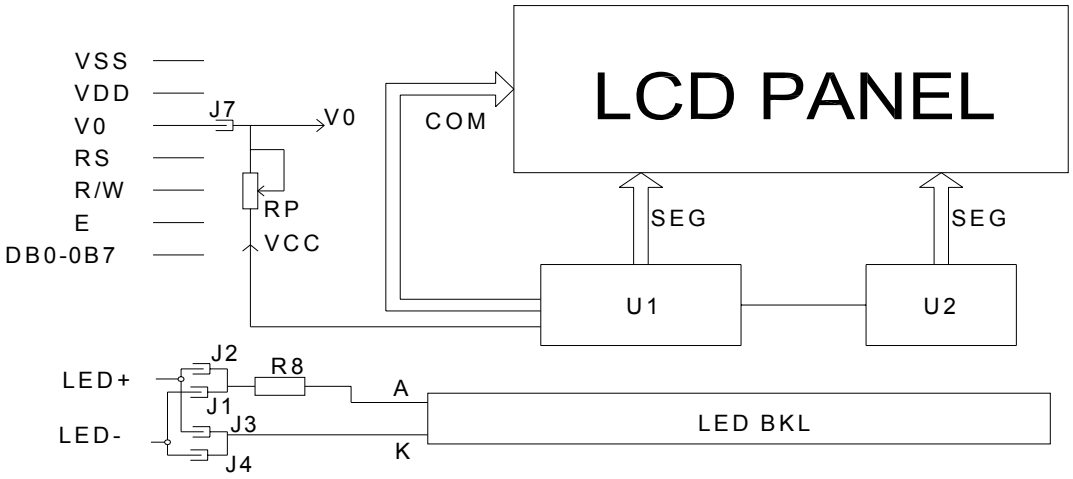
Outline dimension



Absolute maximum ratings

Item	Symbol	Standard			Unit
Power supply voltage	V_{DD}-V_{SS}	-0.3	-	6.0	V
Input voltage	VIN	-0.3	-	VDD+0.3	
Operating temperature range	Top	-20	-	+70	℃
Storage temperature range	Tst	-25	-	+80	

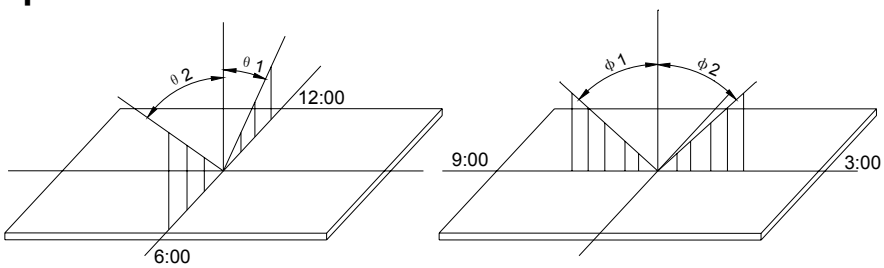
Block diagram



Interface pin description

Pin no.	Symbol	External connection	Function
1	V_{SS}	Power supply	Signal ground for LCM (GND)
2	V_{DD}		Power supply for logic for LCM
3	V_0		Contrast adjust
4	RS(CS)	MPU	Register select signal(chip select for serial mode)
5	R/W(SID)	MPU	Read/write select signal(serial data input for serial mode)
6	E(SCLK)	MPU	Operation (data read/write) enable signal(serial clock for serial mode)
7~10	DB0~DB3	MPU	Four low order bi-directional three-state data bus lines. Used for data transfer between the MPU and the LCM. These four are not used during 4-bit operation.
11~14	DB4~DB7	MPU	Four high order bi-directional three-state data bus lines. Used for data transfer between the MPU
15	LED+	LED BKL power supply	Power supply for Backlight (Anode +5.0V)
16	LED-		Power supply for BKL (GND)

Optical characteristics

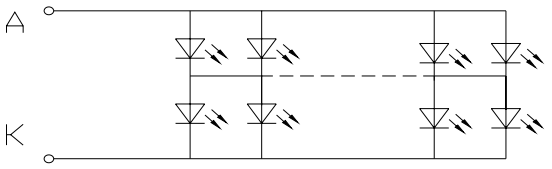


STN type display module (Ta=25℃, VDD=5.0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Viewing angle	θ 1	$C_r \geqslant 3$		30		deg
	θ 2			40		
	Φ 1			35		
	Φ 2			35		
Contrast ratio	C_r		-	10	-	-
Response time (rise)	T_r	-	-	200	250	ms
Response time (fall)	T_r	-	-	300	350	

Electrical characteristics

LED Backlight circuit (color: Yellow-Green)



2*24=48

LED ratings

Item	Symbol	Min	Typ.	Max	Unit
Forward Voltage	Vf	3.8	4.0	4.2	v
Forward current	If		240	300	mA
Power	P			1.3	W
Peak wave length	λp	570	-	575	nm
Luminance	Lv	150		-	Cd/m2
Operating temperature range	Vop	-20	-	+70	℃
Storage temperature range	Vst	-25	-	+80	

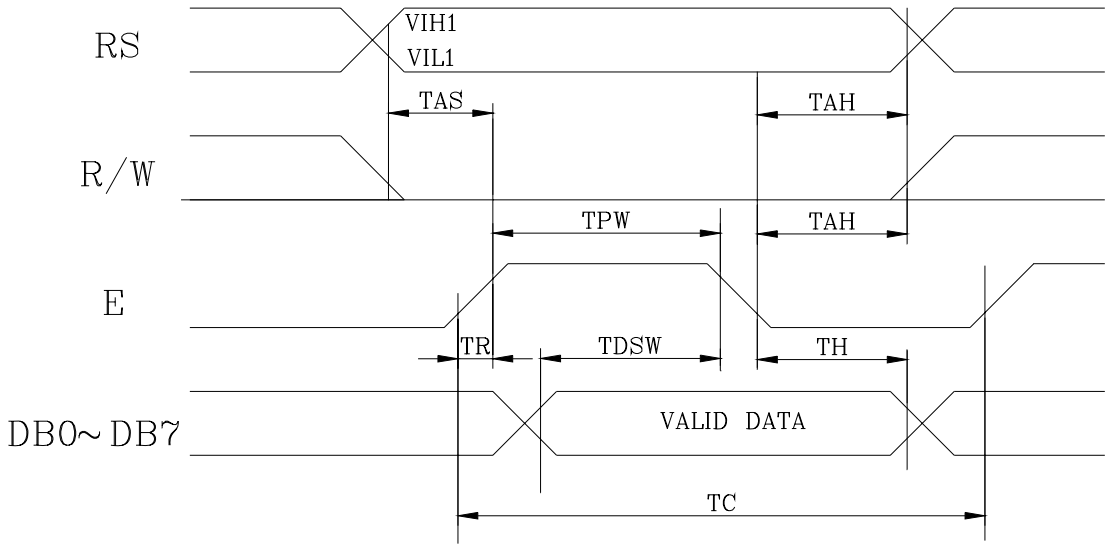
DC characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage for LCD	V_{LCD}		-	6.5	-	V
Input voltage	V_{DD}	V=3.3V	2.7	3.3	5.3	
		V=5V	4.8	5.0	5.3	
Supply current	I_{DD}	Ta=25℃, V_{DD}=5.0V	-	2	4	mA
Input leakage current	I_{LKG}		-	-	1.0	uA
“H” level input voltage	V_{IH}		2.2	-	V_{DD}	V
“L” level input voltage	V_{IL}	Twice initial value or less	0	-	0.6	
“H” level output voltage	V_{OH}	LOH=-0.25mA	2.4	-	-	
“L” level output voltage	V_{OL}	LOH=1.6mA	-	-	0.4	
Backlight supply voltage	V_F		-	-	5.0	
Backlight supply current	I_{led}	V_{LED}=5.0V R=6.8Ω	-	150		mA

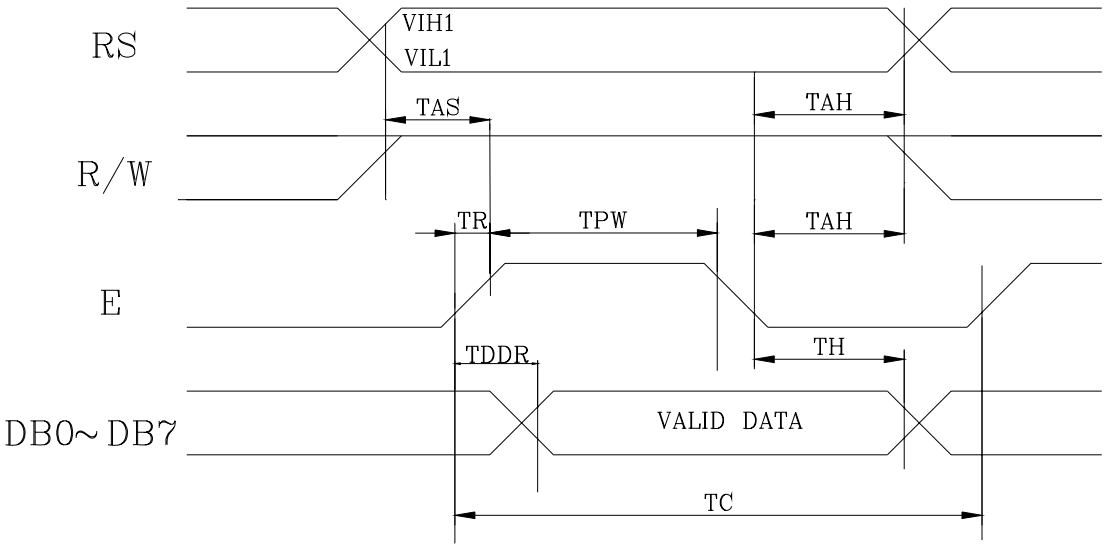
AC Characteristics (T_A = -30℃ ~ 85℃, V_{DD} = 4.5V) Parallel Mode Interface

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
Internal Clock Operation						
fOSC	OSC Frequency	R = 33KW	480	540	600	KHz
External Clock Operation						
fEX	External Frequency	-	480	540	600	KHz
	Duty Cycle	-	45	50	55	%
TR,TF	Rise/Fall Time	-	-	-	0.2	μσ
Write Mode (Writing data from MPU to ST7920)						
TC	Enable Cycle Time	Pin E	1200	-	-	ns
TPW	Enable Pulse Width	Pin E	140	-	-	ns
TR,TF	Enable Rise/Fall Time	Pin E	-	-	25	ns
TAS	Address Setup Time	Pins: RS,RW,E	10	-	-	ns
TAH	Address Hold Time	Pins: RS,RW,E	20	-	-	ns
TDSW	Data Setup Time	Pins: DB0 - DB7	40	-	-	ns
TH	Data Hold Time	Pins: DB0 - DB7	20	-	-	ns
Read Mode (Reading Data from ST7920 to MPU)						
TC	Enable Cycle Time	Pin E	1200	-	-	ns
TPW	Enable Pulse Width	Pin E	140	-	-	ns
TR,TF	Enable Rise/Fall Time	Pin E	-	-	25	ns
TAS	Address Setup Time	Pins: RS,RW,E	10	-	-	ns
TAH	Address Hold Time	Pins: RS,RW,E	20	-	-	ns
TDDR	Data Delay Time	Pins: DB0 - DB7	-	-	100	ns
TH	Data Hold Time	Pins: DB0 - DB7	20	-	-	ns

Write Timing



Read timing



Function Description

- **System interface**

The GDM16032A supports 3 kinds of bus interface to communicate with MPU: 8-bit parallel, 4-bit parallel and clock synchronized serial interface. Parallel interface is selected by PSB=”P” and serial interface is by PSB=”S”. 8-bit / 4-bit interface is selected by function set instruction DL bit.

- **Busy Flag (BF)**

The LCD module needs a process time for any received instruction. Before finishing the received instruction, any further instruction is not accepted. The process time of each instruction is not equal and the internal process is finished or not can be determined by the BF. Internal operation is in progress while BF=”1”, that means module is in busy state. No further instructions will be accepted until BF=”0”. MPU must check BF to determine whether the internal operation is finished or not before issuing instruction.

- **Character Generation ROM (CGROM) and Half-width Character Generation ROM (HCGROM)**

The LCD module is built in a Character Generation ROM (CGROM) to provide 8192 16x16 character fonts and a Half-width Character Generation ROM to provide 128 8x16 alphanumeric characters. It is easy to support multi-language applications such as Chinese and English. Two consecutive bytes are used to specify one 16x16 character or two 8x16 half-width characters. Character codes are written into DDRAM and the corresponding fonts are mapped from CGROM or HCGROM to the display drivers.

- **Character Generation RAM (CGRAM)**

The LCD module is built in a Character Generation RAM (CGRAM) to support user-defined fonts. Four sets of 16x16 bit-mapped RAM spaces are available. These user-defined fonts are displayed the same ways as CGROM fonts by writing the related character code into the DDRAM.

- **Display Data RAM (DDRAM)**

There are 64x256 bytes RAM spaces for the Display Data RAM. It can store display data such as 10 characters (16x16) by 2 lines or 32 characters (8x16) by 4 lines. However, only 2 character-lines (maximum 32 common outputs) can be displayed at one time. Character codes stored in DDRAM will refer to the fonts specified by CGROM, HCGROM and CGRAM. The LCD module can display half-width HCGROM fonts, user-defined CGRAM fonts and full 16x16 CGROM fonts. The character codes in 0000H~0006H will use user-defined fonts in CGRAM. The character codes in 02H~7FH will use half-width alpha numeric fonts. The character code larger than A1H will be treated as 16x16 fonts and will be combined with the next byte automatically. The 16x16 BIG5 fonts are stored in A140H~D75FH while the 16x16 GB fonts are stored in A1A0H~F7FFH. In short:

1. To display HCGROM fonts:

Write 2 bytes of data into DDRAM to display two 8x16 fonts. Each byte represents 1 character. The data is among 02H~7FH.

2. To display CGRAM fonts:

Write 2 bytes of data into DDRAM to display one 16x16 font. Only 0000H, 0002H, 0004H and 0006H are acceptable.

3. To display CGROM fonts:

Write 2 bytes of data into DDRAM to display one 16x16 font. A140H~D75FH are BIG5 code, A1A0H~F7FFH are GB code.

The higher byte (D15~D8) is written first and the lower byte (D7~D0) is the next.

Please refer to Table 1 for the relationship between DDRAM and the address/data of CGRAM.

CGRAM fonts and CGROM fonts can only be displayed in the start position of each address. (Refer to Table 4)

80		81		82		83		84		85		86		87		88		89		8A		8B		8C		8D		8E		8F	
H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L
S	i	t	r	o	n	i	x		S	T	7	9	2	0																	
矽		創		電		子		.	.	中		文		編		碼			(	正		確		)							
矽		創		電		子		.	.	.	中		文		編		碼														

Table 4

Incorrect start position

■ **Graphic RAM (GDRAM)**

Graphic Display RAM has 64x256 bits bit-mapped memory space. GDRAM address is set by writing 2 consecutive bytes of vertical address and horizontal address. Two-byte data (16 bits) configures one GDRAM horizontal address. The Address Counter (AC) will be increased by one automatically after receiving the 16-bit data for the next operation. After the horizontal address reaching 0FH, the horizontal address will be set to 00H and the vertical address will not change. The procedure is summarized below:

1. Set vertical address (Y) for GDRAM
2. Set horizontal address (X) for GDRAM
3. Write D15~D8 to GDRAM (first byte)
4. Write D7~D0 to GDRAM (second byte)

Please refer to Table 3 for Graphic Display RAM mapping.

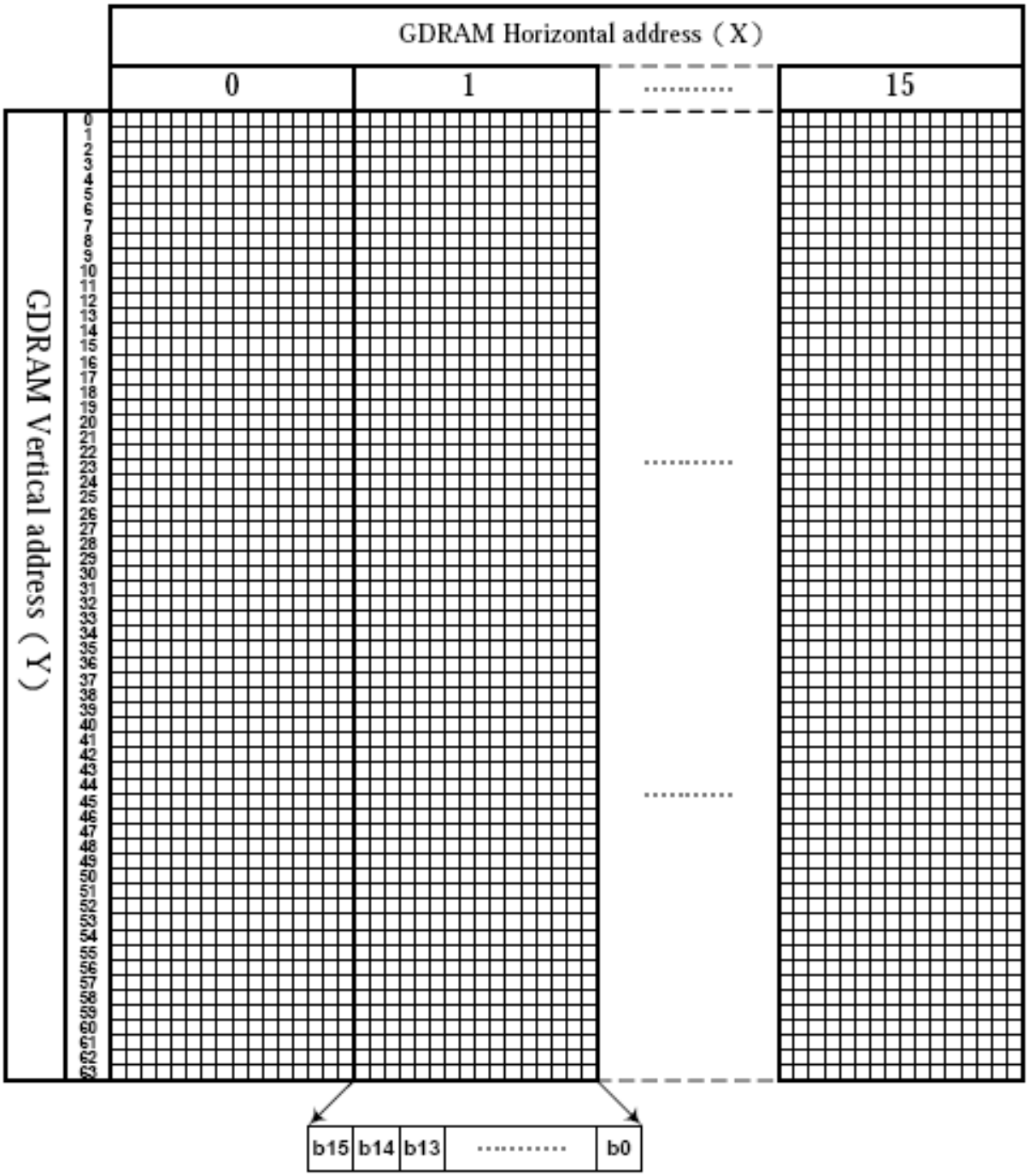


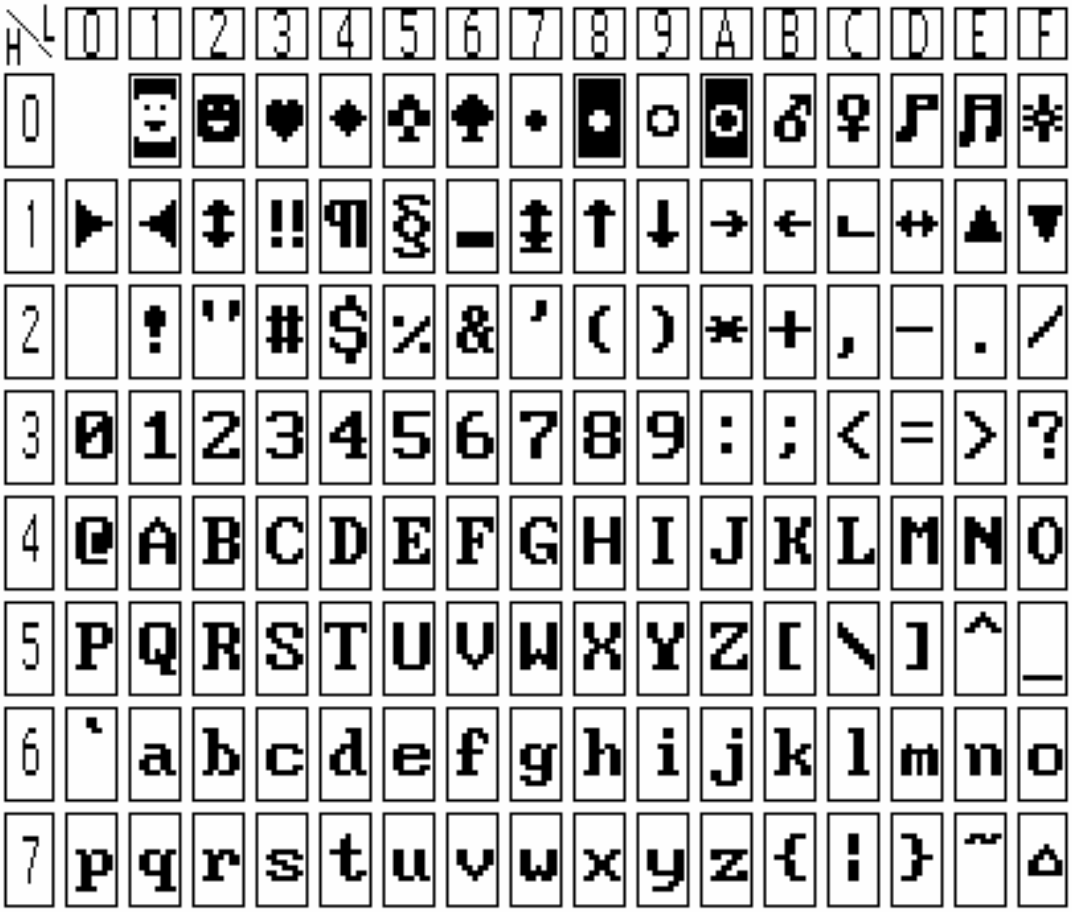
Table 3 GDRAM display coordinates and corresponding address

DDRAM data (char. code)					CGRAM Addr.					CGRAM data (higher byte)								CGRAM data (lower byte)							
B15~ B4	B3	B2	B1	B0	B5	B4	B3	B2	B1	B0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	X	00	X	00	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0	0	0
					0	0	0	1	1	1	1	1	1	1	1	0	0	0	1	0	0	0	0	0	0	0
					0	0	1	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0	0	0
					0	0	1	1	0	0	0	1	0	0	0	0	0	0	1	1	1	1	1	1	0	0
					0	1	0	0	0	0	1	0	0	1	0	0	1	0	0	0	0	0	1	0	0	0
					0	1	0	1	0	0	1	1	1	1	0	0	1	0	0	0	0	0	1	0	0	0
					0	1	1	0	0	1	1	0	0	1	0	1	0	1	0	0	0	1	0	0	0	0
					0	1	1	1	1	0	1	0	0	1	1	0	0	1	0	0	0	1	0	0	0	0
					1	0	0	0	0	0	1	0	0	1	0	0	0	1	0	1	0	0	0	0	0	0
					1	0	0	1	0	0	1	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0
					1	0	1	0	0	0	1	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0
					1	0	1	1	0	0	1	1	1	1	0	0	0	0	0	1	0	0	0	0	0	0
					1	1	0	0	0	0	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0
					1	1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
					1	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
					1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	X	01	X	01	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	1	0
					0	0	0	1	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	1	0	0
					0	0	1	0	0	0	1	0	0	0	0	1	0	0	1	1	0	1	0	1	0	0
					0	0	1	1	0	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0	0	0
					0	1	0	0	1	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0	0	0
					0	1	0	1	0	1	1	1	1	1	1	1	0	0	1	0	0	1	0	0	0	0
					0	1	1	0	0	1	0	0	0	0	0	1	0	0	1	0	0	1	0	0	0	0
					0	1	1	1	0	1	1	1	1	1	1	1	0	0	1	0	0	1	0	0	0	0
					1	0	0	0	0	1	0	0	0	0	0	1	0	0	1	0	0	1	0	0	0	0
					1	0	0	1	0	1	1	1	1	1	1	1	0	0	1	0	0	1	0	0	0	0
					1	0	1	0	0	1	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0
					1	0	1	1	0	1	1	1	1	1	1	1	1	0		0	0	1	0	0	0	0
					1	1	0	0	1	0	1	0	0	0	0	0	1	0	1	0	0	1	0	0	0	0
					1	1	0	1	1	0	1	1	1	1	1	1	1	0	0	1	1	1	0	0	0	0
					1	1	1	0	1	0	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0
					1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table1 DDRAM data (character code) vs. CGRAM data/address map

Notes:

1. DDRAM data (character code) bit1 and bit2 are identical with CGRAM address bit4 and bit5.
2. CGRAM address bit0 to bit3 specify total 16 rows. Row-16 is for cursor display. The data in Row-16 will be logically OR to the cursor.
3. CGRAM data for each address is 16 bits.
4. To select the CGRAM font, the bit4 through bit15 of DDRAM data must be “0” while bit0 and bit3 are “don’t care”.



16x8 half-width characters

Display command

Instruction Set 1: (RE=0: Basic Instruction)

Inst.	Code										Description	Exec time (540KHZ)
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Display Clear	0	0	0	0	0	0	0	0	0	1	Fill DDRAM with "20H" and set DDRAM address counter (AC) to "00H".	1.6 ms
Return Home	0	0	0	0	0	0	0	0	1	X	Set DDRAM address counter (AC) to "00H", and put cursor to origin ；the content of DDRAM are not changed	72 us
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Set cursor position and display shift when doing write or read operation	72 us
Display Control	0	0	0	0	0	0	1	D	C	B	D=1: Display ON C=1: Cursor ON B=1: Character Blink ON	72 us
Cursor Display Control	0	0	0	0	0	1	S/C	R/L	X	X	Cursor position and display shift control; the content of DDRAM are not changed	72 us
Function Set	0	0	0	0	1	DL	X	0 RE	X	X	DL=1 8-bit interface DL=0 4-bit interface **RE=1: extended instruction** **RE=0: basic instruction**	72 us
Set CGRAM Address.	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address to address counter (AC) **Make sure that in extended instruction SR=0 (scroll or RAM address select)**	72 us
Set DDRAM Address.	0	0	1	0 AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address to address counter (AC) AC6 is fixed to 0	72 us
Read Busy Flag (BF) & AC.	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Read busy flag (BF) for completion of internal operation, also Read out the value of address counter (AC)	0 us
Write RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data to internal RAM (DDRAM/CGRAM/GDRAM)	72 us
Read RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM/GDRAM)	72 us

Instruction set 2: (RE=1: extended instruction)

Inst.	Code										Description	Exec time (540KHZ)
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Standby	0	0	0	0	0	0	0	0	0	1	Enter standby mode, any other instruction can terminate. COM1…32 are halted.	72 us
Scroll or RAM Address. Select	0	0	0	0	0	0	0	0	1	SR	SR=1: enable vertical scroll position SR=0: enable CGRAM address **(basic instruction)**	72 us
Reverse (by line)	0	0	0	0	0	0	0	1	R1	R0	Select 1 out of 4 line (in DDRAM) and decide whether to reverse the display by toggling this instruction **R1,R0 initial value is 0,0**	72 us
Extended Function Set	0	0	0	0	1	DL	X	1 RE	G	0	DL=1 :8-bit interface DL=0 :4-bit interface **RE=1: extended instruction set** **RE=0: basic instruction set** G=1 :graphic display ON G=0 :graphic display OFF	72 us
Set Scroll Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	SR=1: AC5~AC0 the address of vertical scroll	72 us
Set Graphic Display RAM Address	0	0	1	0 0	0 AC5	0 AC4	AC3 AC3	AC2 AC2	AC1 AC1	AC0 AC0	Set GDRAM address to address counter (AC) Set the vertical address first and followed the horizontal address by consecutive writings Vertical address range: AC5…AC0 Horizontal address range: AC3…AC0	72 us

Note:

1. Make sure that ST7920 is not in busy state by reading the busy flag before sending instruction or data. If using delay loop instead, please make sure the delay time is enough. Please refer to the instruction execution time.
2. “RE” is the selection bit of basic and extended instruction set. After setting the RE bit, the value will be kept. So that the software doesn’t have to set RE every time when using the same instruction set.

Initial Setting (Register flag) (RE=0: basic instruction)

Inst.	Code										Description
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Cursor move to right ,DDRAM address counter (AC) plus 1
									1	0	
Display Control	0	0	0	0	0	0	1	D	C	B	Display, cursor and blink are ALL OFF
								0	0	0	
CURSOR DISPLAY SHIFT	0	0	0	0	0	1	S/C	R/L	X	X	No cursor or display shift operation
							X	X			
FUNCTION SET	0	0	0	0	1	DL	X	0 RE	X	X	8-bit MPU interface , basic instruction set
						1		0			

Initial Setting (Register flag) (RE=1: extended instruction set)

Inst.	Code										Description
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
SCROLL OR RAM ADDR. SELECT	0	0	0	0	0	0	0	0	1	SR	Allow IRAMaddress or set CGRAM address
										0	
REVERSE	0	0	0	0	0	0	0	1	R1	R0	Begin with normal and toggle to reverse
									0	0	
EXTENDED FUNCTION SET	0	0	0	0	1	DL	X	1 RE	G	0	Graphic display OFF
									0		

Description of basic instruction set

- Display Clear

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

This instruction will change the following items:
1. Fill DDRAM with "20H"(space code).
2. Set DDRAM address counter (AC) to"00H".
3. Set Entry Mode I/D bit to be "1". Cursor moves right and AC adds 1 after write or read operation.

- Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	-

Set address counter (AC) to "00H". Cursor moves to origin. Then content of DDRAM is not changed.

- **Entry Mode Set**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	S

Set the cursor movement and display shift direction when doing write or read operation.
I/D: Address Counter Control: (Increase/Decrease)
When I/D = "1", cursor moves right, address counter (AC) is increased by 1.
When I/D = "0", cursor moves left, address counter (AC) is decreased by 1.
S: Display Shift Control: (Shift Left/Right)

S	I/D	DESCRIPTION
H	H	Entire display shift left by 1
H	L	Entire display shift right by 1

- **Display Control**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Controls display, cursor and blink ON/OFF.
D: Display ON/OFF control bit
When D = "1", display ON
When D = "0", display OFF, the content of DDRAM is not changed
C: Cursor ON/OFF control bit
When C = "1", cursor ON.
When C = "0", cursor OFF.
B: Character Blink ON/OFF control bit
When B = "1", cursor position blink ON. Then display data (character) in cursor position will blink.
When B = "0", cursor position blink OFF

- Cursor/Display Shift Control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	-	-

This instruction configures the cursor moving direction or the display shifting direction. The content of DDRAM is not changed.

S/C	R/L	Description	AC Value
L	L	Cursor moves left by 1 position	AC=AC-1
L	H	Cursor moves right by 1 position	AC=AC+1
H	L	Display shift left by 1, cursor also follows to shift.	AC=AC
H	H	Display shift right by 1, cursor also follows to shift.	AC=AC

- **Function Set**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	-	RE	-	-

DL: 4/8-bit interface control bit
When DL = "1", 8-bit MPU bus interface
When DL = "0", 4-bit MPU bus interface
RE: extended instruction set control bit
When RE = "1", extended instruction set
When RE = "0", basic instruction set
In same instruction cannot alter DL and RE at once. Make sure that change DL first then RE.

- **Set CGRAM Address**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address into address counter (AC)
AC range is 00H…3FH
Make sure that in extended instruction SR=0 (scroll address or RAM address select)

- **Set DDRAM Address**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address into address counter (AC).
First line AC range is 80H…8FH
Second line AC range is 90H…9FH
Third line AC range is A0H…AFH
Fourth line AC range is B0H…BFH
Please note that only 2 lines can be display

- **Read Busy Flag (BF) and Address**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Read busy flag (BF) can check whether the internal operation is finished or not. At the same time, the value of address counter (AC) is also read. When BF = “1”, further instruction(s) will not be accepted until BF = “0”.

- **Write Data to RAM**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write data to the internal RAM and increase/decrease the (AC) by 1
Each RAM address (CGRAM, DDRAM and GDRAM…) must write 2 consecutive bytes for 16-bit data. After receiving the second byte, the address counter will increase or decrease by 1 according to the entry mode set control bit.

- **Read RAM Data**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read data from the internal RAM and increase/decrease the (AC) by 1
After the operation mode changed to Read (CGRAM, DDRAM and GDRAM…), a “Dummy Read” is required.
There is no need to add a “Dummy Read” for the following bytes unless a new address set instruction is issued.

Description of extended instruction set

- **Standby**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

This Instruction will set ST7920 entering the standby mode. Any other instruction follows this instruction will terminate the standby mode.
The content of DDRAM remains the same.

- **Vertical Scroll or RAM Address Select**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	SR

When SR = "1", the Vertical Scroll mode is enabled.
When SR = "0", “Set CGRAM Address” instruction **(basic instruction)** is enabled.

- **Reverse**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	R1	R0

Select 1 out of 4 lines to reverse the display and to toggle the reverse condition by repeating this instruction. R1, R0 initial vale is 00. The first time issuing this instruction, the display will be reversed while the second time will return the display become normal.

R1	R0	Description
L	L	First line normal or reverse
L	H	Second line normal or reverse
H	L	Third line normal or reverse
H	H	Fourth line normal or reverse

- **Extended Function Set**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	-	RE	G	-

DL: 4/8-bit interface control bit
When DL = "1", 8-bit MPU interface.
When DL = "0", 4-bit MPU interface.
RE: extended instruction set control bit
When RE = "1", extended instruction set
When RE = "0", basic instruction set
G: Graphic display control bit
When G = "1", Graphic Display ON
When G = "0", Graphic Display OFF
In same instruction cannot alter DL, RE and G at once. Make sure that change DL or G first and then RE.

- **Set Scroll Address**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

SR=1: AC5~AC0 is vertical scroll displacement address

- **Set Graphic RAM Address**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	AC5	AC4	AC3	AC2	AC1	AC0

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	AC3	AC2	AC1	AC0

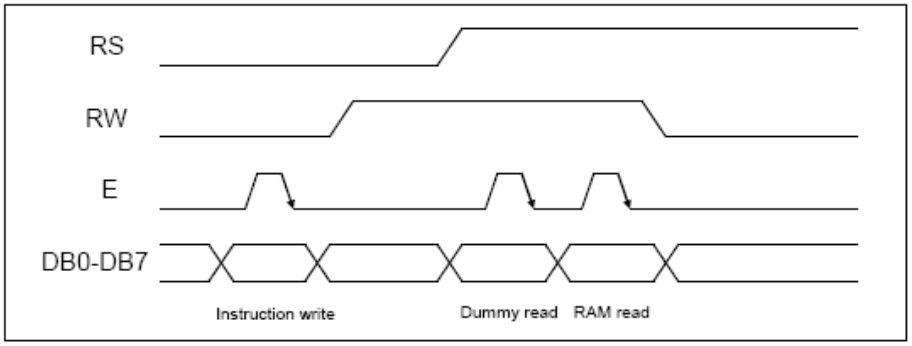
Set GDRAM address into address counter (AC). This is a 2-byte instruction.
The first instruction sets the vertical address while the second one sets the horizontal address (write 2 consecutive bytes to complete the vertical and horizontal address setting).
Vertical address range is AC5...AC0
Horizontal address range is AC3…AC0
The address counter (AC) of graphic RAM (GRAM) will be increased automatically after the vertical and horizontal addresses are set. After horizontal address is increased up to 0FH, it will automatically return to 00H. However, the vertical address will not increase as the result of the same action.

■ Parallel interface:

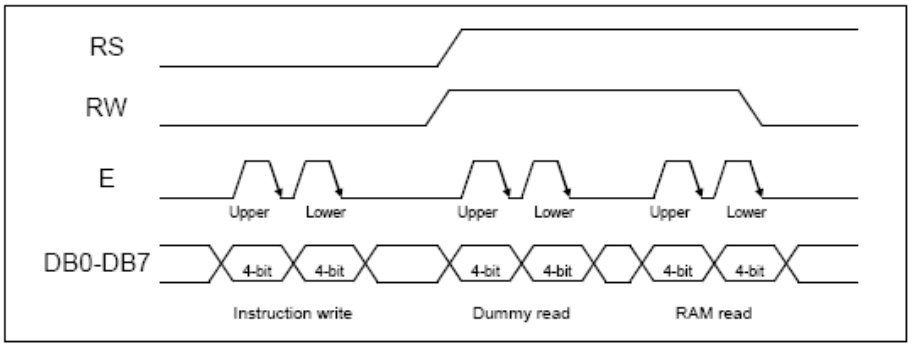
The LCD module is in parallel mode by pulling up PSB pin. The LCD module can select 8-bit or 4-bit bus interface by

setting the DL control bit in “Function Set” instruction. MPU can control RS, RW, E and DB0…DB7 pins to complete the data transmission.

In 4-bit transfer mode, every 8-bit data or instruction is separated into 2 parts. The higher 4 bits (bit-7~bit-4) data will be transferred first through data pins (DB7~DB4). The lower 4 bits (bit-3~bit-0) data will be transferred second through data pins (DB7~DB4). The (DB3~DB0) data pins are not used during 4-bit transfer mode.



Timing Diagram of 8-bit Parallel Bus Mode Data Transfer



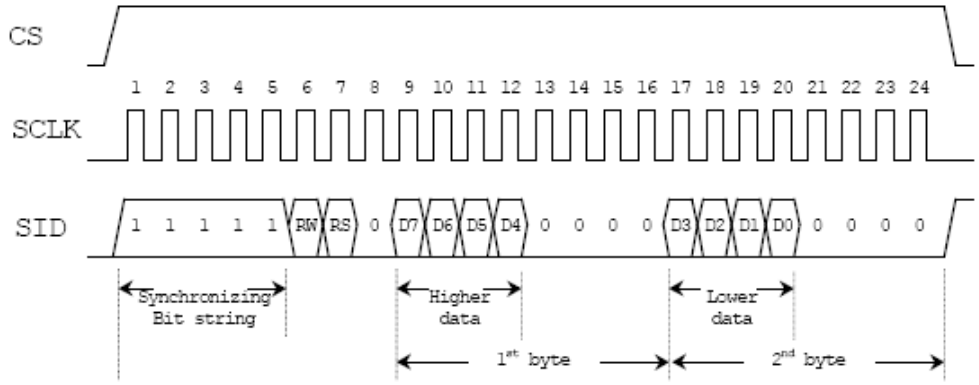
Timing Diagram of 4-bit Parallel Bus Mode Data Transfer

■ Serial Interface & Transferring Serial Data

The LCD module enters serial mode when the PSB pin is set low. A two-line clock synchronous transfer method is used. The module receives serial input data (SID) by synchronizing with a transfer clock (SCLK) sent from the master side. When the st7920 interfaces with several chips, chip select pin (CS) must be used. The transfer clock (SCLK) input is activated by making chip select (CS) high. In addition, the transfer counter of the st7920 can be reset and serial transfer synchronized by making chip select (CS) low. Here, since the data which was being sent at reset is cleared, restart the transfer from the first bit of this data. In a minimum system where a single module interfaces to a single MPU, an interface can be constructed from the transfer clock (SCLK) and serial input data (SID). In this case, chip select (CS) should be fixed to high.

the transfer clock(SCLK) is independent of operational clock of the LCD module. However, when several instructions are continuously transferred, the instruction execution time determined by the operational clock must be considered since the st7920 does not have an internal transmit/receive buffer. Following figure shows the basic procedure for transferring serial data. To begin with, transfer the start byte. By receiving five consecutive bits of 1(synchronizing bit string) at the beginning of the start byte, the transfer counter of the st7920 is reset and serial transfer is synchronized. The 2 bits following the synchronizing bit string(5 bits) specify transfer direction(R/W bit) and register select(RS bit). Be sure to transfer 0 in the 8 bit.

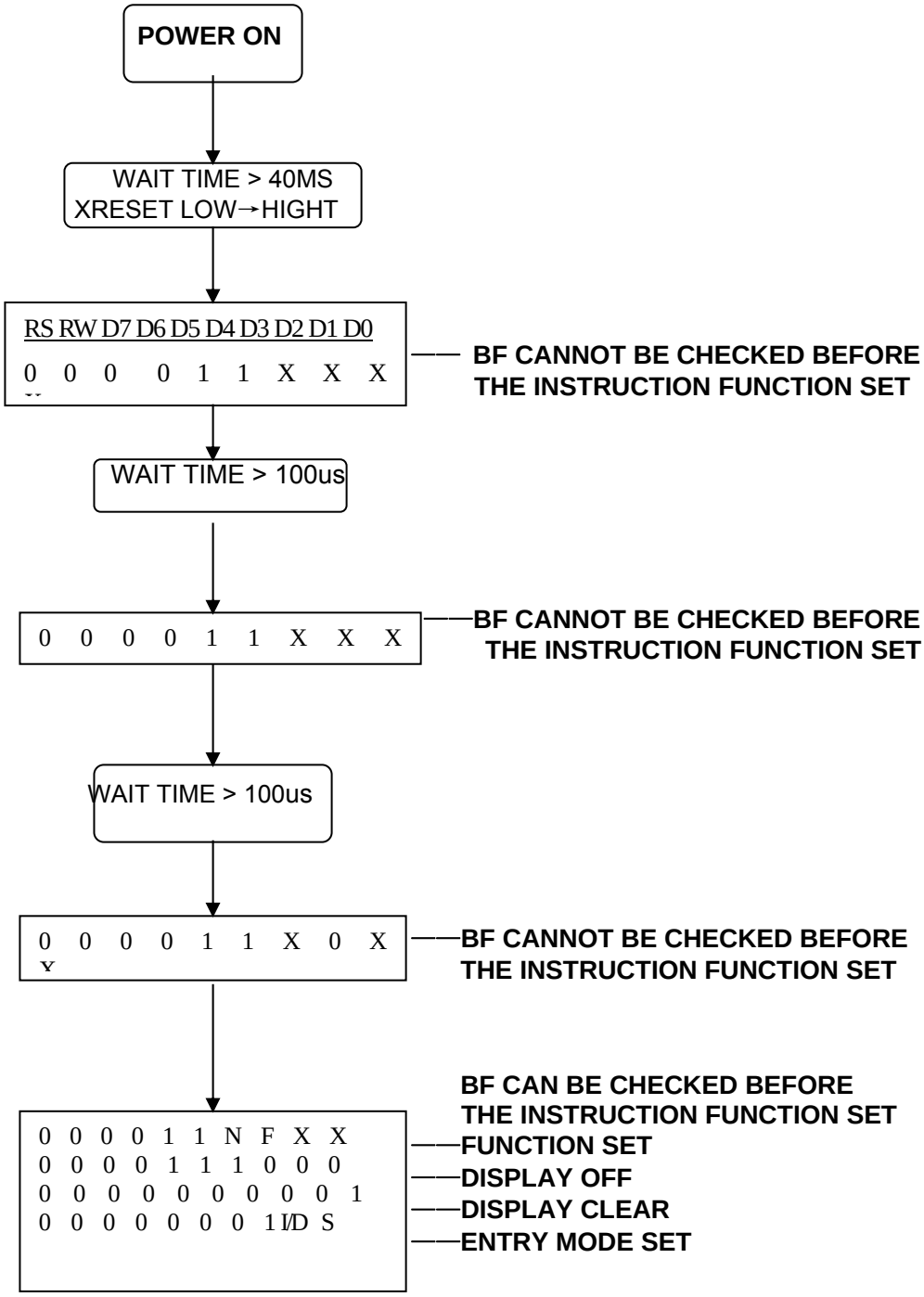
After receiving the start synchronizing bit string, the R/W bit (=0), and RS bit in the start byte, an 8-bit instruction is received in 2 bytes: the higher 4 bits of the instruction are placed in the lsb of the first byte, and the lower 4 bits of the instruction are placed in the lsb of the second byte. Be sure to transfer 0 in the following 4 bits of each byte.

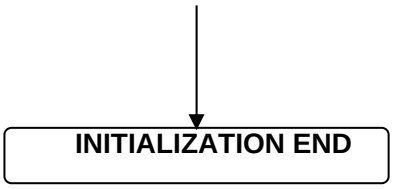


Timing Diagram of Serial Mode Data Transfer

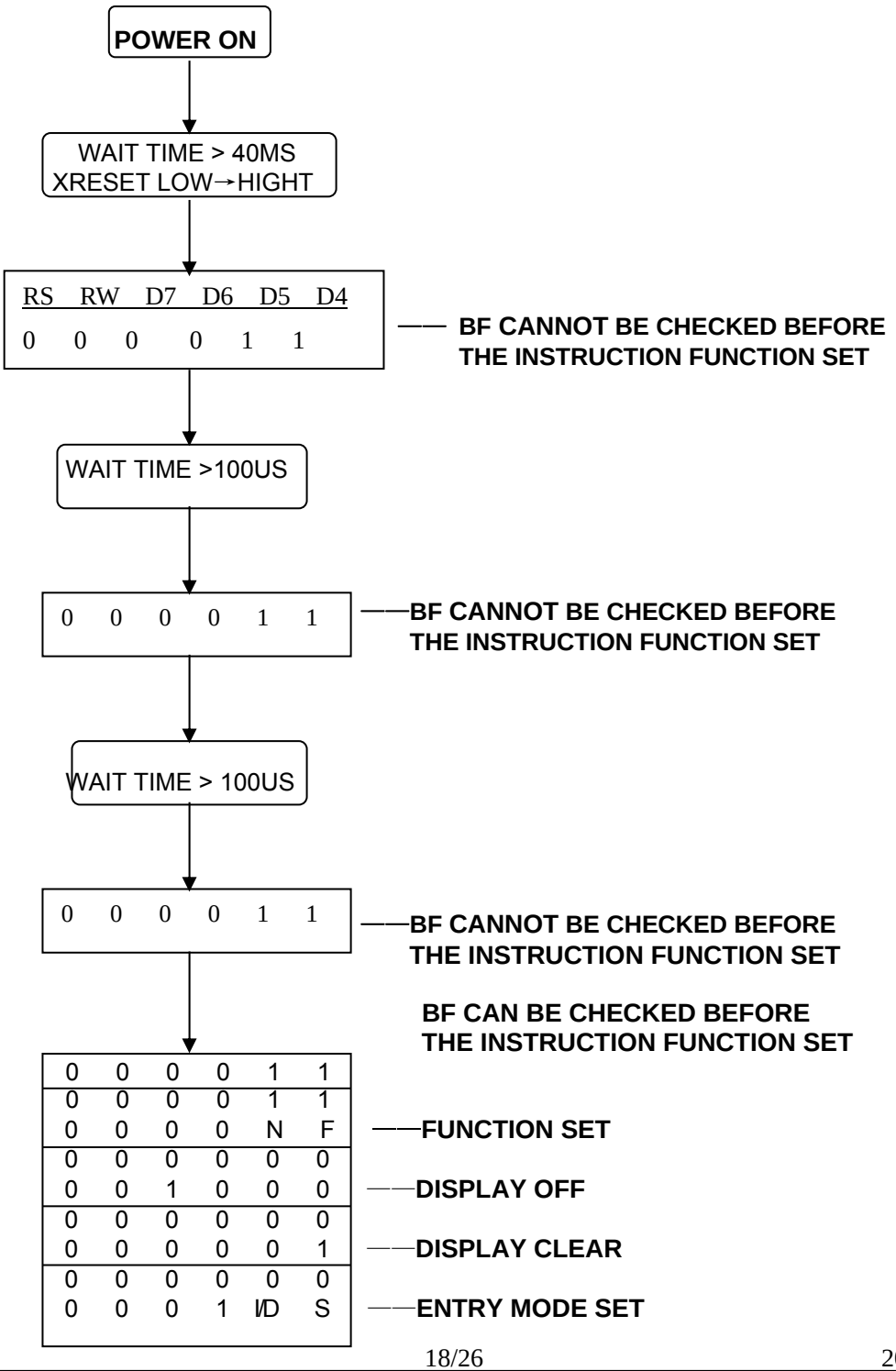
2. INITIALIZING BY INSTRUCTION

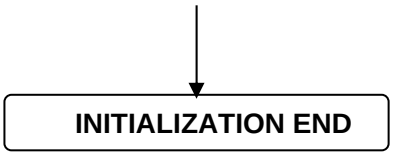
- 8-BIT INTERFACE:





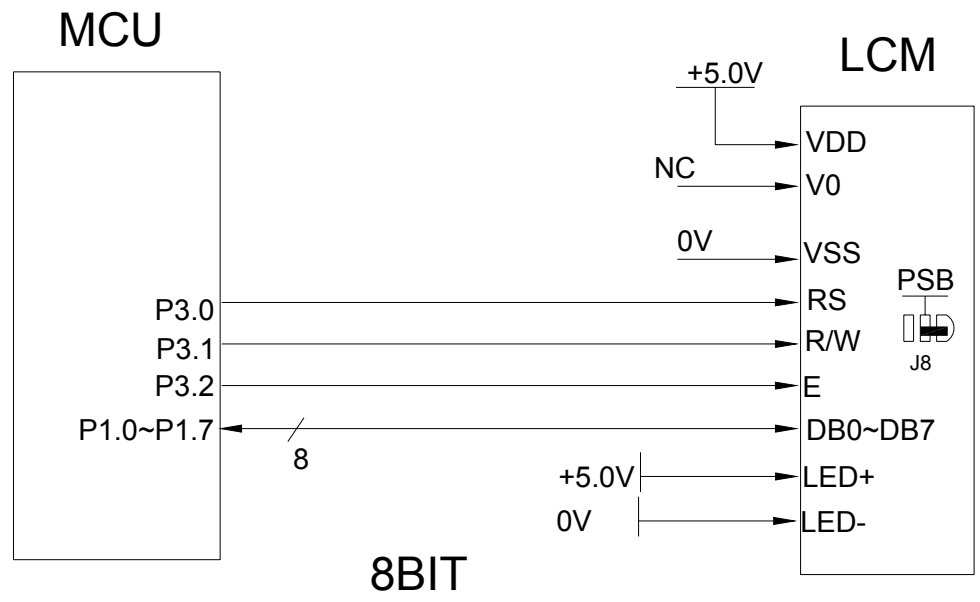
- **4-BIT INTERFACE**



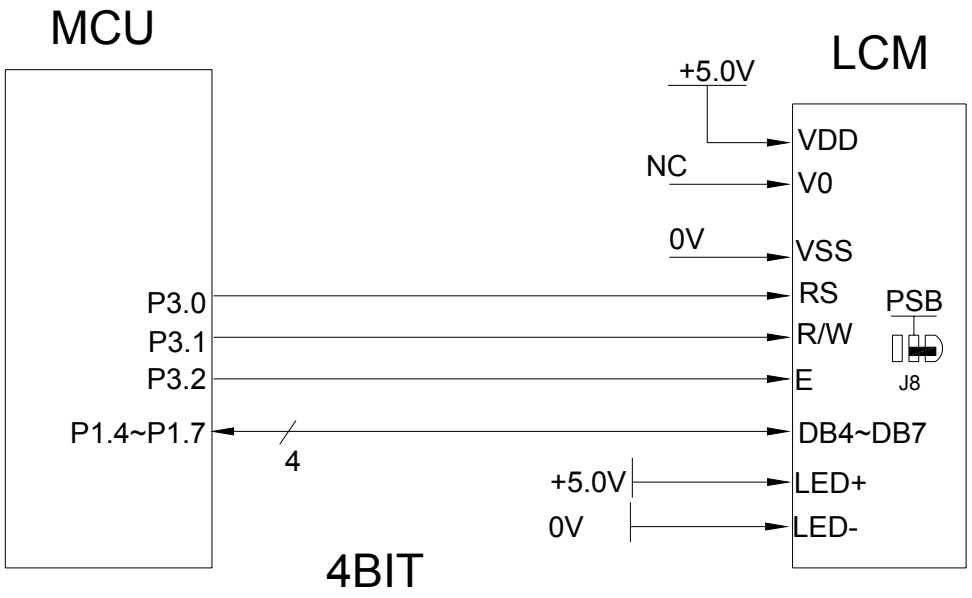


Product	Font Type
ST7920-0A	BIG-5 code traditional character set
ST7920-0B	GB code simplified character set
ST7920-0C	GB code,BIG-5 code and Japanese code

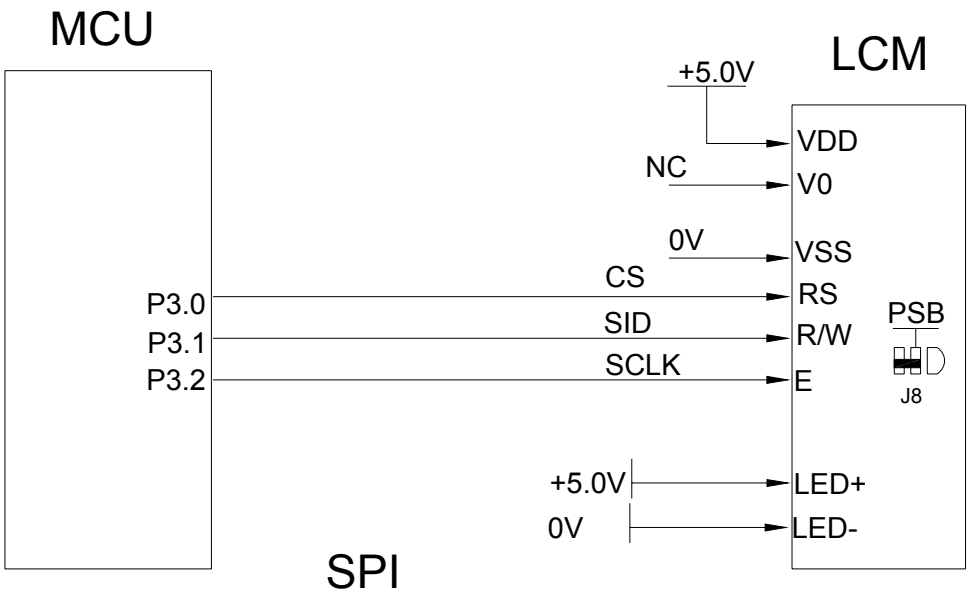
Interface to communicate with MPU



8BIT



4BIT



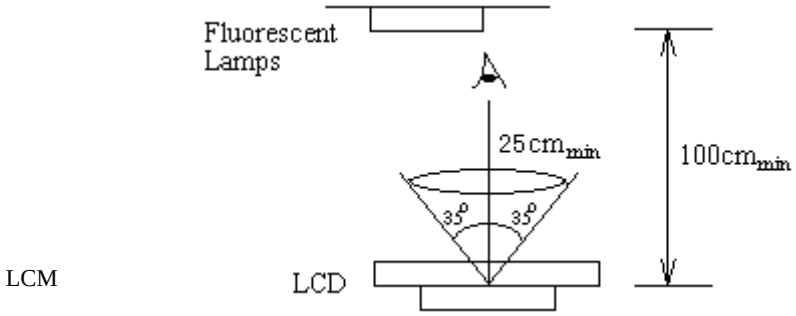
SPI

QUALITY SPECIFICATIONS

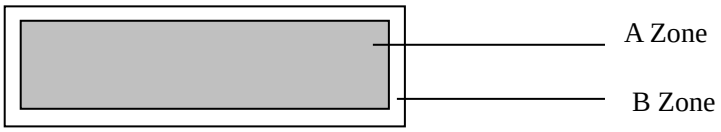
1 Standard of the product appearance test

Manner of appearance test: The inspection should be performed in using 20W x 2 fluorescent lamps. Distance between LCM and fluorescent lamps should be 100 cm or more. Distance between LCM and inspector eyes should be 25 cm or more.

Viewing direction for inspection is 35° from vertical against LCM.



Definition of zone:



A Zone: Active display area (minimum viewing area).
B Zone: Non-active display area (outside viewing area).

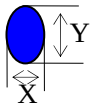
2 Specification of quality assurance

AQL inspection standard
Sampling method: GB2828-87, Level II, single sampling
Defect classification **(Note: * is not including)**

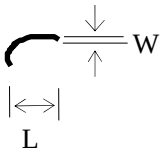
Classify	Item		Note	AQL
Major	Display state	Short or open circuit	1	0.65
		LC leakage		
		Flickering		
		No display		
		Wrong viewing direction		
		Contrast defect (dim, ghost)	2	
		Back-light	1,8	
	Non-display	Flat cable or pin reverse	10	
		Wrong or missing component	11	
Minor	Display state	Background color deviation	2	1.0
		Black spot and dust	3	
		Line defect, Scratch	4	
		Rainbow	5	
		Chip	6	
		Pin hole	7	
	Polarizer	Protruded	12	
		Bubble and foreign material	3	
	Soldering	Poor connection	9	
	Wire	Poor connection	10	
	TAB	Position, Bonding strength	13	

Note on defect classification

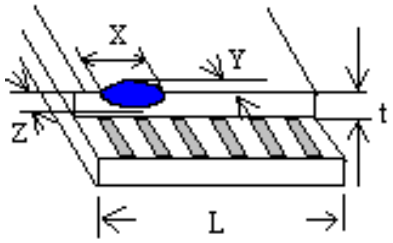
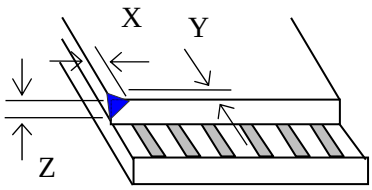
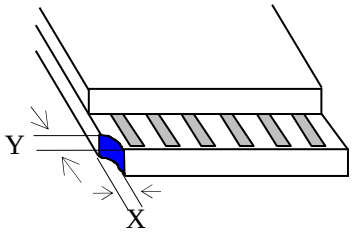
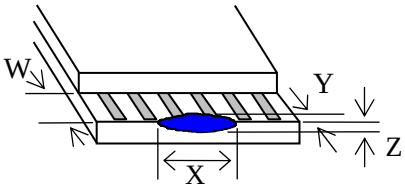
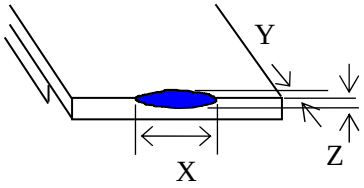
<table>
<tr><th>No.</th><th>Item</th><th>Criterion</th></tr>
<tr><td rowspan="6">1</td><td>Short or open circuit</td><td rowspan="6">Not allow</td></tr>
<tr><td>LC leakage</td></tr>
<tr><td>Flickering</td></tr>
<tr><td>No display</td></tr>
<tr><td>Wrong viewing direction</td></tr>
<tr><td>Wrong Back-light</td></tr>
<tr><td>2</td><td>Contrast defect
Backgroundcolor deviation</td><td>Refer to approval sample</td></tr>
<tr><td>3</td><td>Point defect,
Black spot, dust
(including Polarizer)

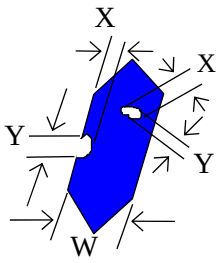
ϕ = (X+Y)/2</td><td> 

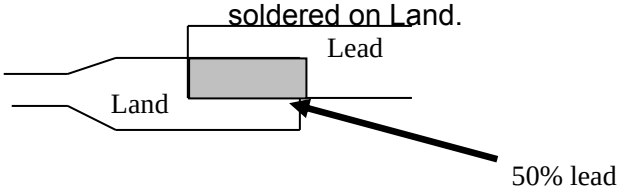
<table>
<tr><th>Point Size</th><th>Acceptable Qty.</th></tr>
<tr><td>ϕ≤0.10</td><td>Disregard</td></tr>
<tr><td>0.10<ϕ≤0.15</td><td>2</td></tr>
<tr><td>0.15<ϕ≤0.25</td><td>1</td></tr>
<tr><td>ϕ>0.25</td><td>0</td></tr>
</table>
Unit：Inch^2</td></tr>
<tr><td>4</td><td>Line defect,

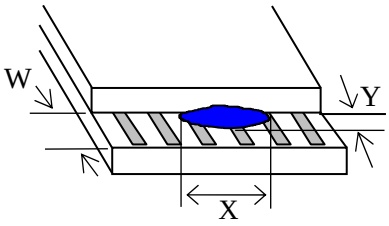
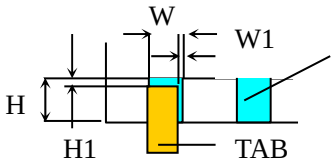
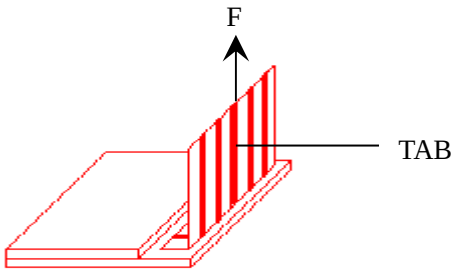
Scratch</td><td> 

<table>
<tr><th colspan="2">Line</th><th>Acceptable Qty.</th></tr>
<tr><td>L</td><td>W</td><td></td></tr>
<tr><td>---</td><td>0.05>W</td><td rowspan="3">Disregard</td></tr>
<tr><td>3.0>L</td><td>0.1>W>0.05</td></tr>
<tr><td>2.0>L</td><td>0.15≥W>0.1</td></tr>
</table>
Unit: mm</td></tr>
<tr><td>5</td><td>Rainbow</td><td>Not more than two color changes across the viewing area.</td></tr>
</table>

No	Item	Criterion
6	Chip Remark: X: Length direction Y: Short direction Z: Thickness direction t: Glass thickness W: Terminal Width L:Glass length	 Acceptable criterion X: < L /8; Y: 0.5mm; Z: ≤t/2  Acceptable criterion X: ≤2; Y: 0.5mm; Z: ≤t  Acceptable criterion X: ≤3; Y: ≤2; Z: ≤t shall not reach to ITO  Acceptable criterion X: Disregard; Y: ≤0.2; Z: ≤t  Acceptable criterion X: ≤5; Y: ≤2; Z: ≤t/3

<table>
<tr><th>No.</th><th>Item</th><th>Criterion</th></tr>
<tr><td>7</td><td>Segment
pattern
W = Segment width
ϕ = (X+Y)/2</td><td>(1) Pin hole
ϕ < 0.10mm is acceptable.
 

<table>
<tr><th>Point Size</th><th>Acceptable Qty</th></tr>
<tr><td>ϕ≤1/4W</td><td>Disregard</td></tr>
<tr><td>1/4W< ϕ≤1/2W</td><td>1</td></tr>
<tr><td>ϕ>1/2W</td><td>0</td></tr>
</table>
Unit: mm</td></tr>
<tr><td>8</td><td>Back-light</td><td>(1) The color of backlight should correspond its specification.
(2) Not allow flickering</td></tr>
<tr><td>9</td><td>Soldering</td><td>(1) Not allow heavy dirty and solder ball on PCB.
(The size of dirty refer to point and dust defect)
(2) Over 50% of lead should be soldered on Land.
 
</td></tr>
<tr><td>10</td><td>Wire</td><td>(1) Copper wire should not be rusted
(2) Not allow crack on copper wire connection.
(3) Not allow reversing the position of the flat cable.
(4) Not allow exposed copper wire inside the flat cable.</td></tr>
<tr><td>11*</td><td>PCB</td><td>(1) Not allow screw rust or damage.
(2) Not allow missing or wrong putting of component.</td></tr>
</table>

No	Item	Criterion
12	Protruded W: Terminal Width	 Acceptable criteria: Y ≤ 0.4
13	TAB	1. Position  W1≤1/3W H1≤1/3H 2 TAB bonding strength test  P (=F/TAB bonding width) ≥650gf/cm ,(speed rate: 1mm/min) 5pcs per SOA (shipment)
14	Total no. of acceptable Defect	A. Zone Maximum 2 minor non-conformities per one unit. Defect distance: each point to be separated over 10mm B. Zone It is acceptable when it is no trouble for quality and assembly in customer's end product.

3 Reliability of LCM

Reliability test condition:

Item	Condition	Time (hrs)	Assessment
High temp. Storage	80°C	48	No abnormalities in functions and appearance
High temp. Operating	70°C	48	
Low temp. Storage	-30°C	48	
Low temp. Operating	-20°C	48	
Humidity	40°C/ 90%RH	48	
Temp. Cycle	0°C ← 25°C →50°C (30 min ← 5 min → 30min)	10cycles	

Recovery time should be 24 hours minimum. Moreover, functions, performance and appearance shall be free from remarkable deterioration within 50,000 hours under ordinary operating and storage conditions room temperature (20±8°C), normal humidity (below 65% RH), and in the area not exposed to direct sun light.

Precaution for using LCD/LCM

LCD/LCM is assembled and adjusted with a high degree of precision. Do not attempt to make any alteration or modification. The followings should be noted.

General Precautions:

1. LCD panel is made of glass. Avoid excessive mechanical shock or applying strong pressure onto the surface of display area.
2. The polarizer used on the display surface is easily scratched and damaged. Extreme care should be taken when handling. To clean dust or dirt off the display surface, wipe gently with cotton, or other soft material soaked with isoproply alcohol, ethyl alcohol or trichlorotriflorothane, do not use water, ketone or aromatics and never scrub hard.
3. Do not tamper in any way with the tabs on the metal frame.
4. Do not make any modification on the PCB without consulting XIAMEM OCULAR
5. When mounting a LCM, make sure that the PCB is not under any stress such as bending or twisting. Elastomer contacts are very delicate and missing pixels could result from slight dislocation of any of the elements.
6. Avoid pressing on the metal bezel, otherwise the elastomer connector could be deformed and lose contact, resulting in missing pixels and also cause rainbow on the display.
7. Be careful not to touch or swallow liquid crystal that might leak from a damaged cell. Any liquid crystal adheres to skin or clothes, wash it off immediately with soap and water.

Static Electricity Precautions:

1. CMOS-LSI is used for the module circuit; therefore operators should be grounded whenever he/she comes into contact with the module.
2. Do not touch any of the conductive parts such as the LSI pads; the copper leads on the PCB and the interface terminals with any parts of the human body.
3. Do not touch the connection terminals of the display with bare hand; it will cause disconnection or defective insulation of terminals.
4. The modules should be kept in anti-static bags or other containers resistant to static for storage.
5. Only properly grounded soldering irons should be used.
6. If an electric screwdriver is used, it should be grounded and shielded to prevent sparks.
7. The normal static prevention measures should be observed for work clothes and working benches.
8. Since dry air is inductive to static, a relative humidity of 50-60% is recommended.

Soldering Precautions:

1. Soldering should be performed only on the I/O terminals.
2. Use soldering irons with proper grounding and no leakage.
3. Soldering temperature: 280°C±10°C
4. Soldering time: 3 to 4 second.
5. Use eutectic solder with resin flux filling.
6. If flux is used, the LCD surface should be protected to avoid spattering flux.
7. Flux residue should be removed.

Operation Precautions:

1. The viewing angle can be adjusted by varying the LCD driving voltage Vo.
2. Since applied DC voltage causes electro-chemical reactions, which deteriorate the display, the applied pulse waveform should be a symmetric waveform such that no DC component remains. Be sure to use the specified operating voltage.
3. Driving voltage should be kept within specified range; excess voltage will shorten display life.
4. Response time increases with decrease in temperature.
5. Display color may be affected at temperatures above its operational range.
6. Keep the temperature within the specified range usage and storage. Excessive temperature and humidity could cause polarization degradation, polarizer peel-off or generate bubbles.
7. For long-term storage over 40°C is required, the relative humidity should be kept below 60%, and avoid direct sunlight.

Limited Warranty

XIAMEM OCULAR LCDs and modules are not consumer products, but may be incorporated by XIAMEM OCULAR 's customers into consumer products or components thereof, XIAMEM OCULAR does not warrant that its LCDs and components are fit for any such particular purpose.

1. The liability of XIAMEM OCULAR is limited to repair or replacement on the terms set forth below. XIAMEM OCULAR will not be responsible for any subsequent or consequential events or injury or damage to any personnel or user including third party personnel and/or user. Unless otherwise agreed in writing between XIAMEM OCULAR and the customer, XIAMEM OCULAR will only replace or repair any of its LCD which is found defective electrically or visually when inspected in accordance with XIAMEM OCULAR general LCD inspection standard . (Copies available on request)
2. No warranty can be granted if any of the precautions state in handling liquid crystal display above has been disregarded. Broken glass, scratches on polarizer mechanical damages as well as defects that are caused accelerated environment tests are excluded from warranty.
3. In returning the LCD/LCM, they must be properly packaged; there should be detailed description of the failures or defect.