SPECIFICATION

Customer: _____

Basic Model: SAT024CP24D04R1-24042U 023ZN-RTP

Model Name: _____

ERP NO.: 1010240001

Spec Vision: _____

Date: _____

☐ Preliminary Specification

☐ Final Specification

Approved by	Comment

Prepared by	Reviewed by	Approved by

Contents

1 .REVISION STATUS

Version	Revise Date	Page	Content	Modified by
V1.0	2018.01.07	-	First Issued.	

2.Numbering System

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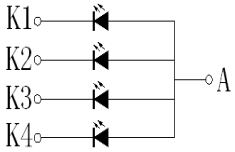
A B C D E F G H I J K L M

No.	Definition	Specifications						
A	**TFT LCM Productor No.**	**SAT INTERNATIONAL CO.LTD.**						
B	**Display monitor opposite angle linesize**	Unit:mm(size<10inch:takes two integers;size>=10inch:takes three integers)						
C	**LCD Brands**	CP--CPT; AU--AUO; PV--PVI; TM--TIANMA; HS--HSD; CM--CMO; IV--IVO; BO--BOE; AT--INNOLUX						
D	**Interface PIN Numbers**	By two figures characters expression from 01 to 99						
E	**LCD Type**	A--Alternated Viode Signal; D--Data Viode Signal; H--High Definition ; I--IPS						
F	**Back Light Circuit Diagram**	4		Min	Typ	Max	Unit	
				60	80	100	Ma	
				3.0	3.3		V	
G	**The Back Light Color Area Definition**	R2	X=0.282 Y=0.335					
		Y0	X=0.268 Y=0.296					
		Y1	X=0.281 Y=0.312					
		B1	X=0.270 Y=0.291					
		B2	X=0.253 Y=0.292					
H	**Structure Size**	2.4inch	24042	Thick:2.4mm Width42.72mm				
I	**Interface Mode**	T: TTL L: LVDS M: MIPI U: MPU						
J	**FPC Length**	It represents the length of FPC with three figures, divided into long rows , middle rows and short rows.						

K	**View Angles CR 10**	Symbol	Condition	Values									Unit
				Z			K			I			
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
		ϕ_L	ĭ=180°(9 o'clock)	..	40	..	..	60	..	..	85	..	Degree
		ϕ_R	ĭ=0°(3 o'clock)	..	50	..	..	70	..	..	85	..	
		ϕ_T	ĭ=90°(12 o'clock)	..	50	..	..	70	..	..	85	..	
		ϕ_B	ĭ=270°(6 o'clock)	..	50	..	..	70	..	..	85	..	

L :	**Operating Mode**	D: DE mode V: VSD mode F: Inverting mode N: No mode requirements
M	**Suffix**	1.NULL ; 2.TP-- Touch panel; 3.other--Insignificance

Remark : Will be subject to actual sample

3. General Specifitions

No.	Item	Specification	Unit
1	Panel Size	2.4”	inch
2	Number of Pixels	240×RGB (3)×320	pixels
3	Active Area	36.72(W)x48.96 (H)	mm
4	Pixel Pitch	0.153 (H)×0.153 (V) x RGB	mm
5	Outline Dimension	42.72(W)×60.26(H)×3.40(D)	mm
6	Pixel arrangement	RGB vertical stripe	-
7	Display Mode	normally white	-
8	Viewing Direction	12 O’CLOCK	-
9	Display Color	16.7M	-
10	Interface	MPU	-
11	Operation Temperature	-10~60	℃
12	Storage Temperature	-20~60	℃
13	Weight	TBD	g

4. Pin Assignment

No.	Symbol	Function	Remark
1	D0		
2	D1		
3	D2		
4	D3		
5	D4		
6	D5		
7	D6		
8	D7		
9	VDD		
10	GND		
11	NWR		
12	NRD		
13	RS		
14	NRST		
15	NCS		
16	GND		
17	LED+		
18	LED-		
19	GND		
20	GND		
21	YU		
22	XL		
23	YD		
24	XR		

5. Operatio n Spections

5.1 Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit
Digital Supply Voltage	VDD	-0.3	6.5	V
Digital Supply Voltage	IOVCC	-0.3	3	V

5.1.1 TFT LCD Module

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Digital Power Supply Voltage	VDD	3.0	3.3	3.6	V
Digital Power Supply Voltage	IOVCC	1.6	1.8	2.0	V

5.1.2 Current Consumption

Item	Symbol	Condition	Values			Unit
			Min.	Typ.	Max.	
Digital Current	IVDD	VDD = 3.3V	-	15	-	mA
Digital Current	IIOVCC	IOVCC=1.8V	-	10	-	mA

5.1.3 Backlight Driving Conditions (27 White Chips)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage of white LED backlight	VL	3.0	3.3	/	V	Note 1
Current for LED backlight	IL	60	80	100	mA	
Luminance (on the module surface,BM-7)		350	400	-	cd/m^2	
LED life time	-	50,000	-	-	Hr	Note 2

5.2 Power ON/OFF Sequence

VDDI and VDD can be applied in any order.

VDD and VDDI can be power down in any order.

During power off, if LCD is in the Sleep Out mode, VDD and VDDI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VDD can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

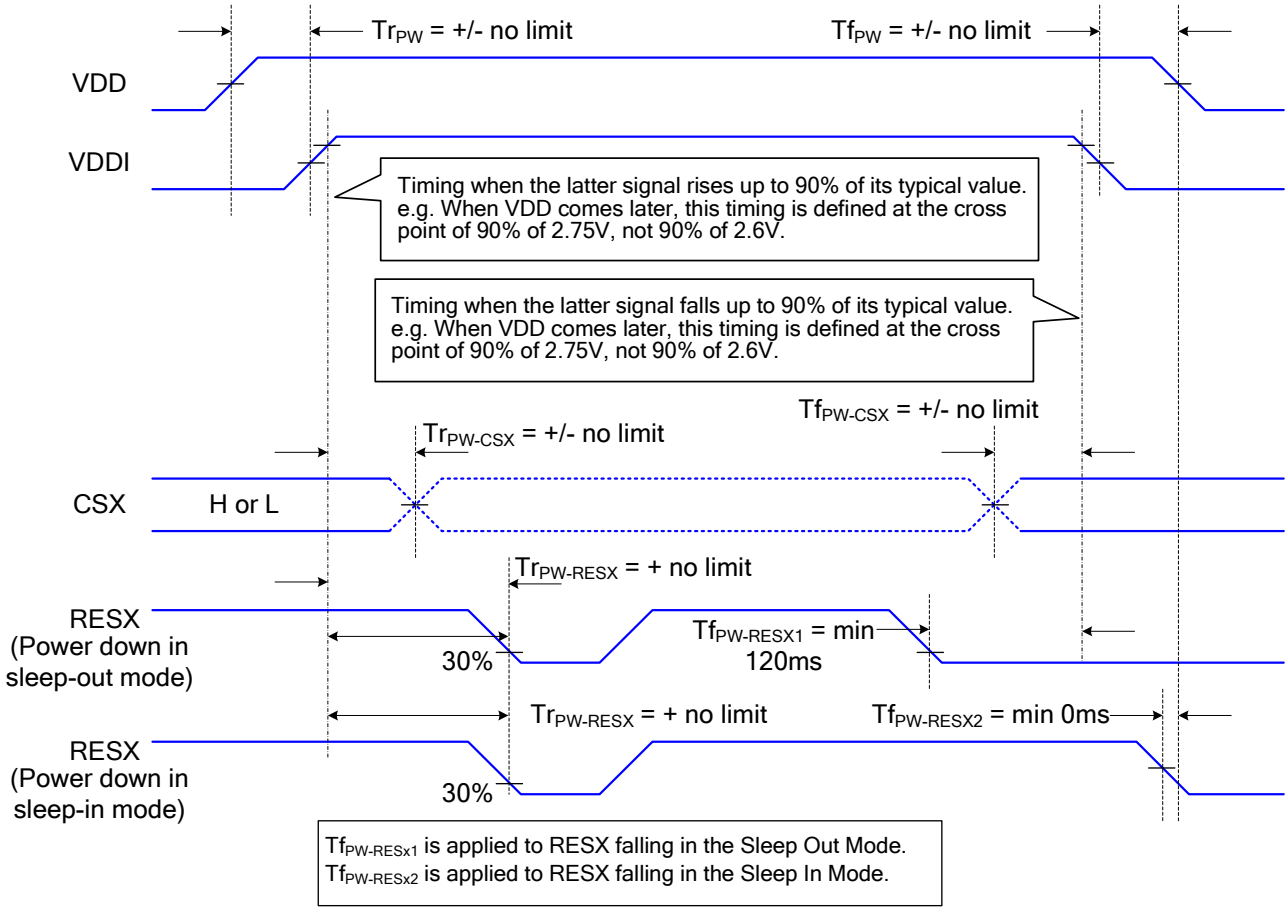
Note 1: There will be no damage to the display module if the power sequences are not met.

Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

Note 4: If RESX line is not held stable by host during Power On Sequence as defined in the sequence below, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below



5.3. DC Characteristics

5.3.1

Parameter	Symbol	Condition	Specification			Unit	Related Pins
			MIN.	TYP.	MAX.		
Power & Operation Voltage							
System Voltage	VDD	Operating voltage	2.4	2.75	3.3	V	
Interface Operation Voltage	VDDI	I/O Supply Voltage	1.65	1.8	3.3	V	
Gate Driver High Voltage	VGH		12.2		14.97	V	Note 4
Gate Driver Low Voltage	VGL		-12.5		-7.16	V	
Gate Driver Supply Voltage		| VGH-VGL |	19.36		27.47	V	Note 5
Input / Output							
Logic-High Input Voltage	VIH		0.7VDDI		VDDI	V	Note 1
Logic-Low Input Voltage	VIL		VSS		0.3VDDI	V	Note 1
Logic-High Output Voltage	VOH	IOH = -1.0mA	0.8VDDI		VDDI	V	Note 1
Logic-Low Output Voltage	VOL	IOL = +1.0mA	VSS		0.2VDDI	V	Note 1
Logic-High Input Current	IIH	VIN = VDDI			1	uA	Note 1
Logic-Low Input Current	IIL	VIN = VSS	-1			uA	Note 1
Input Leakage Current	IIL	IOH = -1.0mA	-0.1		+0.1	uA	Note 1
VCOM Voltage							
VCOM amplitude	VCOM			VSS		V	
Source Driver							
Source Output Range	Vsout		VAN		VAP	V	
Gamma Reference Voltage(Positive)	VAP		4.45		6.4	V	Note 6
Gamma Reference Voltage(Negative)	VAN		-4.6		-2.65	V	
Source Output Settling Time	Tr	Below with 99% precision			20	us	Note 2
Output Offset Voltage	VOFFSET				35	mV	Note 3

Table 2 Basic DC Characteristics

Notes:

1. TA= -30 to 70℃ (to +85℃ no damage).

2. Source channel loading= 2KΩ+12pF/channel, Gate channel loading=5KΩ+40pF/channel.

3. The Max. value is between measured point of source output and gamma setting value.

4. When evaluating the maximum and minimum of VGH, VDD=2.8V.

5. The maximum value of |VGH-VGL| can no over 30V.

6. Default register setting of Vcom and Vcomoffset is 20h

5.3.2 AC Characteristics

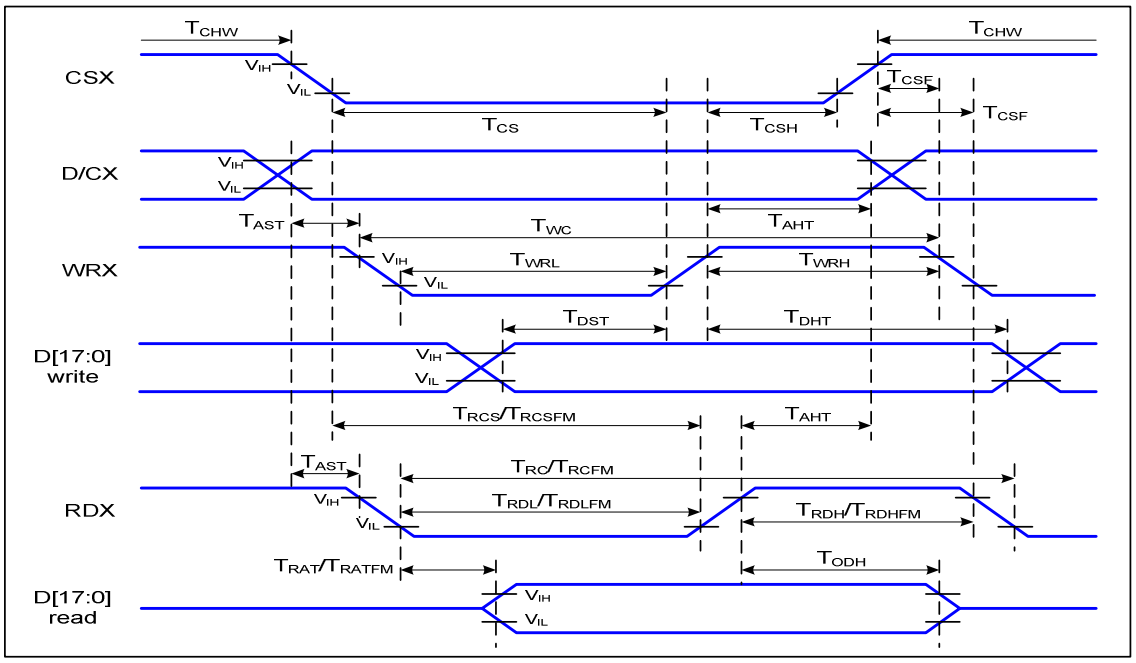


Figure 1 Parallel Interface Timing Characteristics (8080-Series MCU Interface)

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta= -30 to 70 ℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time	0		ns	-
	T_{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T_{CHW}	Chip select “H” pulse width	0		ns	-
	T_{CS}	Chip select setup time (Write)	15		ns	
	T_{RCS}	Chip select setup time (Read ID)	45		ns	
	T_{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T_{CSF}	Chip select wait time (Write/Read)	10		ns	
	T_{CSH}	Chip select hold time	10		ns	
WRX	T_{WC}	Write cycle	66		ns	
	T_{WRH}	Control pulse “H” duration	15		ns	
	T_{WRL}	Control pulse “L” duration	15		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	160		ns	When read ID data
	T_{RDH}	Control pulse “H” duration (ID)	90		ns	
	T_{RDL}	Control pulse “L” duration (ID)	45		ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T_{RDHFM}	Control pulse “H” duration (FM)	90		ns	
	T_{RDLFM}	Control pulse “L” duration (FM)	355		ns	
D[17:0]	T_{DST}	Data setup time	10		ns	For CL=30pF

	T_{DHT}	Data hold time	10		ns	
	T_{RAT}	Read access time (ID)		40	ns	
	T_{RATFM}	Read access time (FM)		340	ns	
	T_{ODH}	Output disable time	20	80	ns	

Table 4 8080 Parallel Interface Characteristics

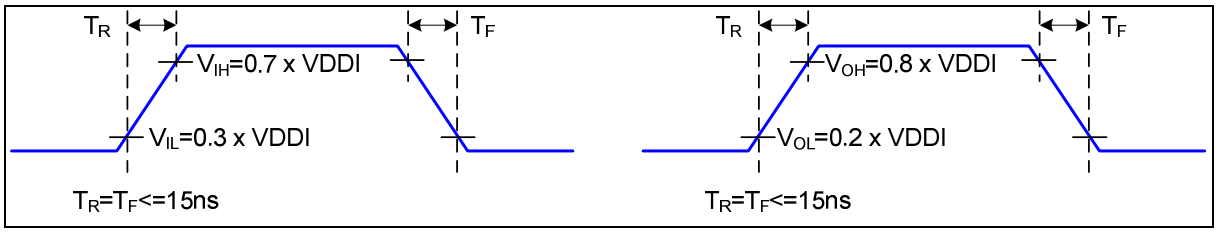


Figure 2 Rising and Falling Timing for I/O Signal

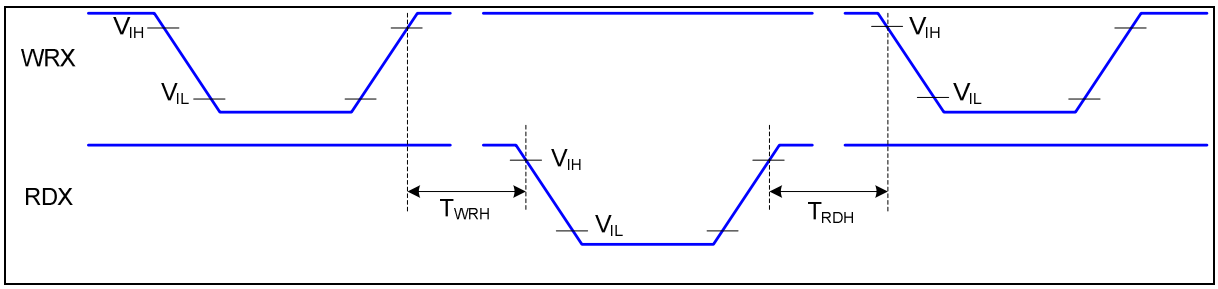


Figure 3 Write-to-Read and Read-to-Write Timing

Note: The rising time and falling time (Tr, Tf) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

5.3.3 Reset input timing

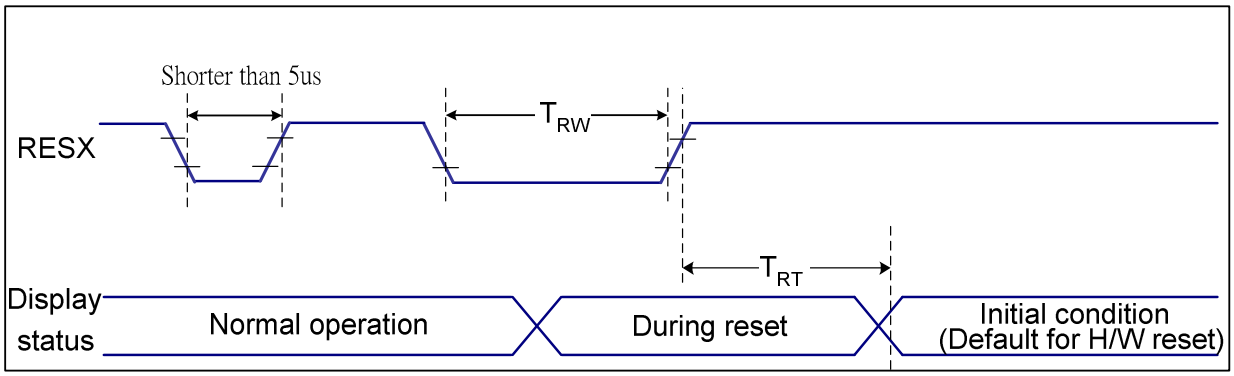


Figure 7 Reset Timing

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 ~ 70 ℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

Table 8 Reset Timing

Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:

6. Optical Specifications

Item		Symbol	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	-	800	-		Note1 Note3
Luminance(center)		L	350	400	-	cd/m2	Note1 Note5 Note7
Luminance uniformity		ΔL	70	75		%	Note7
Response Time		Rising + Falling	-	30	35	ms	Note1 Note4
Viewing Angle K=Contrast Ratio>10	Horizontal	θx^+		45	-	degree	Note2
		θx^-		45	-		
	Vertical	θy^+		50	-		
		θy^-		25	-		
Color Chromaticity (CIE1931)	Red	x	-0.05	0.610	+0.05		Note1 Note5 Note7
		y		0.331			
	Green	x		0.303			
		y		0.582			
	Blue	x		0.144			
		y		0.035			
	White	x		0.287			
		y		0.311			
Color gamut (NTSC ratio)				60		%	

6. .1 Backlighit Driving Table

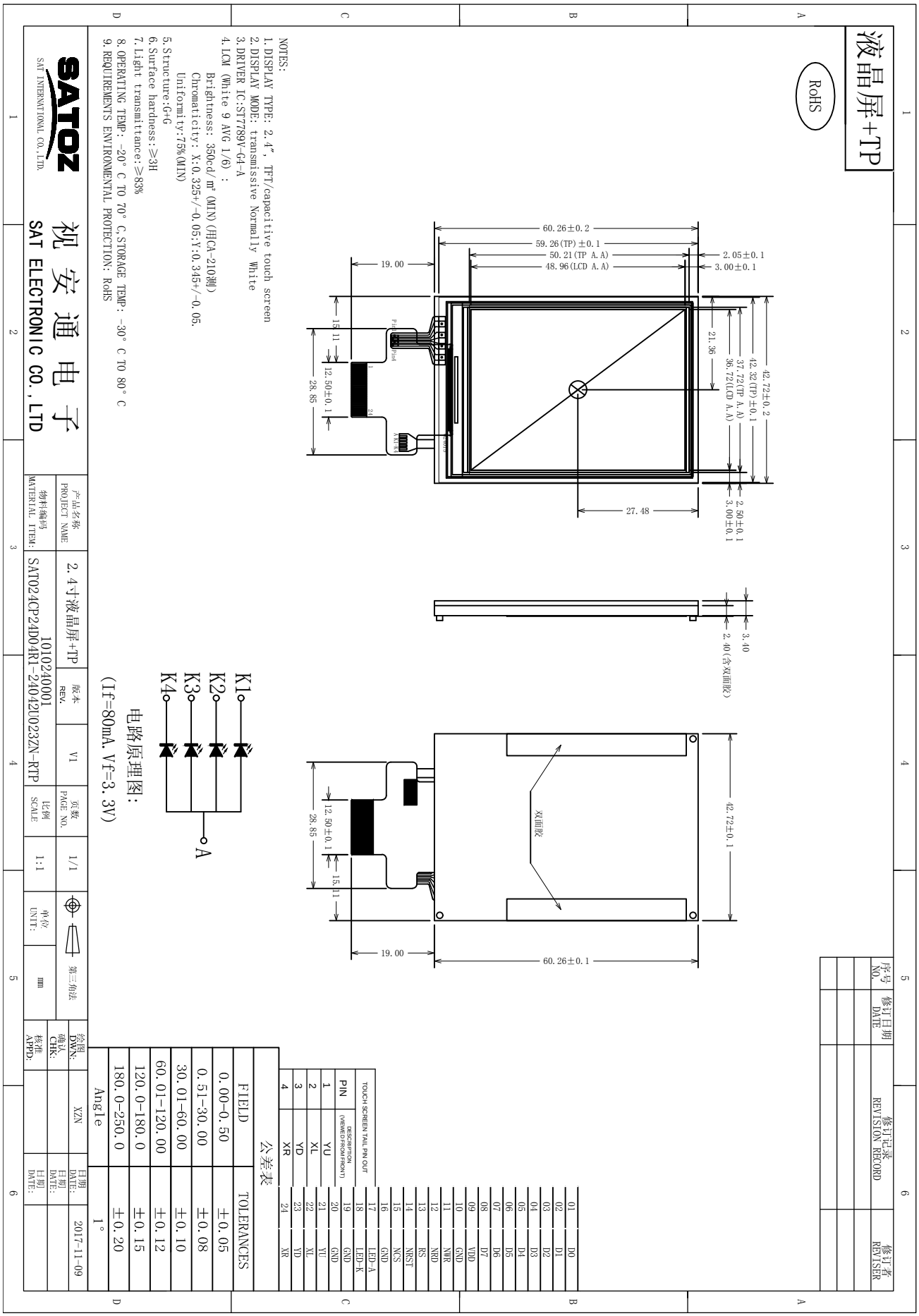
A	B	C	D	E	F	G	H	I	J	K L	M

B	E	H	F			
				28		
			Luminance(BM-7 cd/m2)			
			Min	Typ	Max	Unit
	,	24042	350	400		cd/m2

Test Conditions:

1. VDD3.3V;Backlight current Reference model(note4)
2.The amblent temperature is 25
3.Will be subject to actual sample

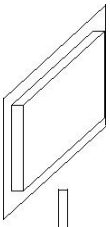
7. Mechanical Drawing



8. PACKAGE DRAWING

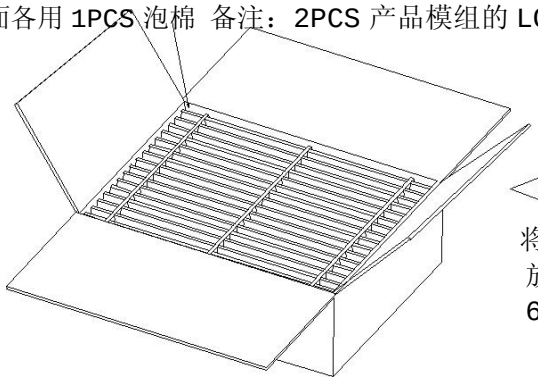
包装图：

将 1PCS 模组产品由 PE 袋包

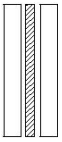


在纸箱里的卡板上下

两面各用 1PCS 泡棉 备注：2PCS 产品模组的 LCD 面对面，中间靠一张泡棉隔开



将 2PCS 产品放入小隔里，共计 60pcs



用泡棉隔开

使用封口胶封口并贴附唛头