LEADTEK GPS MODULE LR9130/LR9130P Specification Sheet

Features:

- *SiRF StarIV ultra low power chipset*
- *Compact module size for easy integration : 24 x 20 x 2.9 mm*
- *I^2C/SPI pins reserved for customizing special user applications*
- *Fully utilized SS4 upgrade features*

Version : 0.7

Change History

Rev.	Date	Change Description	Modified by	Remark
0.1	06, Oct., 2010	LR9130/P product specification Initialization	Jim Lin	
0.2	21, Oct., 2010	Sections & paragraph revised to emphasis key points	Jim Lin	
0.3	02, Nov., 2010	Update product photo	Jim Lin	
0.4	08, Dec., 2010	Sample Run data update	Jim Lin	
0.5	13, Jan., 2010	Interface definition for p-t-p & full function model GSD4e 2.0 software update new features	Jim Lin	
0.6	01, Mar., 2011	Contents Modify	Ken H.	
0.7	14, Apr, 2011	Update spec Modify	Ken H.	

Contents

1 Introduction

The Leadtek LR9130/LR9130P GPS module is a high sensitivity, low power, Surface Mount Device (SMD) that can be compatible to LR9548 or fully utilized SiRFstarIV upgrade features. This 48-channel global positioning system (GPS) receiver is designed for a wide range of OEM applications and is based on the GPS signal search capabilities of the SiRFstarIV GSD4e chipset, SiRF's newest chipset technology. The LR9130/LR9130P provides flexible I/O interfaces (UART , I^2C and SPI by customer requirement).

The LR9130/LR9130P is designed to allow quick and easy integration into GPS-related applications such as:

- PDA, Pocket PC, Tablet and other computing devices
- Fleet Management /Asset Tracking
- AVL and Location-Based Services
- Hand-Held Device for Personal Positioning and Navigation
- All applications of battery drive device that needs lower power consumption

1.1 Features

1.1.1 Performance

- Highest performance GPS PVT engine
- High acquisition sensitivity for fast TTFF
- Extremely low weak signal tracking sensitivity
- High jamming immunity
- Smallest footprint and total solution size
- Highest level of BOM integration
- Value added software enhancements
- Multimode A-GPS (Autonomous, MS-Based, and MS-Assisted) – Need operator support
- Embedded CGEE / SGEE (Need server support) speed up TTFF a lot and makes cold start time to be around 22 seconds.

- SiRFGeoRecov™ Reverse EE makes positioning process being done under power saving mode.
- Reacquisition Time: 0.1 second
- RF Metal Shield for best performance in noisy environments

1.1.2 Interface

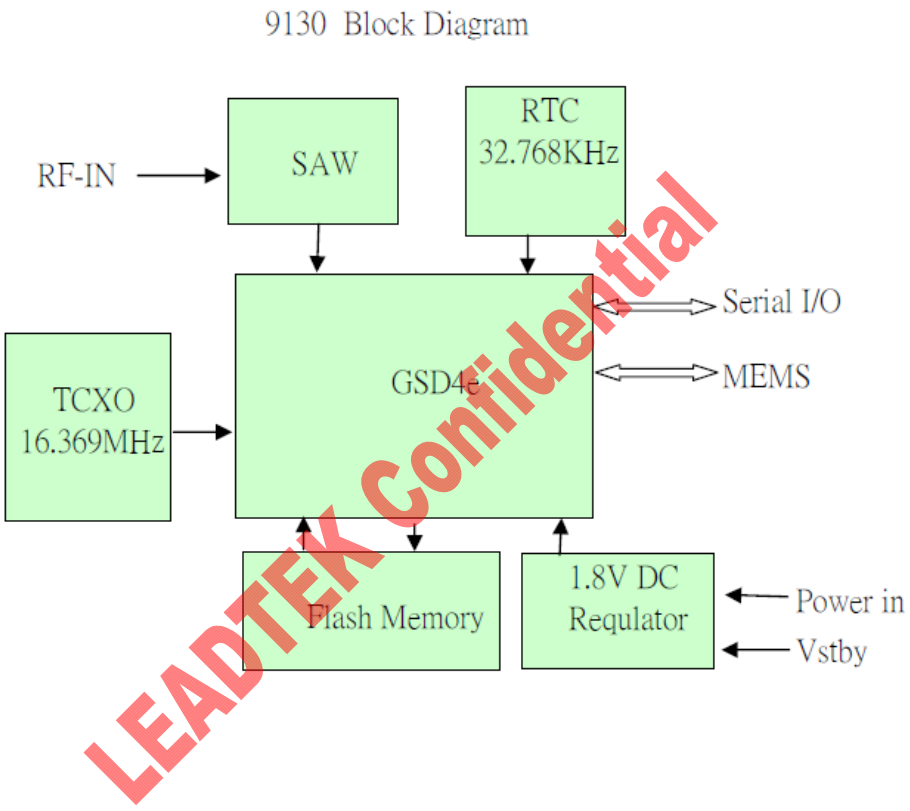
- Multiple host port interfaces (UART, I2C, and SPI)
- One I^2C port for MEMS connection
- Protocol: NMEA-0183(default)
- Baud Rate: 4800 bps

1.2 Advantages

- Built-in LNA.
- Embed CGEE (Client Generated Extended Ephemeris) that can capture ephemeris data from satellites locally and predicts ephemeris out to 3 days. So if the module was off within 3 days, it could complete positioning process within 2 seconds just like hot start.
- It can remove in-band jammer up to 80db-Hz and track up to 8CW jammers, so the module can prevent GPS signal interference when design-in the electrical device with noisy electrical signal interferences such as Laptop, mobile phone, DSC, etc.
- Maintain tracking sensitivity as low as -163dBm, even without network assistance. (SiRF StarIII has only -159dBm sensitivity)
- Support SiRFaware technology :
  - Support adaptive “Micro Power Controller” power management mode.
  - Support MEMS sensor through I^2C interface. (V4.X.X firmware will be supported) MEMS interrupt can improve MicroPower Mode performance.
  - Only 8mW Trickle Power, so user can leave power on all day instead of power off
- 5 Hz Navigation Update Rate: user can select 1 Hz or 5 Hz navigation update rate. (V4.1.0 firmware will be supported)
- SBAS Ranging: SBAS satellite measurements will be used in the navigation solution for improved DOP and coverage. (V4.1.0 firmware will support)
- Suitable for battery drive devices that need lower power consumption application

- Ideal for high volume mass production(Taping reel package)
- Cost saving through elimination of RF and board to board digital connectors
- Flexible and cost effective hardware design for different application needs

1.3 Block Diagram



2 Technical Specifications

2.1 Technical Specifications

2.1.1 Module Specification

Feature	Item	Description
Chipset	GSD4e	SiRFstarIV low power single chipset
General	Frequency C/A code Channels	L1, 1575.42 MHz 1.023 MHz chip rate 48
Accuracy	Position Velocity Time	< 2.5 meters 0.01 meters/second 1 microsecond synchronized to GPS time
Datum	Default Other	WGS-84 selectable for other Datum
Time to First Fix (TTFF -122dBm) (Open Sky & Stationary Requirements)	Reacquisition Snap start Hot start Warm start Cold start	0.1 sec., average 1 sec., average 1 ~ 2 sec. 9 ~ 15 sec. 25 ~ 35 sec.
Dynamic Conditions	Altitude Velocity Acceleration Jerk	18,000 meters (60,000 feet) max. 515 meters/second (1000 knots) max. 4g, max. 20 meters/second^3, max.
Power	Main power input Power Consumption Backup Power	2.8 ~ 5.0 VDC input 50mA (Tracking Mode) 2.8 ~ 5.0 VDC battery input
Serial Port	Electrical interface Protocol messages	Default UART:NMEA-0183@4800bps (I2C/SPI TBA)

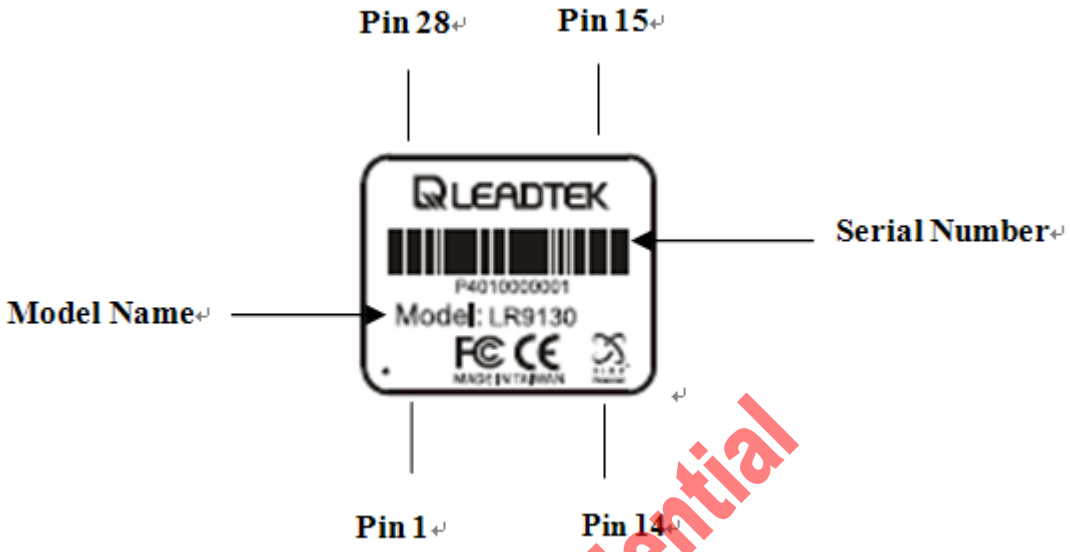
This model is defined to fully utilize SS4 extra upgrade features from SS3. Original design can also be compatible to LR9548S. The comparison is as below table:

2.1.2 Module Comparison

	GSD4e Feature List	LR9130P Compatible to LR9548S	LR9130 Full SS4 Features	Remark
	Power Management			
1	Full Power	●	●	
2	Trickle Power		●	
3	Push to Fix		●	
	Value added software enhancements			
4	Multimode A-GPS (Autonomous, MS-Based, and MS-Assisted)	●	●	Requires Operater Support
5	Embedded CGEE	●*	●	* Production version support
6	SGEE	●	●	Requires Host "downloader"
7	SiRFGeoRecov Reverse EE	●	●	For post-processed navigation computation
	Interface			
8	MEMS sensor I2C Interface		●	
9	Single 1.8 Vdc supply voltage		●	Option
10	2.8Vdc to 5.5Vdc supply Voltage	●	●	
11	Multiple host port interfaces UART/ I2C/SPI Bus:3.3V	●	●	Option, Selected by hardware pin(CTS/RTS) and it need to be selected by buyer before shipping
12	Single ON_OFF power control pin		●	
13	Wakeup pin for external regulator shutdown control		●	
14	Reset control pin	●*	●	* Production version support
15	Backup battery pin	●*	●	* Production version support
16	1.8V I/O interface	●	●	
	External Device Support			
17	MEMS support		●	

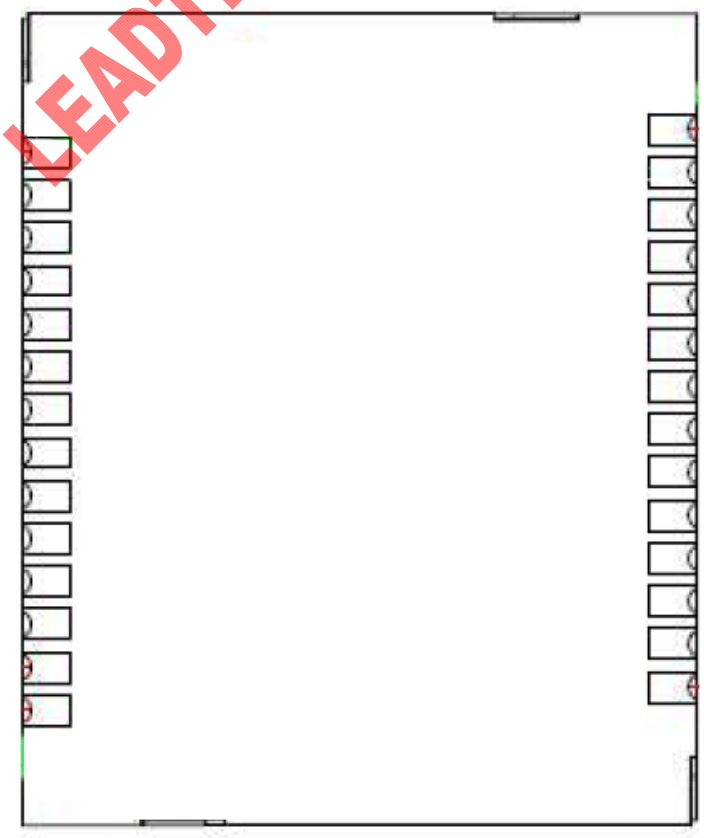
2.2 Electrical Specifications

2.2.1 Photo and Pin Positions



※ Model Name: LR9130=9130 Full Function;
※ Model Name: LR9130P=9130 Pin to Pin

2.2.2 Pin Location



2.2.3 Pin Assignment Comparison

	9548S	9130P (Pin to Pin)	9130 (Full Function)
1	NC (Reserved)	NC (Reserved)	GPIO3(ECLK) Reserved
2	NC (Reserved)	Reserved(WAKE)	WAKE
3	NC (Reserved)	NC (Reserved)	GPIO8 (EIT2) Reserved
4	RXDB	NC	NC
5	RXDA	RXA	RXA
6	TXDA	TXA	TXA
7	NC (Reserved)	Reserved(ON_OFF)	ON_OFF
8	TIME_MARK	TIME_MARK	TIME_MARK
9	NC (Reserved)	NC (Reserved)	VCC_1.8V (Reserved)
10	NC (Reserved)	CTS (Option)	CTS (Option)
11	NC (Reserved)	NC (Reserved)	GPIO4 (EIT) (Reserved)
12	NC (Reserved)	NC (Reserved)	GPIO2(TSYNC) (Reserved)
13	NC (Reserved)	RTS(Option)	RTS(Option)
14	GND	GND	GND
15	VSYSIN	VSYSIN (2.8~5.0V)	VSYSIN (2.8~5.0V)
16	VSTBY	VSTBY (2.8~5.0V)	VSTBY (2.8~5.0V)
17	BOOTSEL	BOOTSEL	BOOTSEL
18	RESETIN	RESETIN	RESETIN
19	GPS Status	NC	NC
20	GND	GND	GND
21	NC (Reserved)	NC (Reserved)	DR_SDA (Reserved)
22	NC (Reserved)	NC (Reserved)	DR_SCL (Reserved)
23	TXDB	NC	NC
24	NC (Reserved)	NC	NC
25	ANTPWR	ANTPWR	ANTPWR
26	GND	GND	GND
27	RF_IN	RF_IN	RF_IN
28	GND	GND	GND

2.3 Environment Characteristics

Item	Description
Operating temperature rang	-40 deg. C to +85 deg. C
Storage temperature range	-55 deg. C to +100 deg. C
Humidity	Up to 95% non-condensing or a wet bulb temperature of +35 deg. C

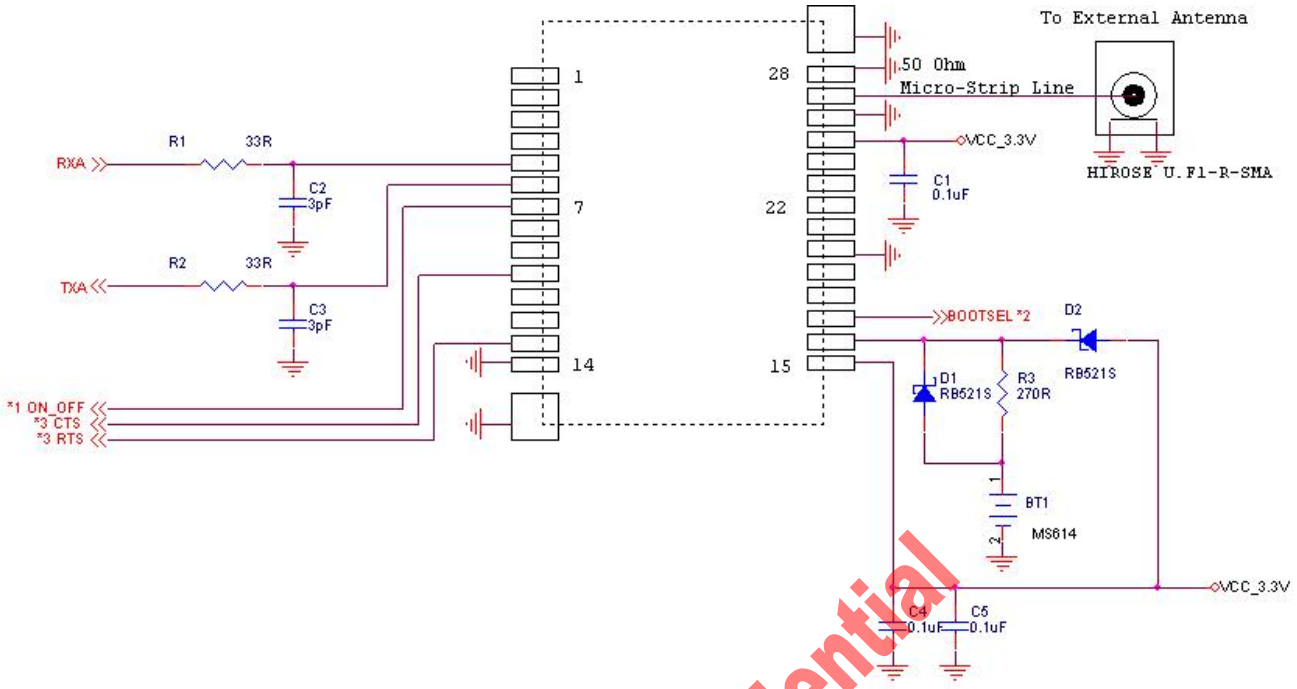
2.4 Physical Characteristics

Items	Description
Length	24 mm ± 0.3mm (0.94in)
Width	20 mm ± 0.3mm (0.79 in)
Height	2.9 mm ± 0.3mm (0.11 in)
Weight	2 gram

2.5 Interface Specification

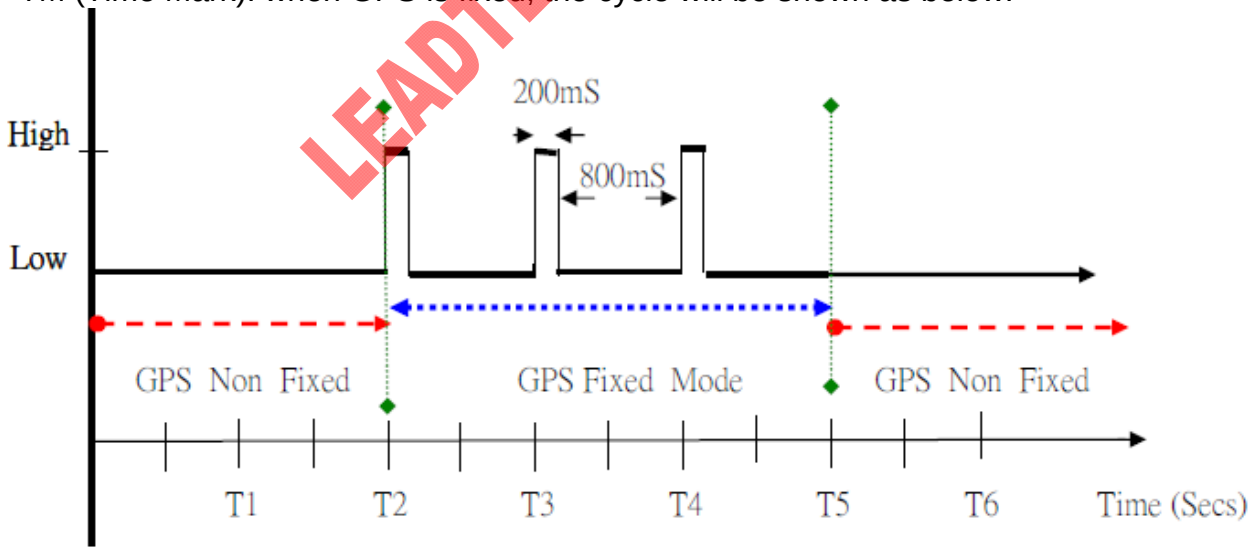
Items	*Description*
I/O	28 pin SMD micro package
Serial I/O	UART, I^2C, SPI by customer request

2.6 Reference Design



- All ground pads attach directly to ground plane by way of via.
- All components are reference only.

※ TM (Time Mark): when GPS is fixed, the cycle will be shown as below:



LR 9131 Time Mark Timing

2.6.1 *2 BOOTSEL Table

	BOOTSEL
Normal	L (GND)
Flash Loader	H (1.8/3.3V)

2.6.2 *3 Interface Selection

I/F	RTS	CTS
UART	--	H
I2C	L	--
SPI	--	--

Note :

1. Based on current official firmware, only support UART. The rest of interfaces will be available around middle of 2011.

3 Software

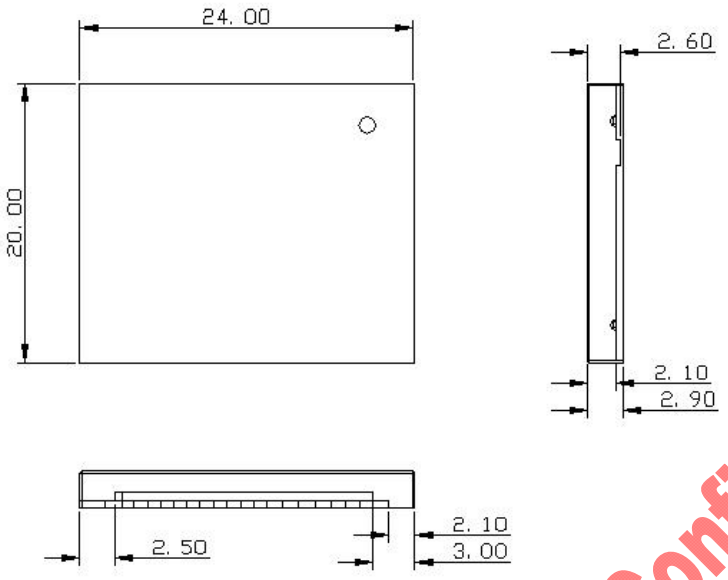
The Leadtek LR9130/LR9130P module includes GSD4e, the SiRF standard GPS software for SiRFstarIV low power single chipset receivers and its features include:

- Excellent sensitivity
- High configurability
- 1 Hz / 5 Hz (GSD4e_4.1.0) position update rate
- Supports use of SBAS(satellite-based augmentation systems), WAAS, EGNOS, MSAS, GAGAN
- Enhanced Navigation Performance
- Improved Jamming Mitigation
- Improved Ephemeris Availability
- Default configuration is as follows:

Item	Description
Core of firmware	SiRF GSD4e_4.1.0
Baud rate	4800 bps
Code type	NMEA-0183 ASCII
Datum	WGS-84
Protocol message	GGA(1s), GSA(1s), GSV(5s), RMC(1s)
Output frequency	1 Hz

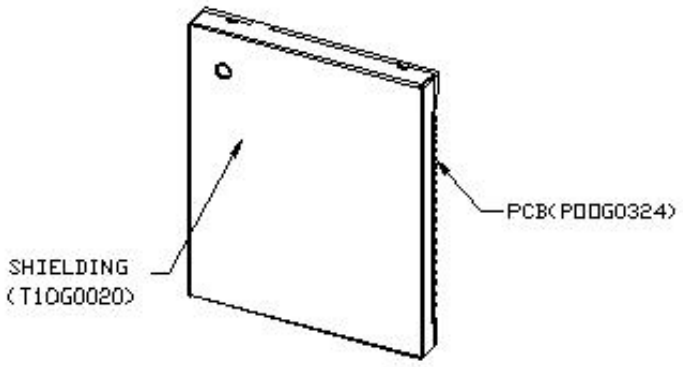
4 Mechanical Drawing and Footprint

4.1 Outline Drawing

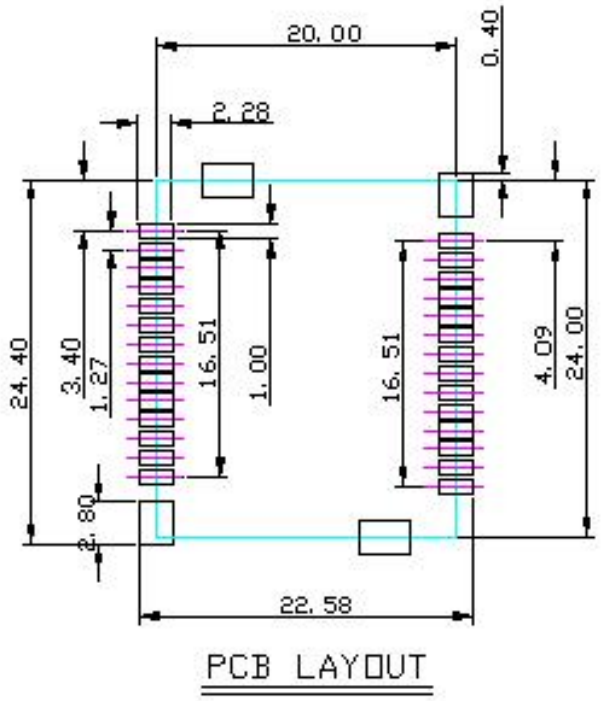


※ Tolerance

Length	24.0 ± 0.3 mm
Width	20.0 ± 0.3 mm
Height	2.90 ± 0.3 mm



4.2 Recommended Footprint

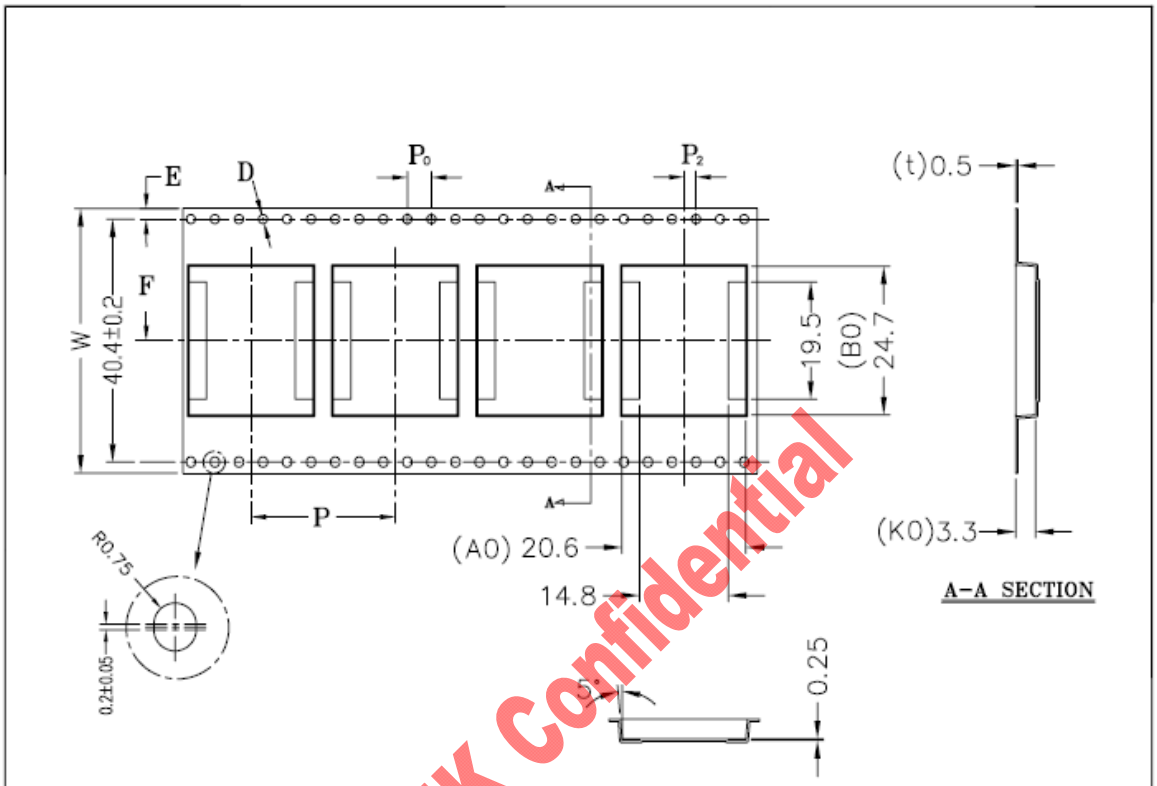


Unit : mm

5 Package Specification

(Unit : mm)

LR9130/LR9130P modules are shipped in the plastic carrier tape on the reel. Each 13” reel can hold maximum 500 pcs of modules. The tape and reel dimensions are shown in the following figures.



ｵ?1.A0=20.4ﾄｳﾀ?-20.6mm
2.B0=24.5ﾄｳﾀ?-24.7mm
3.K0=3.00ﾄｳﾀ?-3.30mm ｵﾈ.?5.02.09

ITEM	W	A_0	B_0	K_0	K_1	P	F	E	D	D_1	P_0	P_2
DIM	$44.0^{+0.30}_{-0.10}$	$20.6^{+0.10}_{-0.10}$	$24.7^{+0.10}_{-0.10}$	$3.30^{+0.10}_{-0.10}$	$00.0^{+0.00}_{-0.00}$	$24.0^{+0.10}_{-0.10}$	$20.2^{+0.10}_{-0.10}$	$1.75^{+0.10}_{-0.10}$	$1.50^{+0.10}_{-0.00}$	$0.00^{+0.00}_{-0.00}$	$4.00^{+0.10}_{-0.10}$	$2.00^{+0.10}_{-0.10}$
ALTERNATE												

Customer Approved: _____ Date: _____ ☐ Accept ☐ Reject Reason:

1. 10 sprocket hole pitch cumulative tolerance ±0.20mm.
2. Carrier camber not to exceed 1mm in 100mm.
3. A_0 and B_0 measured on a plane 0.3mm above the bottom of the pocket.
4. K_0 measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
5. All dimensions meet EIA-481-3 requirements.
6. Material: Black Anti-static Polystyrene.
7. Thickness: 0.50±0.05 mm.
8. Packing length per 22” reel : 51 Meters.
9. Component loaded per 15”reel : 1000 pcs.

Hsin-Lien Precision CO.,LTD. TEL:886-5-5961878 886-5-55961893 FAX:886-5-5961855			
Title	11825		
Customer		ﾖﾖ ｺ APPROVED	
Date	93.12.02		
Unit	mm	ｼf ﾖﾖ AUDITED	
Scale	1:1		
Rev No.	1/1	ｳ] ｺp DESIGNED	
File No.	11825		

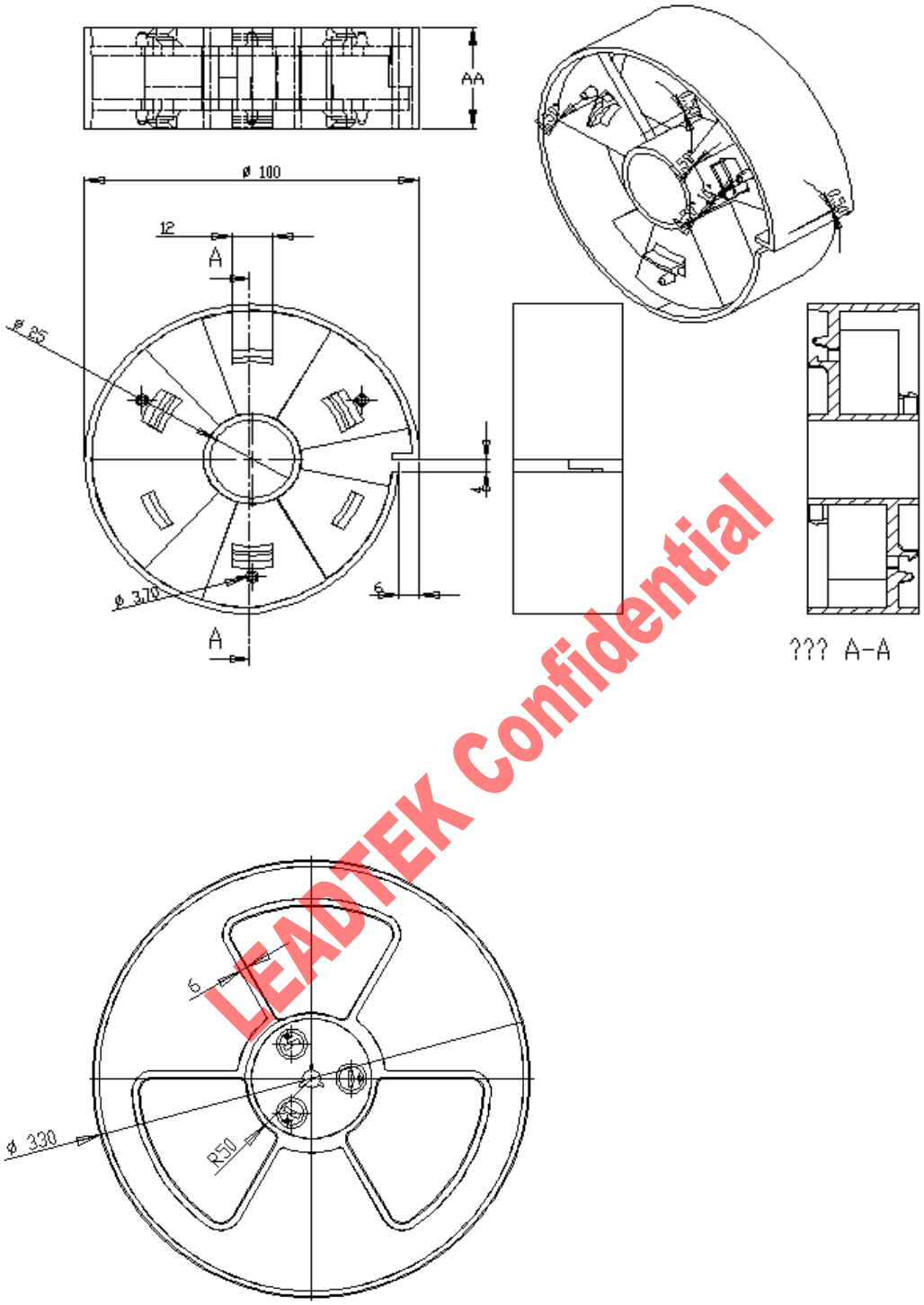
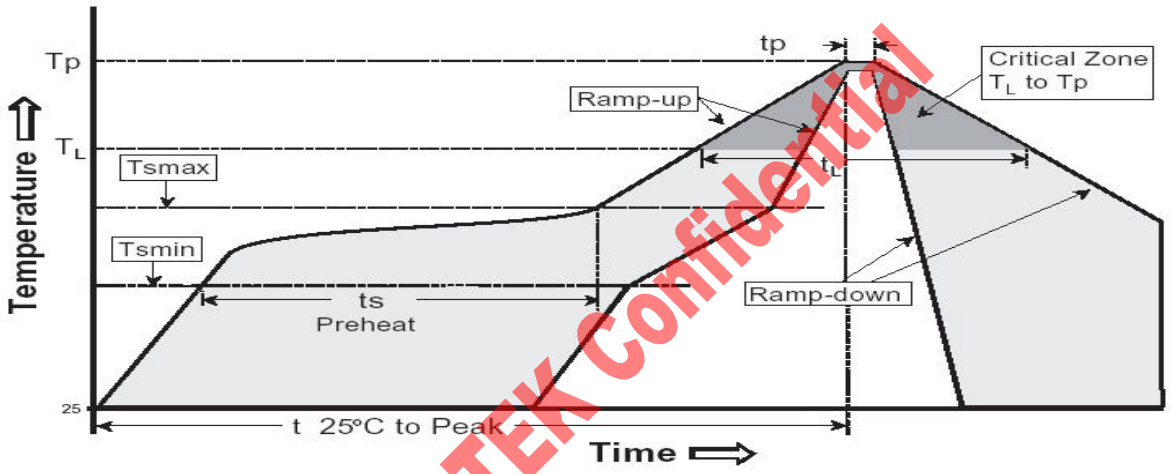


Figure 2: Reel dimensions

6 RoHS Soldering Profile

6.1 Reflow Profile

High quality, low defect soldering requires identifying the optimum temperature profile for reflowing the solder paste. To have the correct profile assures components, boards, and solder joints are not damaged and reliable solder connection is achievable. Profiles are essential for establishing and maintaining processes. You must be able to repeat the profile to achieve process consistency. The heating and cooling rise rates must be compatible with the solder paste and components. The amount of time that the assembly is exposed to certain temperatures must first be defined and then maintained.



Average ramp-up rate	**3℃/second max.**
Preheat (Tsmax – Tsmin, ts)	**150~200℃ ; 60~180seconds**
Time maintained above (TL, tL)	**217℃ ; 60~150seconds**
Peak Temperature (Tp)	**255~260℃ ; 10~20seconds**
Ramp-down rate	**6℃/second max.**
Time 25℃ to Peak Temperature	**8 minutes max.**
Maximum number of reflow cycles	**≤3**

6.2 Storage and Baking Condition

1. Calculated shelf life in sealed bag: 6 months at <40℃ and <90% relative humidity(RH).
2. After bag is opened, devices that will be subjected to reflow soldering or other high temperature process must be :
   2-1. Mounted within: 24 hours of factory conditions ≤30℃ /60% RH, or
   2-2. Stored at <10% RH under the protection against humidity and static electricity
3. Devices require bake before mounting, if :
   3-1. Humidity indicator Card is >60% when read at 23±5℃.
   3-2. 2-1 or 2-2 not met.
4. If baking is required, devices may be baked for 24 hours at 125±5℃.

Note:
if device containers cannot be subjected to high temperature or if shorter bake times are desired, reference IPC/JEDEC J-STD-020 for bake procedure

7 Appendix

N/A