ShinDengen

P100FP12SNK

Power MOSFETs
120V, 100A, N-channel

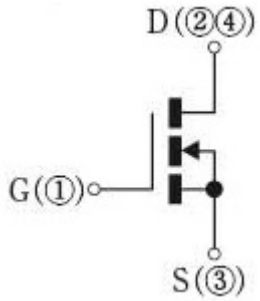
Feature

- N-channel
- SMD
- Large Current
- Low Ron
- 10V Gate Drive
- Low Capacitance
- Available for automotive use
- Pb free terminal
- RoHS:Yes

OUTLINE

Package (House Name): FP
Package (JEITA Code): SC-83 similar

Equivalent circuit



Absolute Maximum Ratings (unless otherwise specified : Tc=25℃)

Item	Symbol	Conditions	Ratings	Unit
Storage temperrature	Tstg		-55 to 175	℃
Channel tempertature	Tch		175	℃
Drain-source voltage	V_{DSS}		120	V
Gate-source voltage	V_{GSS}		±20	V
Continuous drain current(DC)	I_D		100	A
Continuous drain current(Peak)	I_{DP}	Pulse width 10μs, duty=1/100	400	A
Total power dissipation	P_T		238	W
Single avalanche current	I_{AS}	Starting Tch=25℃ Tch≦150℃	57	A
Single avalanche energy	E_{AS}	Starting Tch=25℃ Tch≦150℃	373	mJ

※ :See the original Specifications

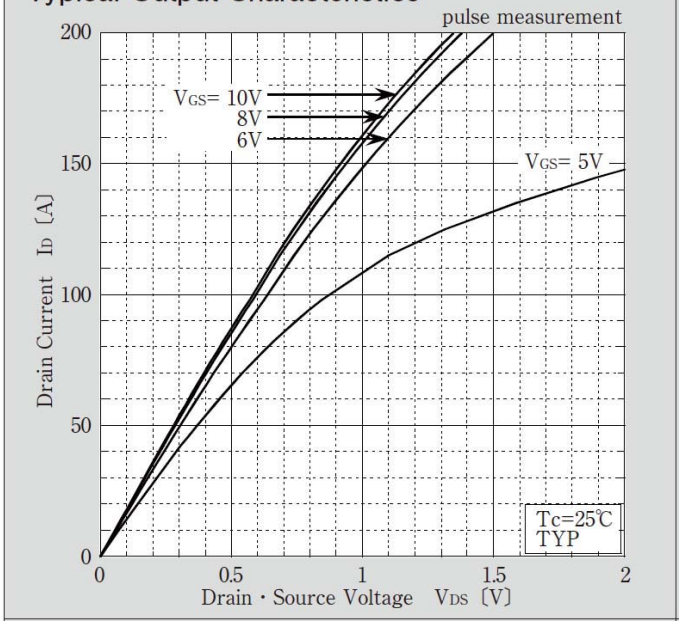
Electrical Characteristics (unless otherwise specified : Tc=25℃)

Item	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Drain-Source breakdown voltage	$V_{(BR)DSS}$	ID=1mA, VGS=0V	120			V
Zero gate voltage drain current	I_{DSS}	VDS=120V, VGS=0V			1	μA
Gate-source leakage current	I_{GSS}	VGS=±20V, VDS=0V			±0.1	μA
Forward transconductance	g_{fs}	ID=50A, VDS=10V	35			S
Static drain-source on-state resistance	$R_{DS(ON)}$	ID=50A, VGS=10V		0.0056	0.007	Ω
Gate threshold voltage	Vth	ID=1mA, VDS=10V	2	3	4	V
Source-drain diode forward voltage	V_{SD}	IS=100A, VGS=0V			1.5	V
Thermal resistance	Rth(j-c)	Junction to case			0.63	℃/W
Total gate charge	Qg	VDD=96V, VGS=10V, ID=100A		164		nC
Gate to source charge	Qgs	VDD=96V, VGS=10V, ID=100A		47		nC
Gate to drain charge	Qgd	VDD=96V, VGS=10V, ID=100A		63		nC
Input capacitance	Ciss	VDS=25V, VGS=0V, f=1MHz		9600		pF
Reverce transfer capacitnce	Crss	VDS=25V, VGS=0V, f=1MHz		320		pF
Output capacitance	Coss	VDS=25V, VGS=0V, f=1MHz		730		pF
Turn-on delay time	td(on)	ID=50A, RL=1.2Ω, VDD=60V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		13		ns
Rise time	tr	ID=50A, RL=1.2Ω, VDD=60V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		34		ns
Turn-off delay time	td(off)	ID=50A, RL=1.2Ω, VDD=60V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		115		ns
Fall time	tf	ID=50A, RL=1.2Ω, VDD=60V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		53		ns
Diode reverse recovery time	trr	IF=100A, VGS=0V, di/dt=100A/μs		75		ns
Diode reverse recovery charge	Qrr	IF=100A, VGS=0V, di/dt=100A/μs		214		nC

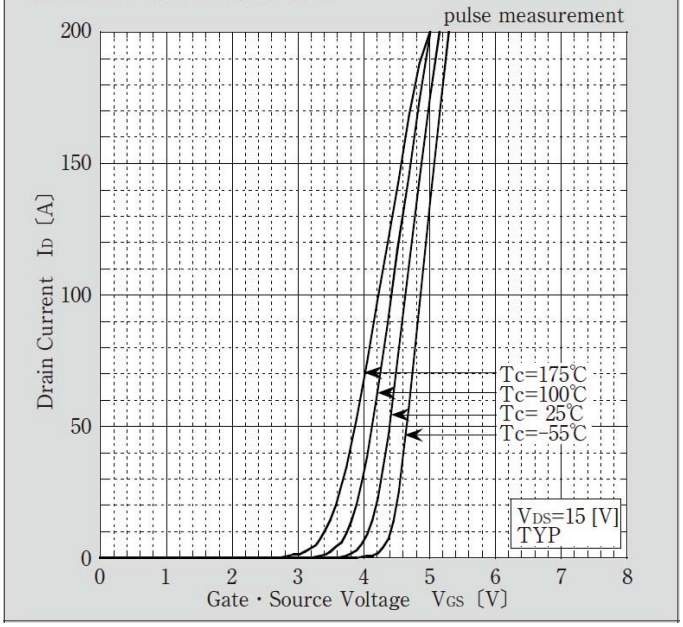
※ ：See the original Specifications

CHARACTERISTIC DIAGRAMS

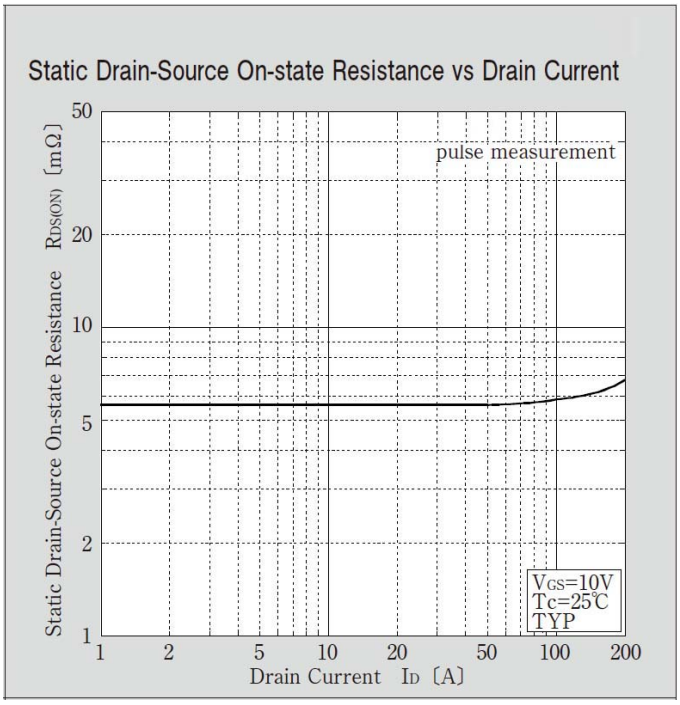
Typical Output Characteristics



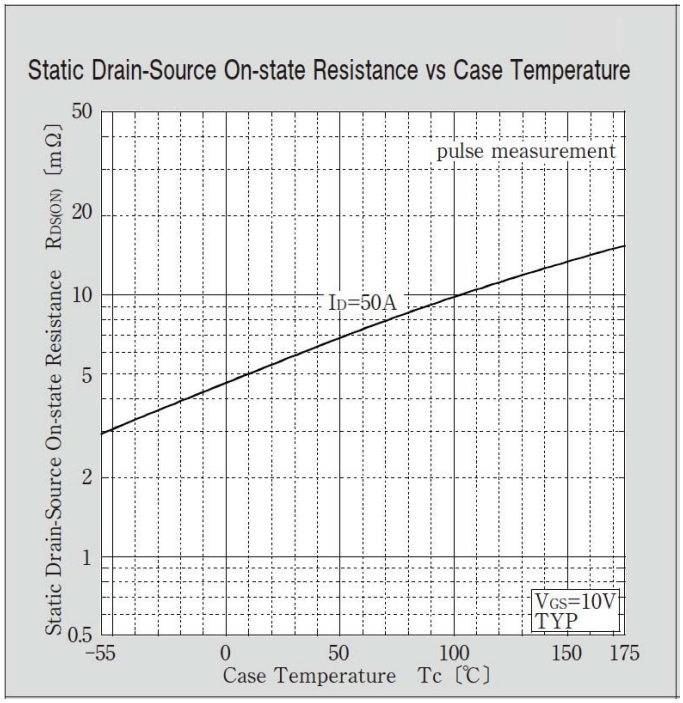
Transfer Characteristics



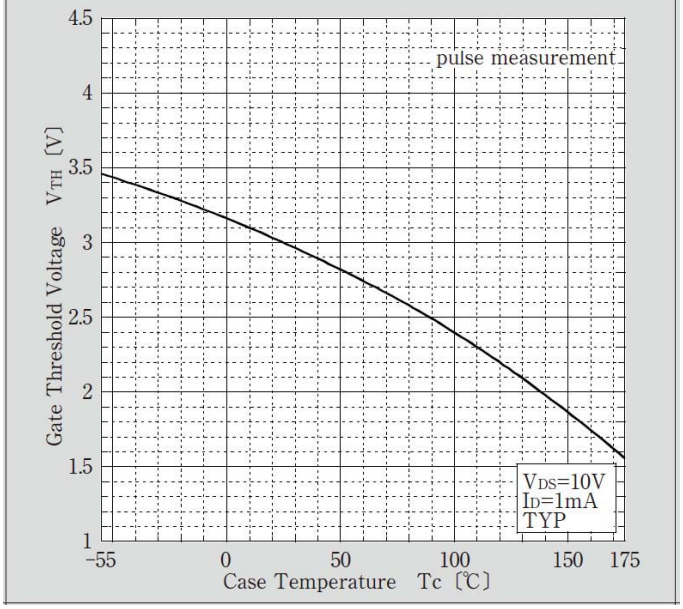
Static Drain-Source On-state Resistance vs Drain Current



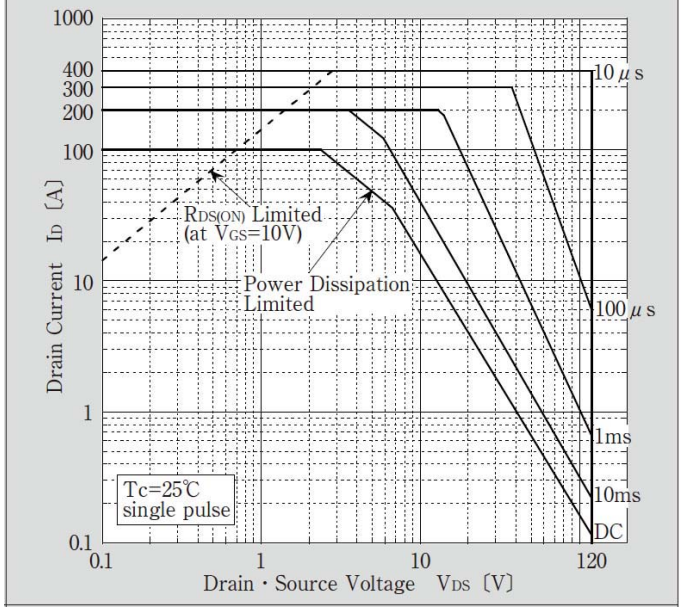
Static Drain-Source On-state Resistance vs Case Temperature



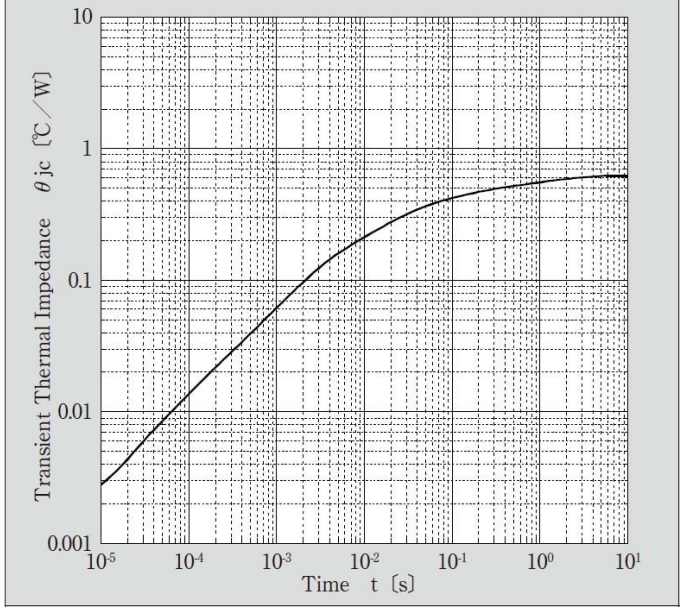
Gate Threshold Voltage vs Case Temperature



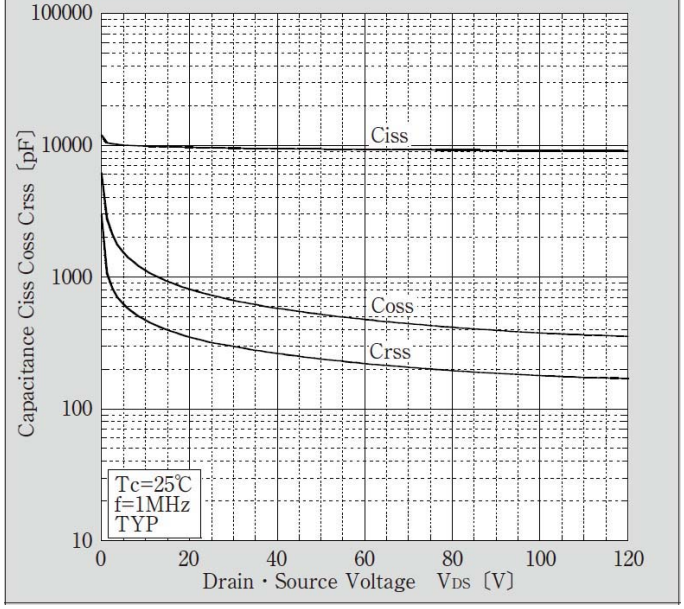
Safe Operating Area



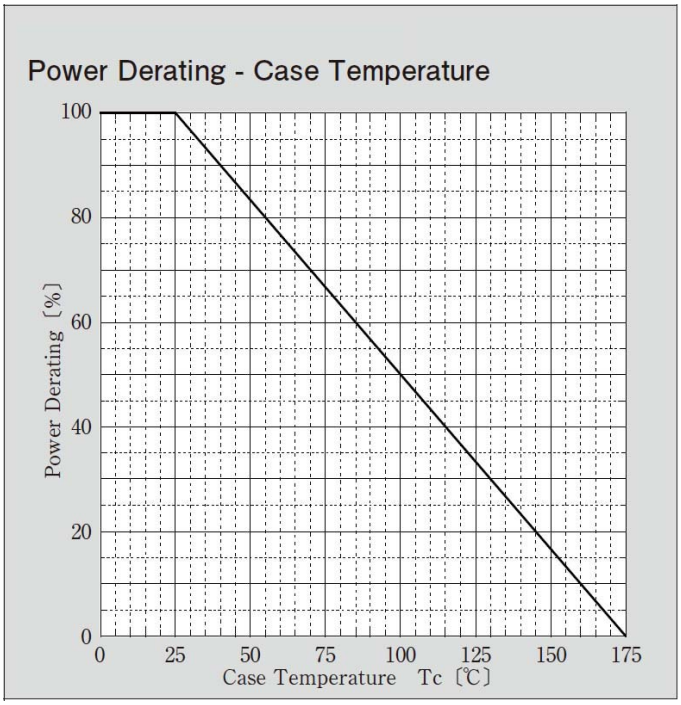
Transient Thermal Impedance



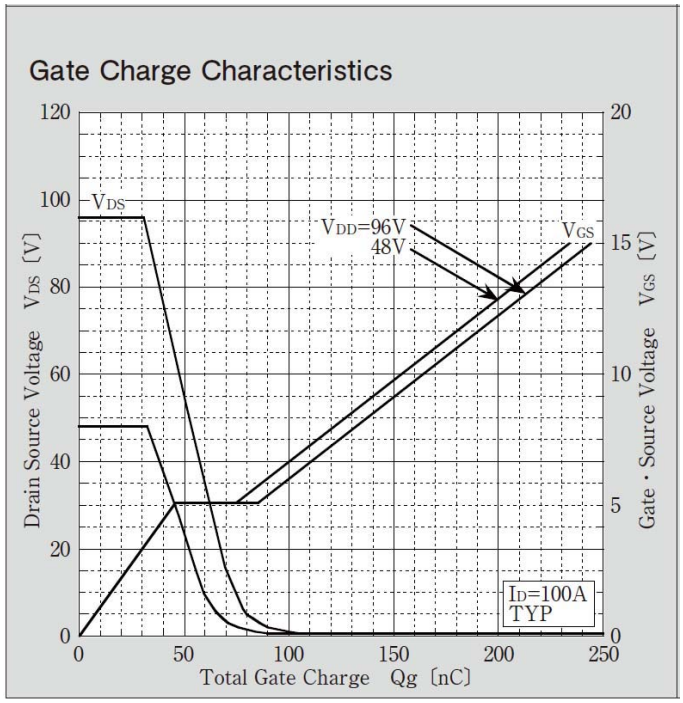
Capacitance Characteristics



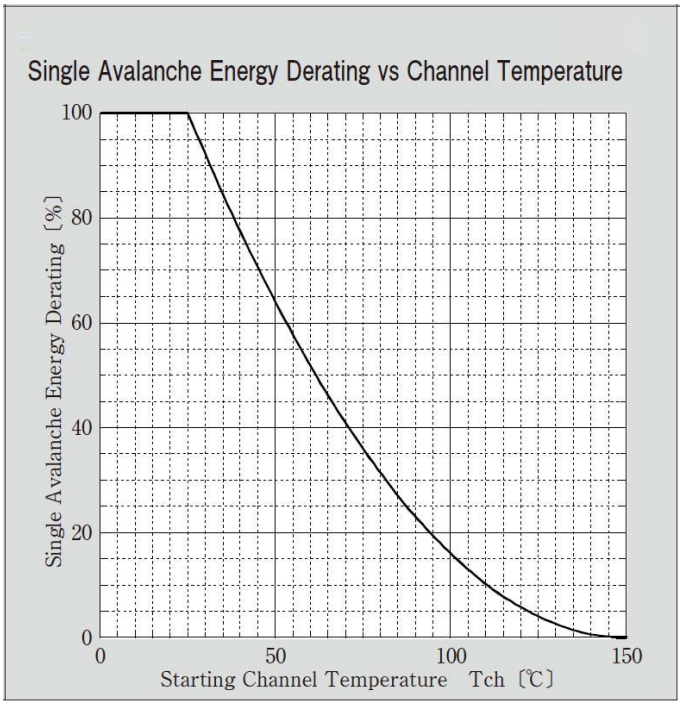
Power Derating - Case Temperature



Gate Charge Characteristics



Single Avalanche Energy Derating vs Channel Temperature



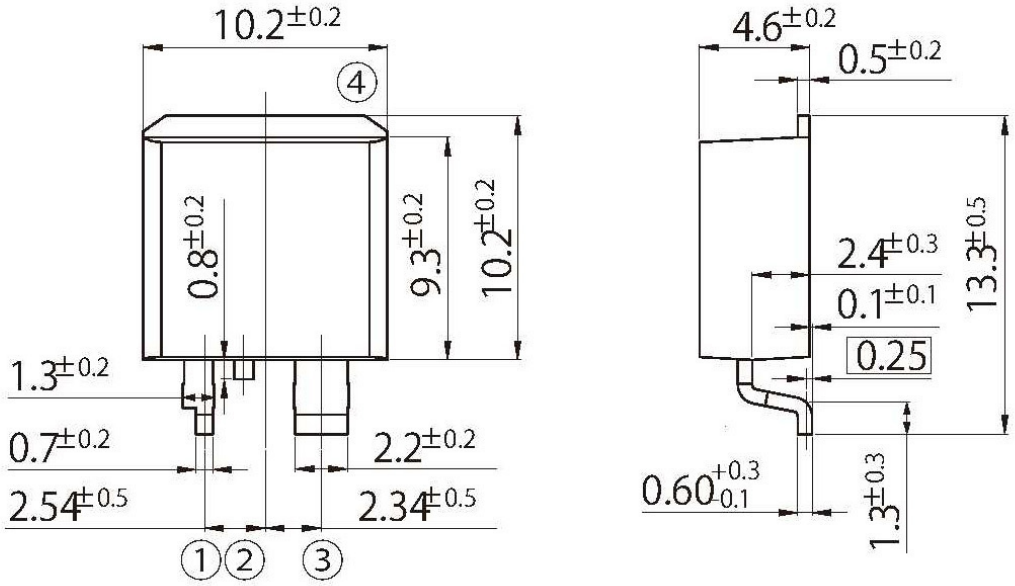
Outline Dimensions

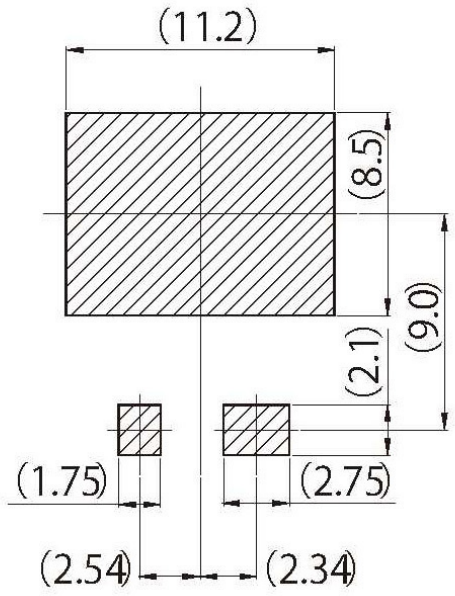
unit:mm

scale: 3/1

H5

JEDEC Code	–
JEITA Code	SC-83 similar
House Name	FP





・Optimize soldering pad to the board design and soldering condition.

Notes

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