

# P1B52HP2

## Power MOSFETs

525V, 1A, N-channel

### Feature

- N-channel
- SMD
- High Voltage
- Low Capacitance
- High Avalanche Durability, High di/dt Durability
- Pb free terminal
- RoHS:Yes

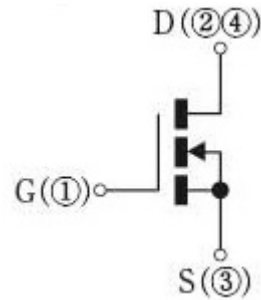
### OUTLINE

Package (House Name): FB

Package (JEDEC Code): TO-252AA



### Equivalent circuit



### Absolute Maximum Ratings (unless otherwise specified : Tc=25°C)

Item	Symbol	Conditions	Ratings	Unit
Storage temperature	T <sub>stg</sub>		-55 to 150	°C
Channel temperature	T <sub>ch</sub>		150	°C
Drain-source voltage	V <sub>DSS</sub>		525	V
Gate-source voltage	V <sub>GSS</sub>		±30	V
Continuous drain current(DC)	I <sub>D</sub>		1	A
Continuous drain current(Peak)	I <sub>DP</sub>	Pulse width 10μs, duty=1/100	4	A
Continuous source current(DC)	I <sub>S</sub>		1	A
Total power dissipation	P <sub>T</sub>		35	W
Repetitive avalanche current	I <sub>AR</sub>	Starting T <sub>ch</sub> =25°C T <sub>ch</sub> ≤150°C	1	A
Single avalanche energy	E <sub>AS</sub>	Starting T <sub>ch</sub> =25°C T <sub>ch</sub> ≤150°C	10	mJ
Repetitive avalanche energy	E <sub>AR</sub>	Starting T <sub>ch</sub> =25°C T <sub>ch</sub> ≤150°C	1	mJ
Drain-source diode di/dt strength	di/dt	I <sub>S</sub> =1A, T <sub>c</sub> =25°C	350	A/μs

\* :See the original Specifications

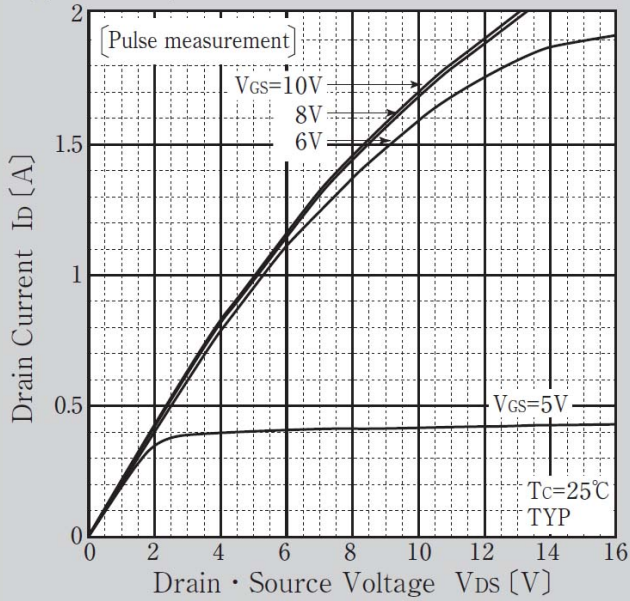
**Electrical Characteristics** (unless otherwise specified : Tc=25°C)

Item	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Drain-Source breakdown voltage	$V_{(BR)DSS}$	ID=1mA, VGS=0V	525			V
Zero gate voltage drain current	$I_{DSS}$	VDS=525V, VGS=0V			100	μA
Gate-source leakage current	$I_{GSS}$	VGS=±25V, VDS=0V			±10	μA
Forward transconductance	$g_{fs}$	ID=0.5A, VDS=10V	0.4	1		S
Static drain-source on-state resistance	$R_{DS(ON)}$	ID=0.5A, VGS=10V		6	7.2	Ω
Gate threshold voltage	$V_{th}$	ID=1mA, VDS=10V	3	3.75	4.5	V
Source-drain diode forward voltage	$V_{SD}$	IS=0.5A, VGS=0V			1.5	V
Thermal resistance	$R_{th(j-c)}$	Junction to case			3.55	°C/W
Total gate charge	$Q_g$	VDD=400V, VGS=10V, ID=1A		4.3		nC
Input capacitance	$C_{iss}$	VDS=50V, VGS=0V, f=1MHz		125		pF
Reverse transfer capacitance	$C_{rss}$	VDS=50V, VGS=0V, f=1MHz		3.5		pF
Output capacitance	$C_{oss}$	VDS=50V, VGS=0V, f=1MHz		20		pF
Turn-on delay time	$t_{d(on)}$	ID=0.5A, RL=300Ω, VDD=150V, Rg=50Ω, VGS(+)=10V, VGS(-)=0V		9		ns
Rise time	$t_r$	ID=0.5A, RL=300Ω, VDD=150V, Rg=50Ω, VGS(+)=10V, VGS(-)=0V		7		ns
Turn-off delay time	$t_{d(off)}$	ID=0.5A, RL=300Ω, VDD=150V, Rg=50Ω, VGS(+)=10V, VGS(-)=0V		28		ns
Fall time	$t_f$	ID=0.5A, RL=300Ω, VDD=150V, Rg=50Ω, VGS(+)=10V, VGS(-)=0V		18		ns

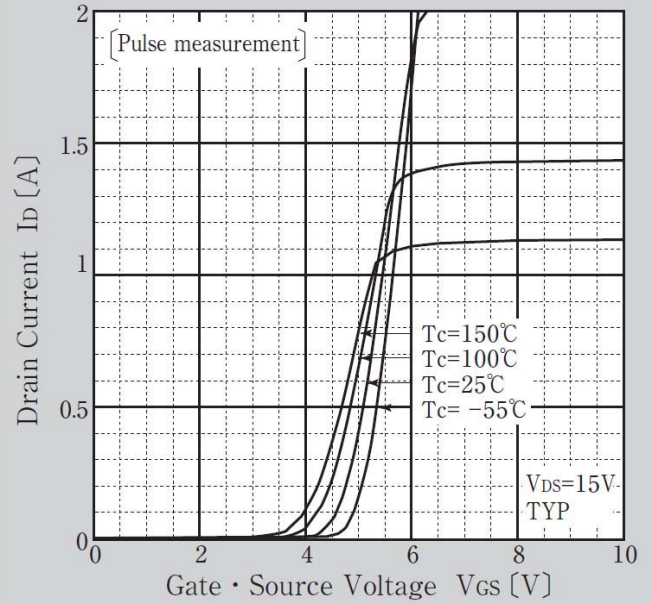
\* : See the original Specifications

# CHARACTERISTIC DIAGRAMS

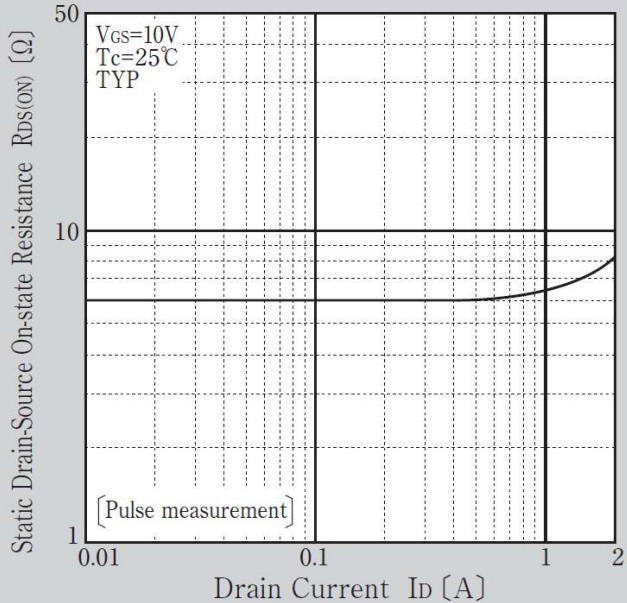
### Typical Output Characteristics



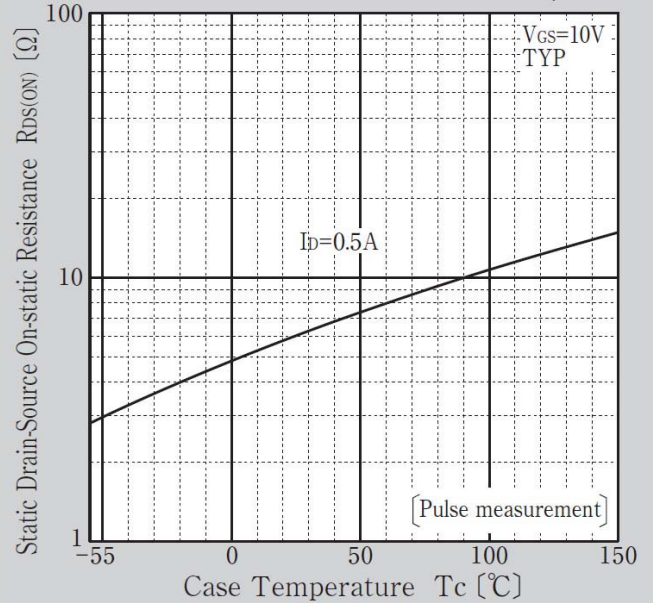
### Transfer Characteristics



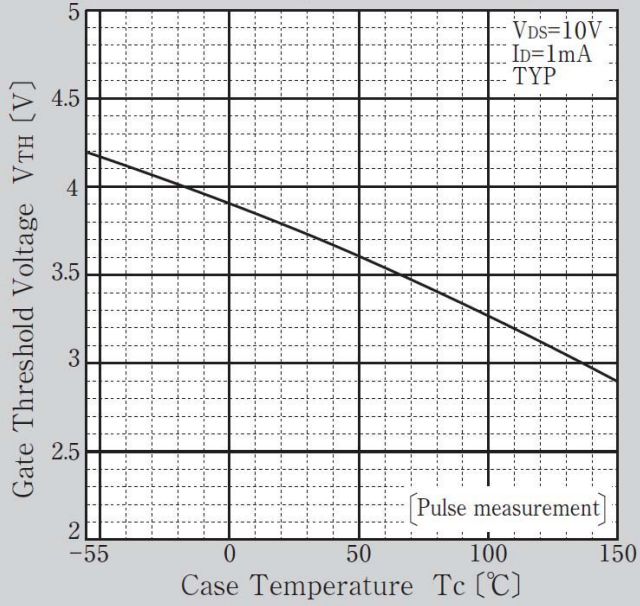
### Static Drain-Source On-state Resistance vs Drain Current



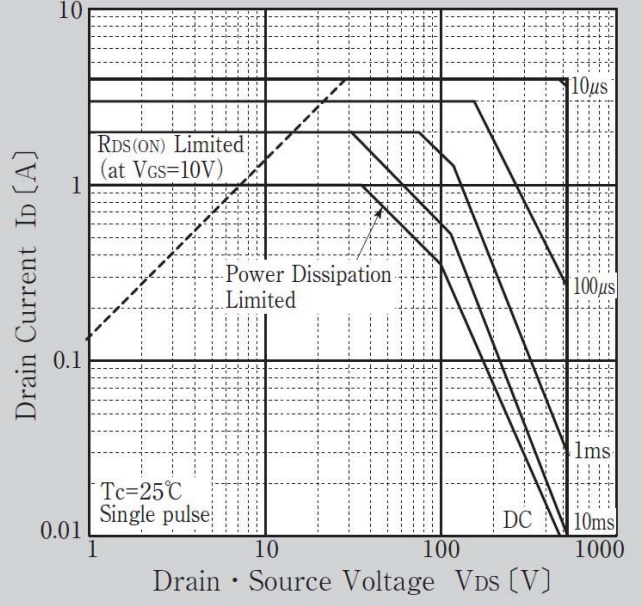
### Static Drain-Source On-state Resistance vs Case Temperature



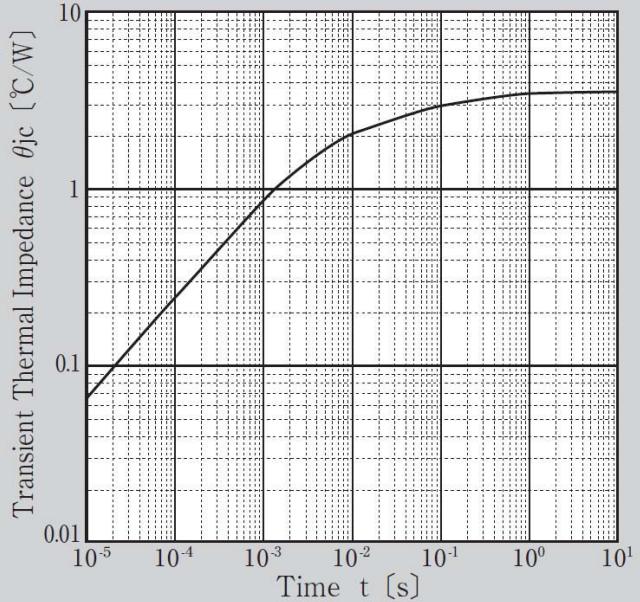
Gate Threshold Voltage vs Case Temperature



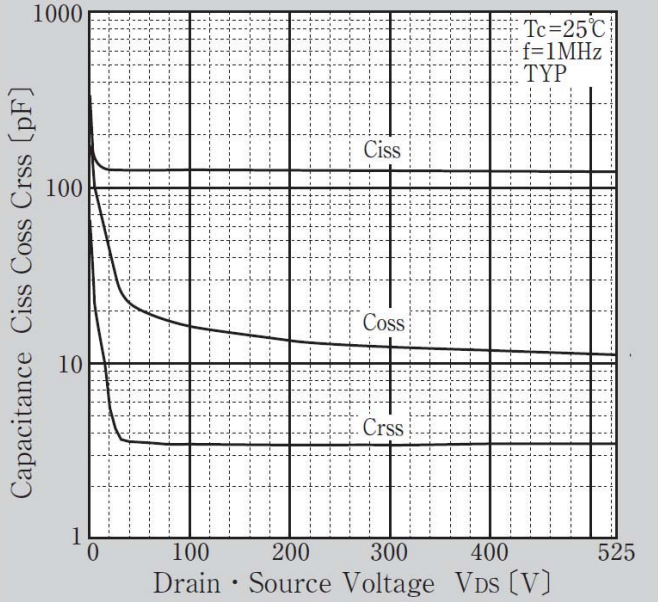
Safe Operating Area

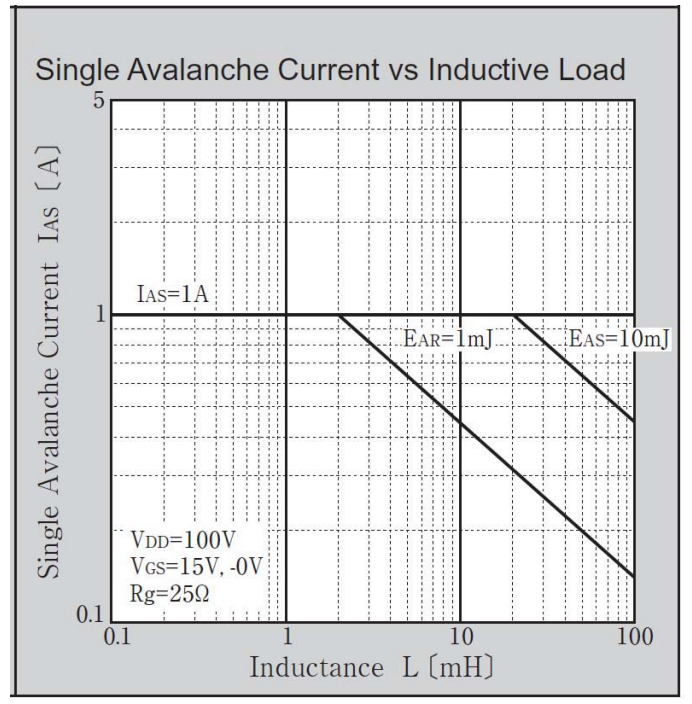
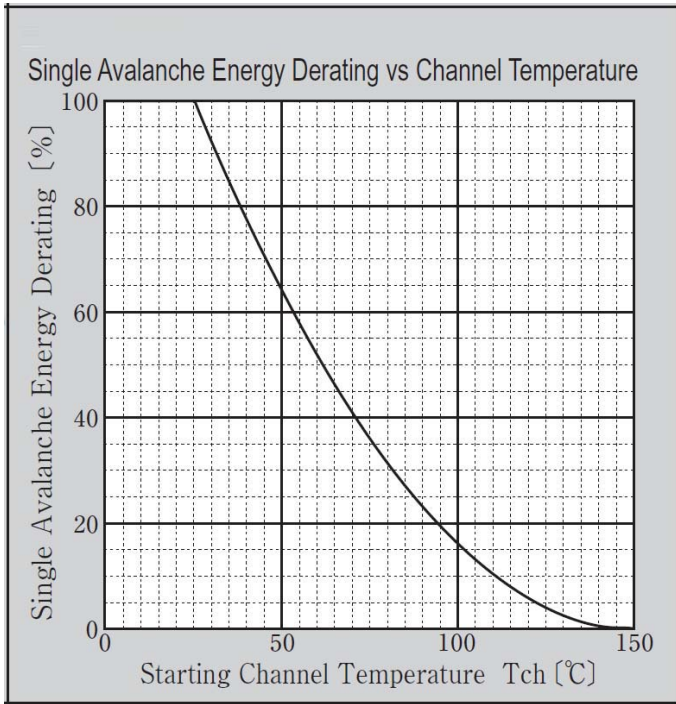
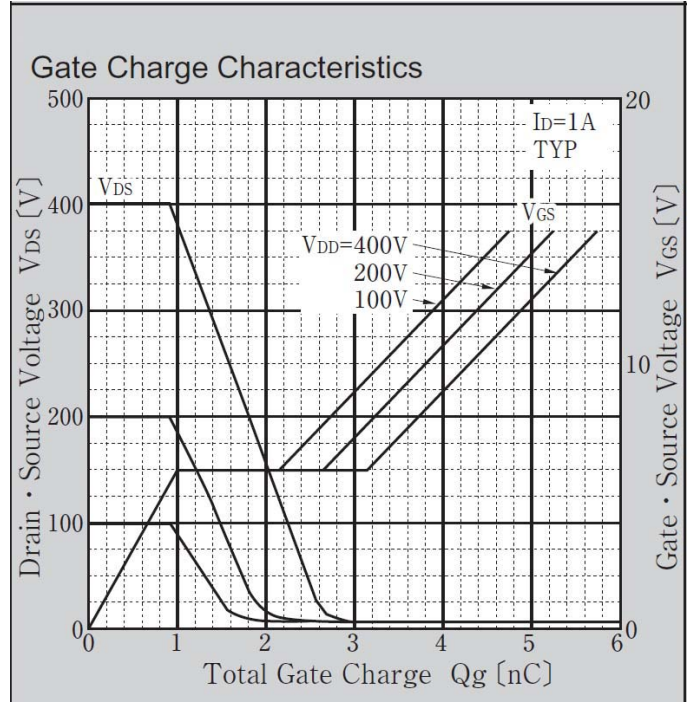
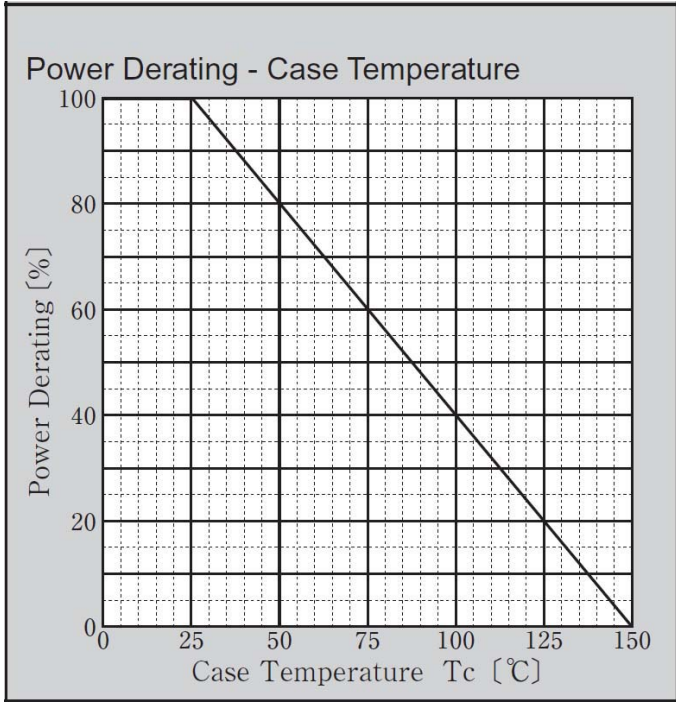


Transient Thermal Impedance



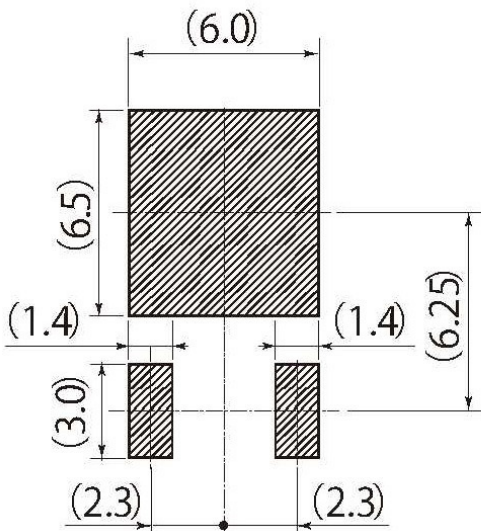
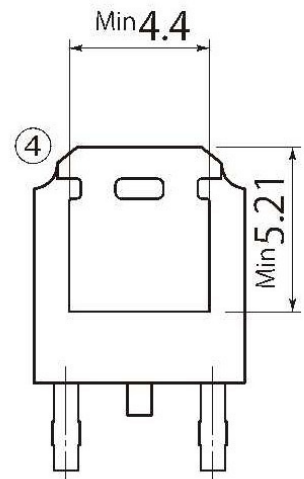
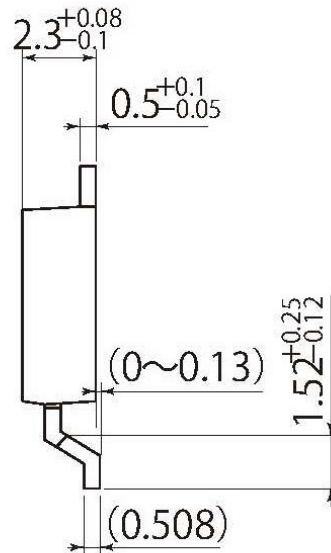
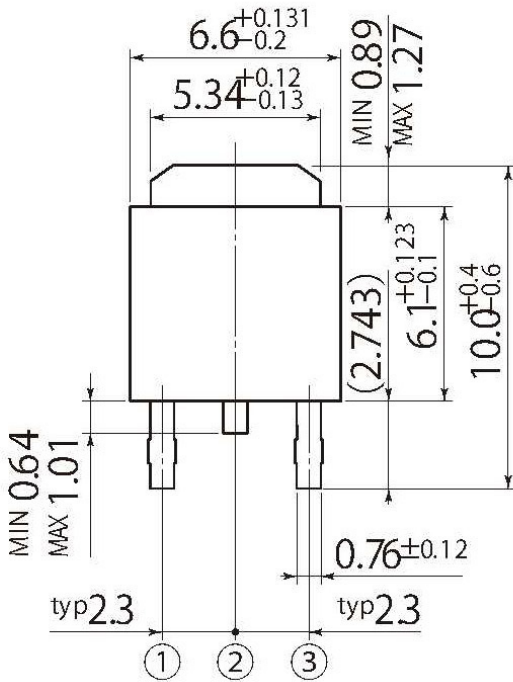
Capacitance Characteristics





G2

JEDEC Code	TO-252AA
JEITA Code	-
House Name	FB



Referential Soldering Pad

• Optimize soldering pad to the board design and soldering condition.

## Notes

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