

P26FE10SLK

Power MOSFETs

100V, 26A, N-channel

Feature

- N-channel
- SMD
- Low Ron
- 4.5V Gate Drive
- Low Capacitance
- Based on AEC-Q101
- Pb free terminal
- RoHS:Yes

OUTLINE

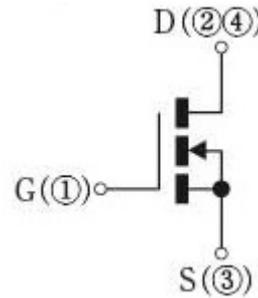
Package (House Name): FE

Package (JEDEC Code): TO-252AB similar

Package (JEITA Code): SC-63



Equivalent circuit



Absolute Maximum Ratings (unless otherwise specified : Tc=25°C)

Item	Symbol	Conditions	Ratings	Unit
Storage temperature	T _{stg}		-55 to 175	°C
Channel temperature	T _{ch}		-55 to 175	°C
Drain-source voltage	V _{DSS}		100	V
Gate-source voltage	V _{GSS}		±20	V
Continuous drain current(DC)	I _D		26	A
Continuous drain current(Peak)	I _{DP}	Pulse width 10μs, duty=1/100	78	A
Total power dissipation	P _T		44	W
Single avalanche current	I _{AS}	Starting T _{ch} =25°C T _{ch} ≤150°C	19	A
Single avalanche energy	E _{AS}	Starting T _{ch} =25°C T _{ch} ≤150°C	18	mJ

* : See the original Specifications

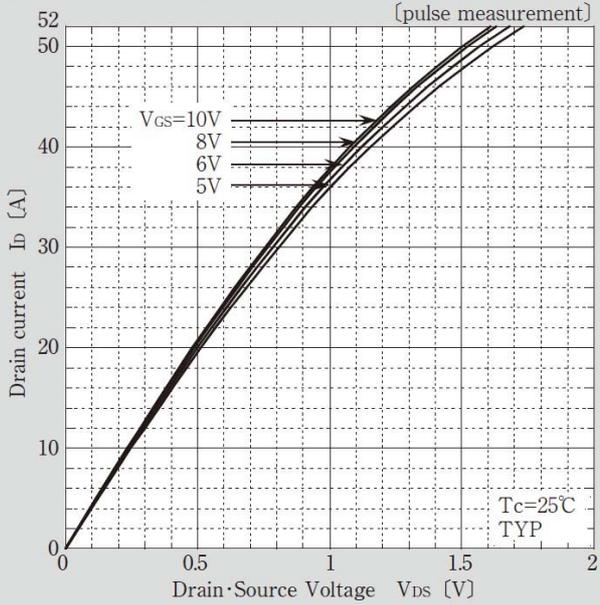
Electrical Characteristics (unless otherwise specified : Tc=25°C)

Item	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Drain-Source breakdown voltage	$V_{(BR)DSS}$	ID=1mA, VGS=0V	100			V
Zero gate voltage drain current	I_{DSS}	VDS=100V, VGS=0V			1	μA
Gate-source leakage current	I_{GSS}	VGS=±20V, VDS=0V			±0.1	μA
Forward transconductance	g_{fs}	ID=13A, VDS=10V	10			S
Static drain-source on-state resistance	$R_{DS(ON)}$	ID=13A, VGS=10V		0.024	0.03	Ω
Static drain-source on-state resistance	$R_{DS(ON)}$	ID=13A, VGS=4.5V		0.026	0.035	Ω
Gate threshold voltage	V_{th}	ID=1mA, VDS=10V	1.5	2	2.5	V
Source-drain diode forward voltage	V_{SD}	IS=26A, VGS=0V			1.5	V
Thermal resistance	$R_{th(j-c)}$	Junction to case, with heatsink ※			3.4	°C/W
Total gate charge	Q_g	VDD=80V, VGS=10V, ID=26A		43		nC
Gate to source charge	Q_{gs}	VDD=80V, VGS=10V, ID=26A		9		nC
Gate to drain charge	Q_{gd}	VDD=80V, VGS=10V, ID=26A		12		nC
Input capacitance	C_{iss}	VDS=25V, VGS=0V, f=1MHz		1975		pF
Reverse transfer capacitance	C_{rss}	VDS=25V, VGS=0V, f=1MHz		76		pF
Output capacitance	C_{oss}	VDS=25V, VGS=0V, f=1MHz		158		pF
Turn-on delay time	$t_{d(on)}$	ID=13A, RL=3.85Ω, VDD=50V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		6		ns
Rise time	t_r	ID=13A, RL=3.85Ω, VDD=50V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		10		ns
Turn-off delay time	$t_{d(off)}$	ID=13A, RL=3.85Ω, VDD=50V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		30		ns
Fall time	t_f	ID=13A, RL=3.85Ω, VDD=50V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		17		ns
Diode reverse recovery time	t_{rr}	IF=26A, VGS=0V, di/dt=100A/μs		53		ns
Diode reverse recovery charge	Q_{rr}	IF=26A, VGS=0V, di/dt=100A/μs		100		nC

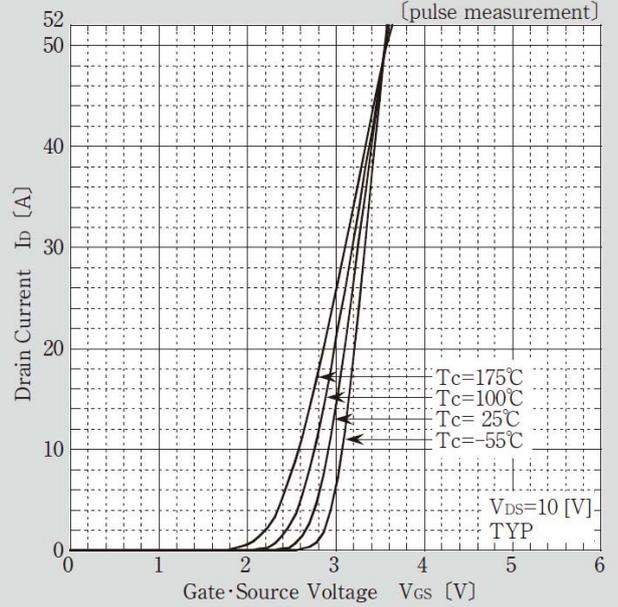
※ : See the original Specifications

CHARACTERISTIC DIAGRAMS

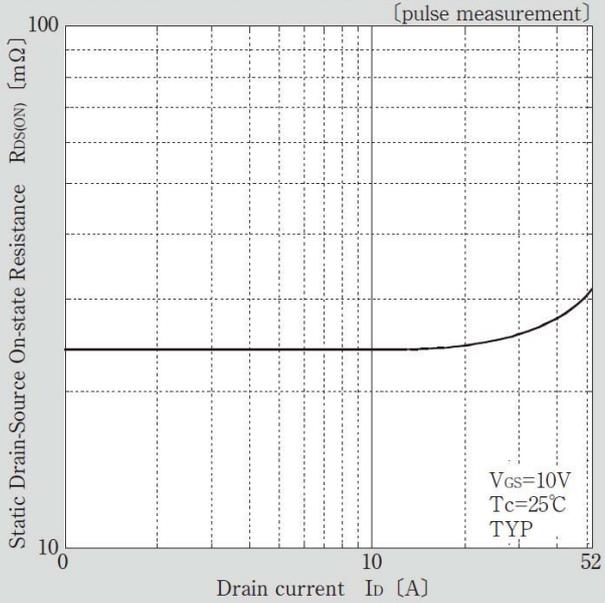
Typical Output Characteristics



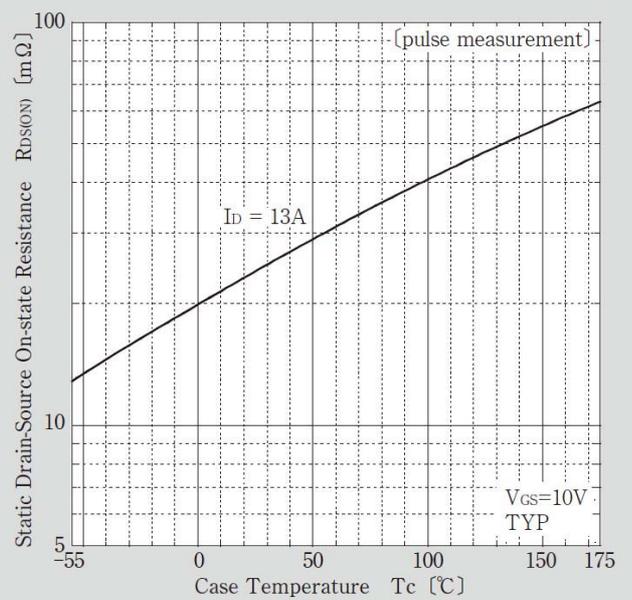
Transfer Characteristics



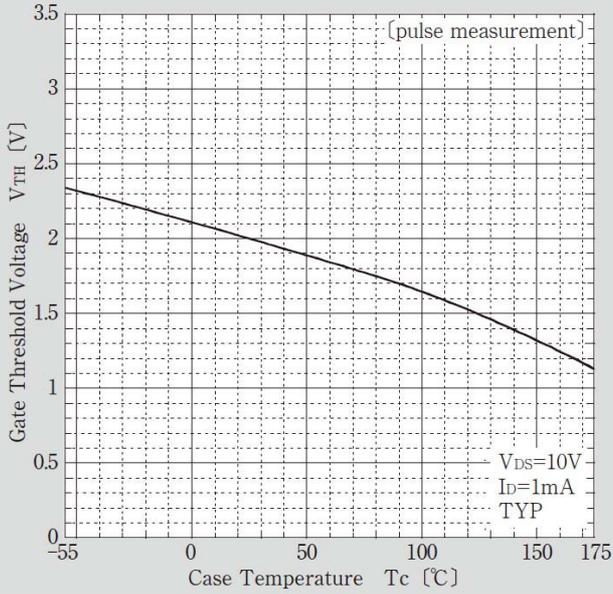
Static Drain-Source On-state Resistance vs Drain Current



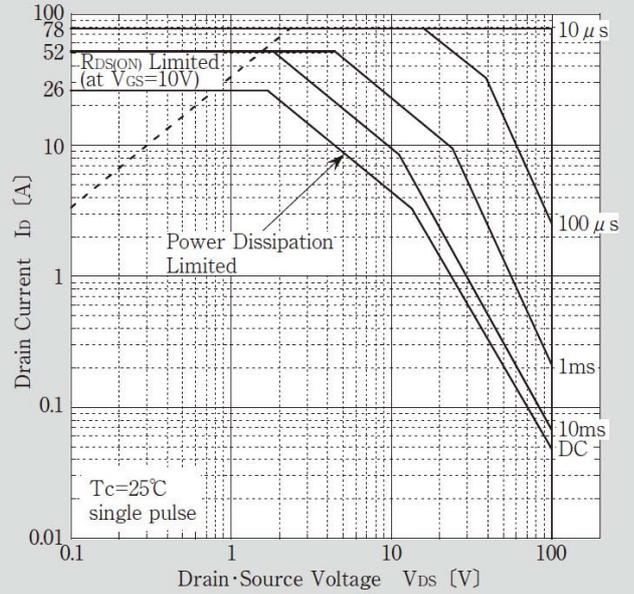
Static Drain-Source On-state Resistance vs Case Temperature



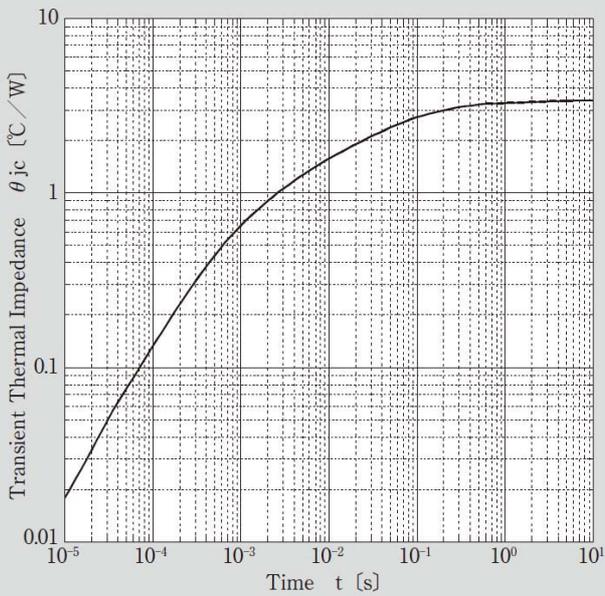
Gate Threshold Voltage vs Case Temperature



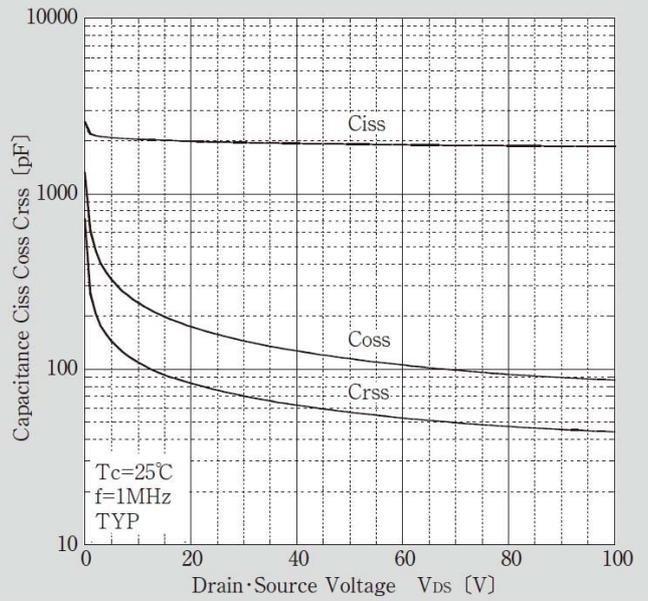
Safe Operating Area



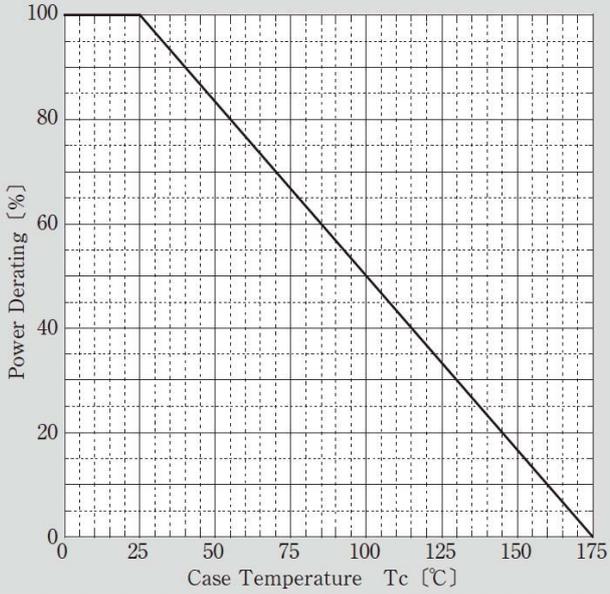
Transient Thermal Impedance



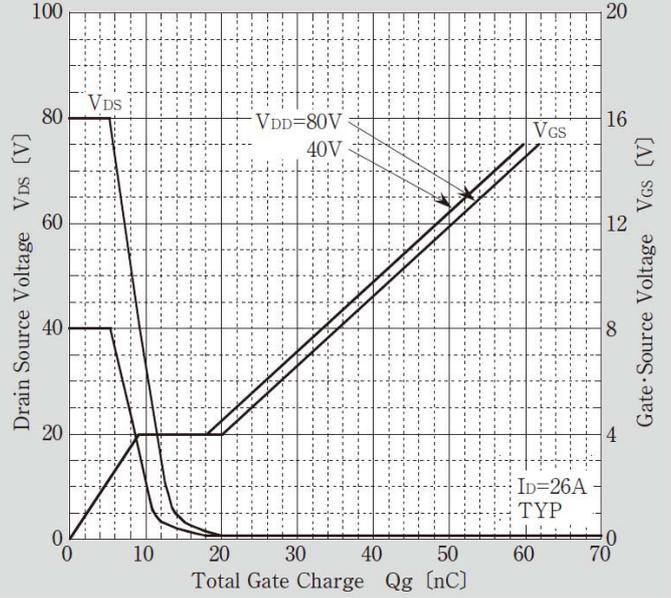
Capacitance Characteristics



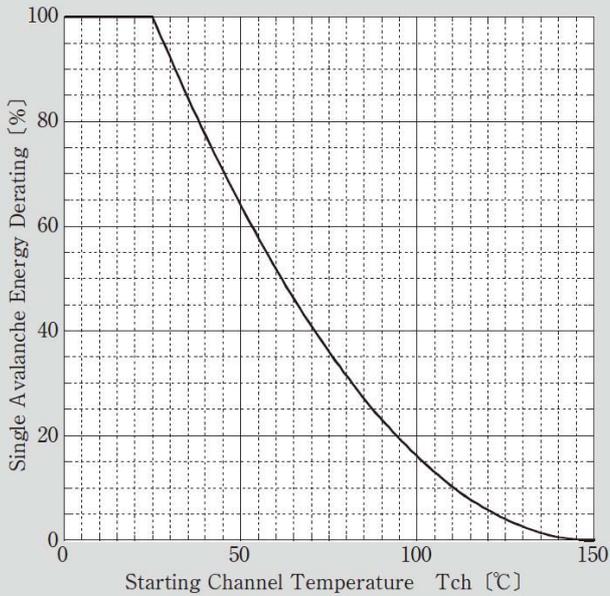
Power Derating - Case Temperature



Gate Charge Characteristics

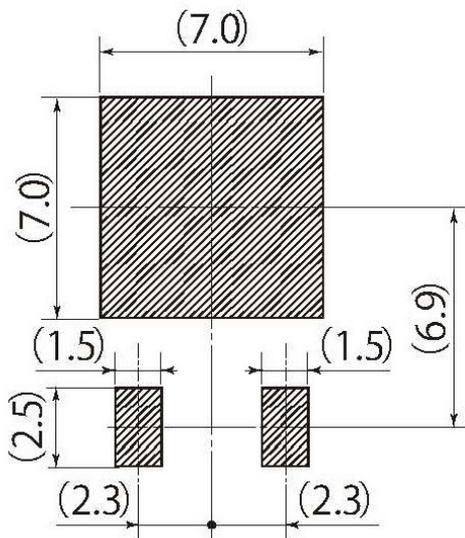
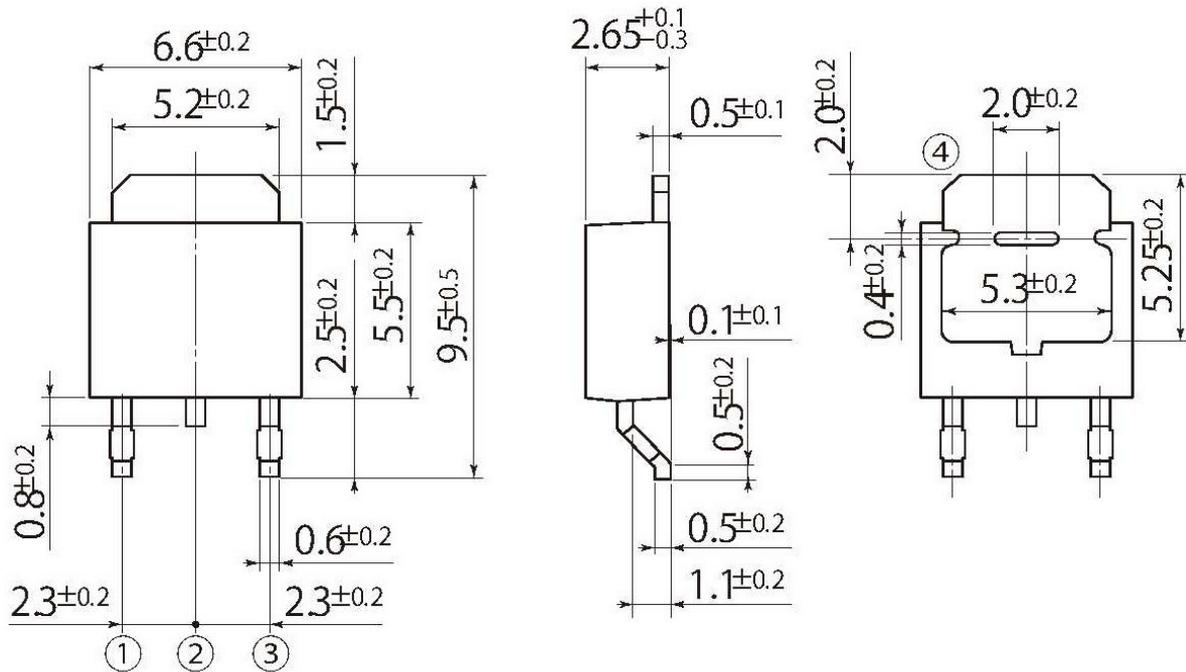


Single Avalanche Energy Derating vs Channel Temperature



G3

JEDEC Code	TO-252AB similar
JEITA Code	SC-63
House Name	FE



Referential Soldering Pad

• Optimize soldering pad to the board design and soldering condition.

Notes

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