

# FML60N150S2FDHF

## Super J MOS<sup>®</sup> S2 series

## N-Channel enhancement mode power MOSFET

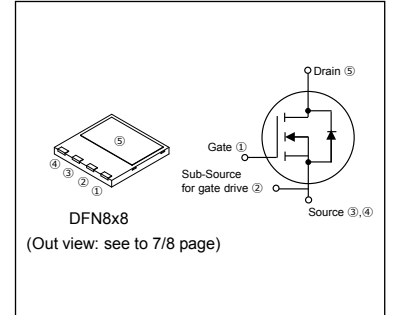
### Features

- Pb-free lead terminal
- RoHS compliant
- Halogen-free molding compound
- MSL:1, Reflow available

### Applications

- For switching

### Package and Internal circuit chart



### Absolute Maximum Ratings at $T_c=25^\circ\text{C}$ (unless otherwise specified)

Parameter	Symbol	Characteristics	Unit	Remarks
Drain-Source Voltage	$V_{DS}$	600	V	
	$V_{DSX}$	600	V	$V_{GS} = -30\text{ V}$
Continuous Drain Current	$I_D$	28.7	A	$T_c=25^\circ\text{C}$ Note*1,2
		18.2	A	$T_c=100^\circ\text{C}$ Note*1,2
Pulsed Drain Current	$I_{DP}$	83.6	A	Note *2
Gate-Source Voltage	$V_{GS}$	$\pm 30$	V	
Non-Repetitive Maximum Avalanche Current	$I_{AS}$	3.5	A	Note *3
Non-Repetitive Maximum Avalanche Energy	$E_{AS}$	517.5	mJ	Note *4
Maximum MOSFET $dv/dt$	$dv_{DS}/dt$	50	V/ns	$V_{GS} \leq 600\text{ V}$
Continuous Diode Forward Current	$I_{DR}$	28.7	A	$T_c=25^\circ\text{C}$ Note*1,2
		18.2	A	$T_c=100^\circ\text{C}$ Note*1,2
Pulsed Diode Forward Current	$I_{DRP}$	83.6	A	Note *2
Peak Diode Recovery $dv/dt$	$dv/dt$	30	V/ns	Note *5
Peak Diode Recovery $-di_{DR}/dt$	$-di_{DR}/dt$	100	A/ $\mu\text{s}$	Note *6
Maximum Power Dissipation	$P_{tot}$	159	W	$T_c=25^\circ\text{C}$
		2.78	W	$T_a=25^\circ\text{C}$
Operating Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$	
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$	

Note \*1 : Maximum duty cycle  $D=0.55$

Note \*2 : Limited by maximum channel temperature.

Note \*3 :  $T_{ch} \leq 150^\circ\text{C}$ , See Figure 1 and 2.

Note \*4 : Starting  $T_{ch} = 25^\circ\text{C}$ ,  $I_{AS} = 2.1\text{ A}$ ,  $L = 215\text{ mH}$ ,  $V_{DD} = 60\text{ V}$ ,  $R_G = 50\ \Omega$ . See Figure 1 and 2.

$E_{AS}$  limited by maximum channel temperature and avalanche current.

Note \*5 :  $I_{DR} \leq 22.7\text{ A}$ ,  $-di_{DR}/dt \leq 100\text{ A}/\mu\text{s}$ ,  $V_{DS\text{ peak}} \leq 600\text{ V}$ ,  $T_{ch} \leq 150^\circ\text{C}$ .

Note \*6 :  $I_{DR} \leq 22.7\text{ A}$ ,  $dv/dt \leq 30\text{ V/ns}$ ,  $V_{DS\text{ peak}} \leq 600\text{ V}$ ,  $T_{ch} \leq 150^\circ\text{C}$ .

**Electrical Characteristics at  $T_c=25^\circ\text{C}$  (unless otherwise specified)**

**• Static characteristics**

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}$ $I_D = 250\ \mu\text{A}$	600	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ $I_D = 3.5\ \text{mA}$	3.0	4.0	5.0	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 600\text{ V}$ $V_{GS} = 0\text{ V}$ $T_{ch} = 25^\circ\text{C}$	-	-	25	$\mu\text{A}$
		$V_{DS} = 480\text{ V}$ $V_{GS} = 0\text{ V}$ $T_{ch} = 125^\circ\text{C}$	-	-	250	
Gate-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}$ $V_{GS} = \pm 30\text{ V}$	-	10	100	nA
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$ $I_D = 5.7\ \text{A}$	-	0.134	0.150	$\Omega$
Gate resistance	$r_g$	$f = 1\ \text{MHz}$ , open drain	-	8.3	-	$\Omega$

**• Dynamic characteristics**

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Forward Transconductance	$g_{fs}$	$V_{DS} = 25\text{ V}$ $I_D = 11.4\ \text{A}$	4	16	-	S
Input Capacitance	$C_{iss}$	$V_{DS} = 400\text{ V}$ $V_{GS} = 0\text{ V}$ $f = 250\ \text{kHz}$	-	1190	-	$\mu\text{F}$
Output Capacitance	$C_{oss}$		-	42	-	
Reverse Transfer Capacitance	$C_{rss}$		-	5.8	-	
Effective output capacitance, energy related (Note *7)	$C_{o(er)}$	$V_{DS} = 0 \dots 400\text{ V}$ $V_{GS} = 0\text{ V}$	-	103	-	$\text{pF}$
Effective output capacitance, time related (Note *8)	$C_{o(tr)}$	$V_{DS} = 0 \dots 400\text{ V}$ $V_{GS} = 0\text{ V}$ $I_D = \text{constant}$	-	410	-	
Turn-On Time	$t_{d(on)}$	$V_{DD} = 400\text{ V}$ $V_{GS} = 10\text{ V}$	-	41	-	ns
	$t_r$	$I_D = 11.4\ \text{A}$	-	38	-	
Turn-Off Time	$t_{d(off)}$	$R_G = 33\ \Omega$	-	198	-	
	$t_f$	See Figure 3 and 4	-	21	-	
Total Gate Charge	$Q_G$	$V_{DD} = 400\text{ V}$ $V_{GS} = 10\text{ V}$ $I_D = 22.7\ \text{A}$	-	59	-	nC
Gate-Source Charge	$Q_{GS}$	See Figure 5	-	25	-	
Gate-Drain Charge	$Q_{GD}$		-	34	-	

Note \*7 :  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400 V.

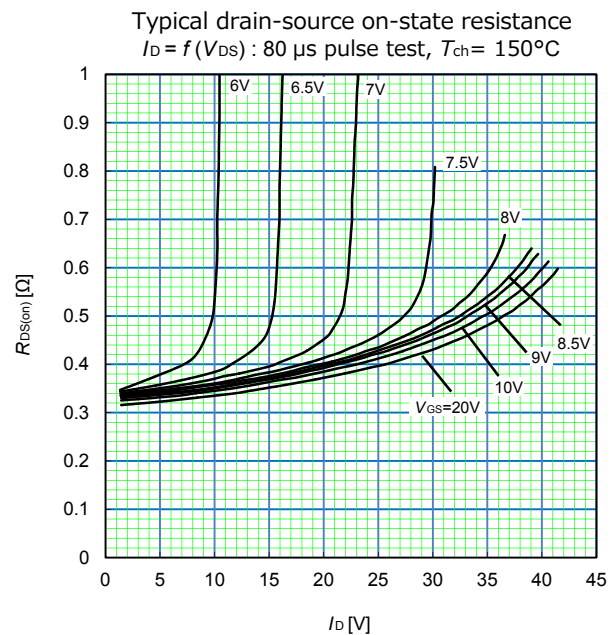
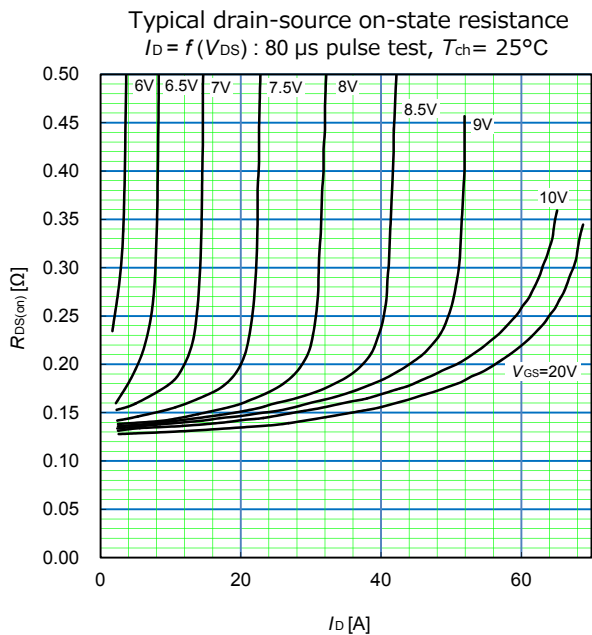
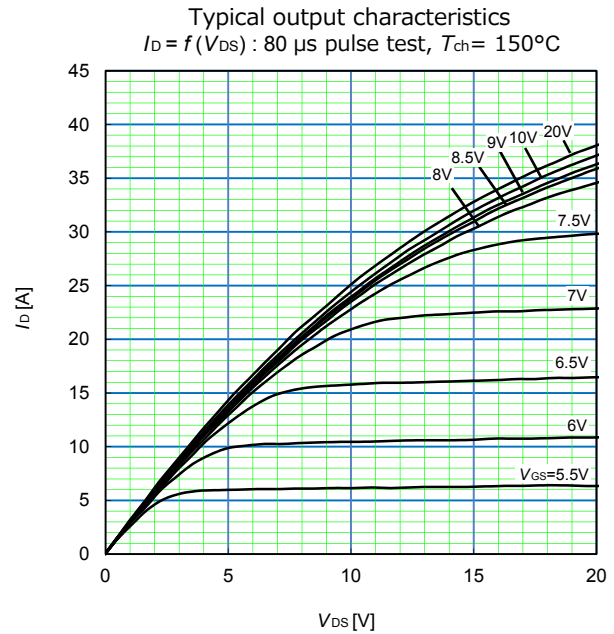
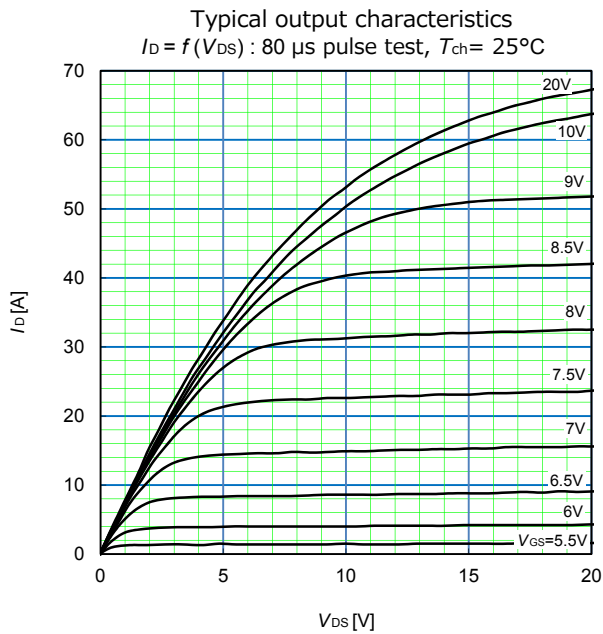
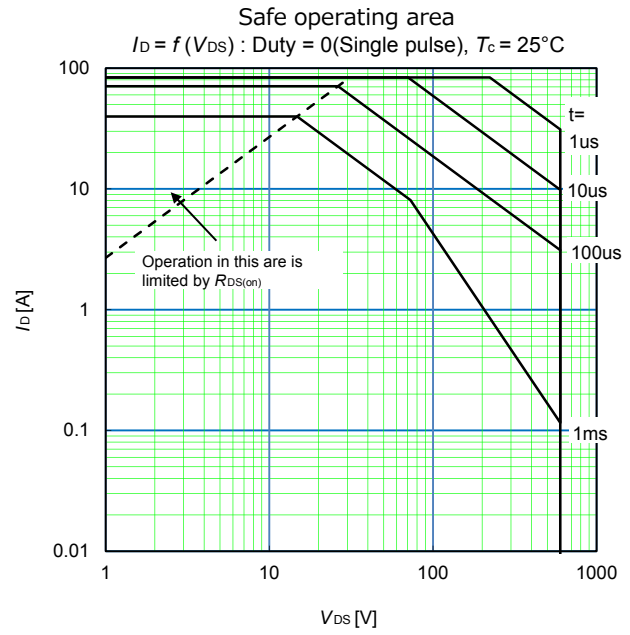
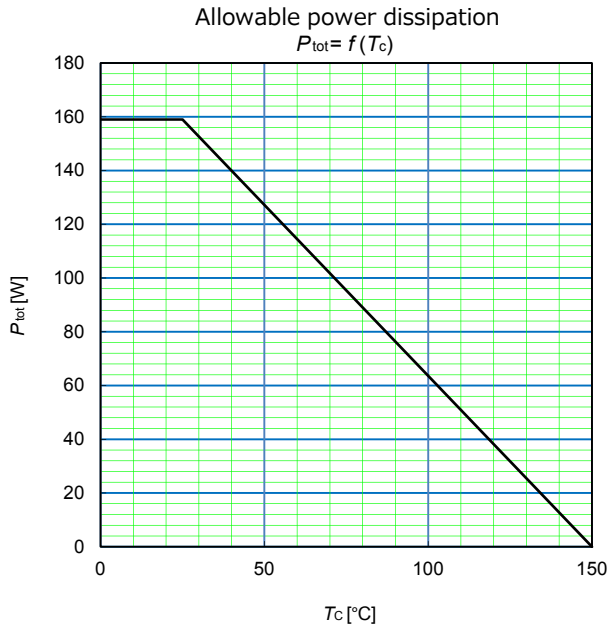
Note \*8 :  $C_{o(tr)}$  is a fixed capacitance that gives the same charging times as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400 V.

**• Reverse diode characteristics**

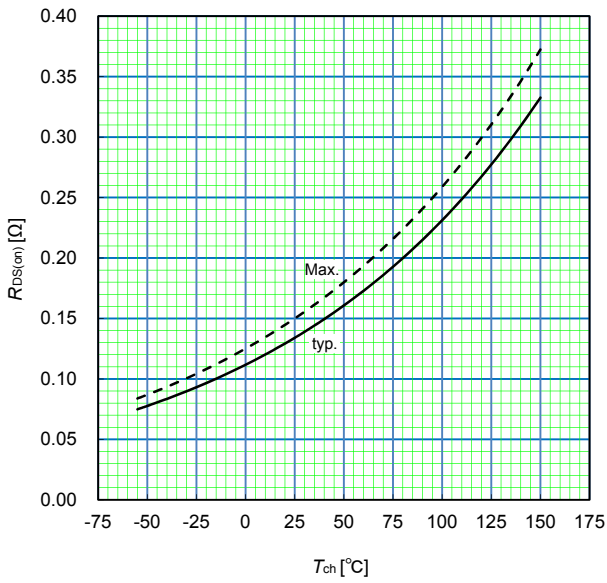
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Diode Forward On-Voltage	$V_{DSR}$	$I_{DR} = 22.7\ \text{A}$ , $V_{GS} = 0\text{ V}$ $T_{ch} = 25^\circ\text{C}$	-	1.00	1.35	V
Reverse Recovery Time	$t_{rr}$	$V_{DD} = 400\text{ V}$ $I_{DR} = 22.7\ \text{A}$	-	160	-	ns
Reverse Recovery Charge	$Q_{rr}$	$V_{GS} = 0\text{ V}$ $-di_{DR}/dt = 100\ \text{A}/\mu\text{s}$ $T_{ch} = 25^\circ\text{C}$	-	1.2	-	$\mu\text{C}$
Peak Reverse Recovery Current	$I_{rrm}$	See Figure 6 and 7	-	14.5	-	A

**■ Thermal Resistance**

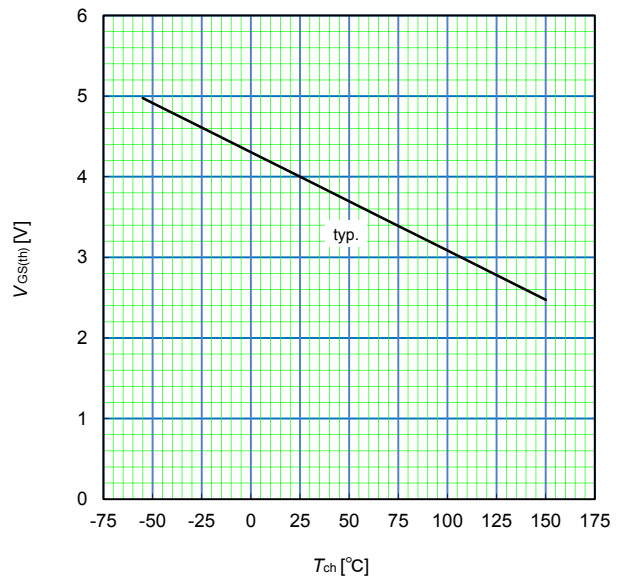
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Thermal Resistance, Channel – Ambient	$R_{th(ch-a)}$	Device mounted on PCB (FR4) Size:40mm*40mm*1.5mm with 6cm <sup>2</sup> copper area (one layer, 70 $\mu\text{m}$ thickness) for drain connection and cooling.	-	-	45	$^\circ\text{C}/\text{W}$
Thermal Resistance, Channel – Case	$R_{th(ch-c)}$		-	-	0.786	$^\circ\text{C}/\text{W}$



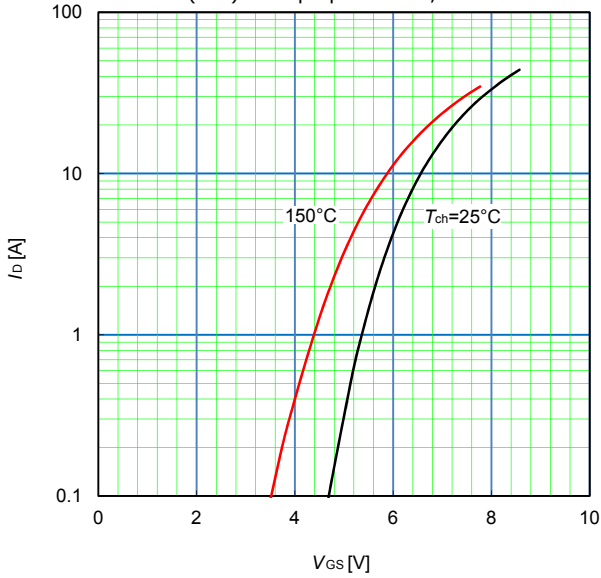
Drain-source on-state resistance  
 $R_{DS(on)} = f(T_{ch}) : I_D = 5.7 \text{ A}, V_{GS} = 10 \text{ V}$



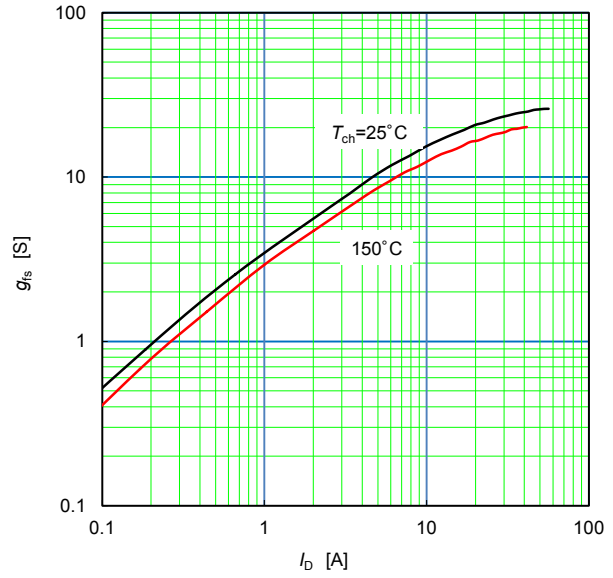
Gate threshold voltage  
 $V_{GS(th)} = f(T_{ch}) : V_{DS} = V_{GS}, I_D = 3.5 \text{ mA}$



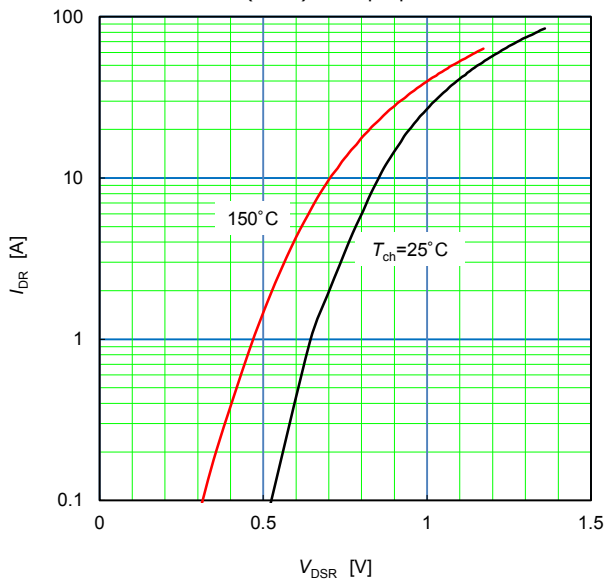
Typical transfer characteristic  
 $I_D = f(V_{GS}) : 80 \mu\text{s pulse test}, V_{DS} = 25 \text{ V}$



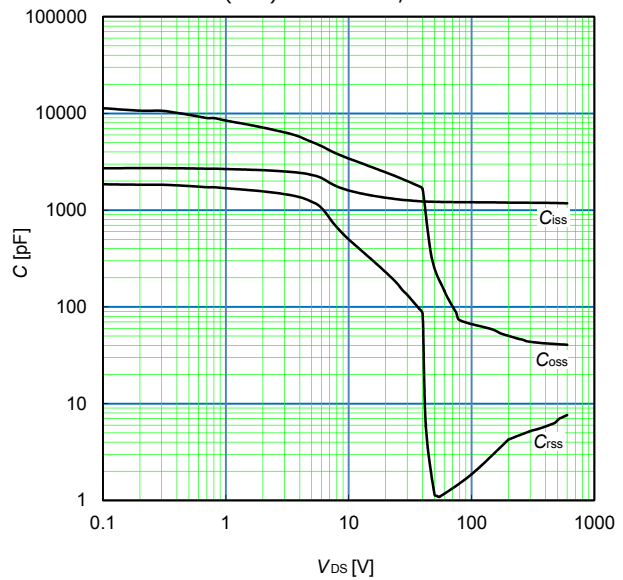
Typical transconductance  
 $g_{fs} = f(I_D) : 80 \mu\text{s pulse test}, V_{DS} = 25 \text{ V}$



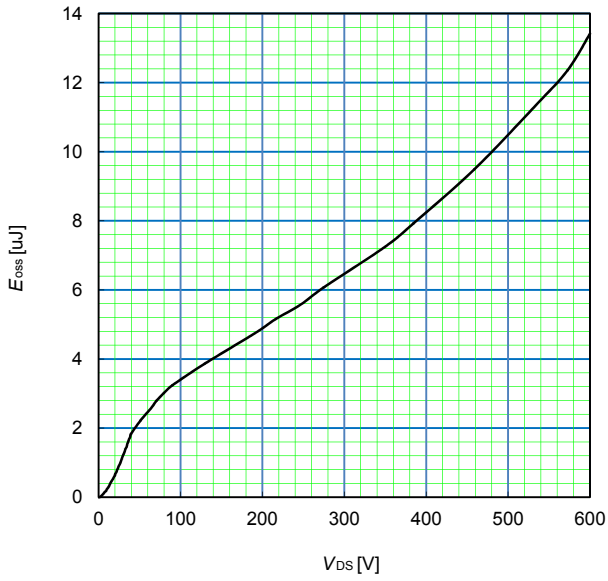
Typical forward characteristics of reverse diode  
 $I_{DR} = f(V_{DSR}) : 80 \mu\text{s pulse test}$



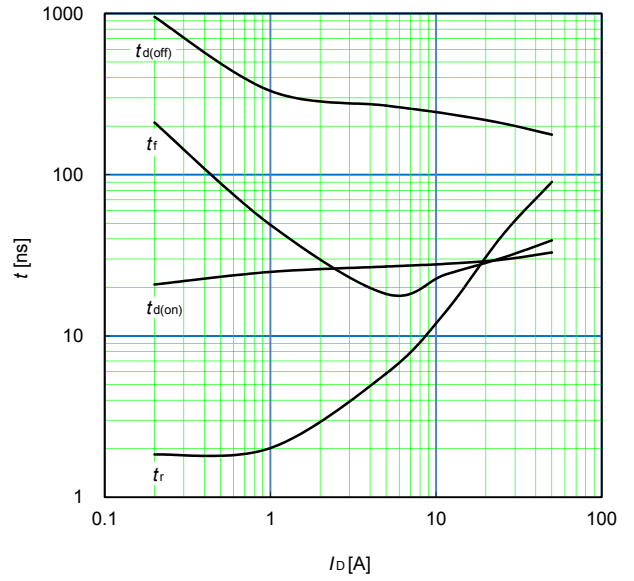
Typical capacitance  
 $C = f(V_{DS}) : V_{GS} = 0 \text{ V}, f = 250 \text{ kHz}$



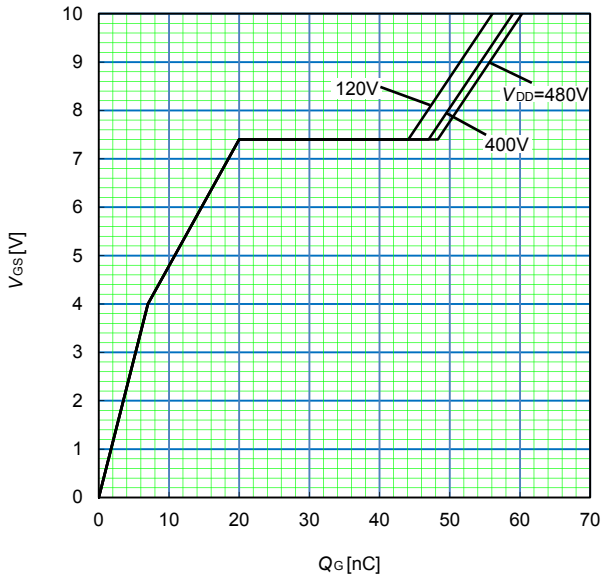
Typical  $C_{oss}$  stored energy



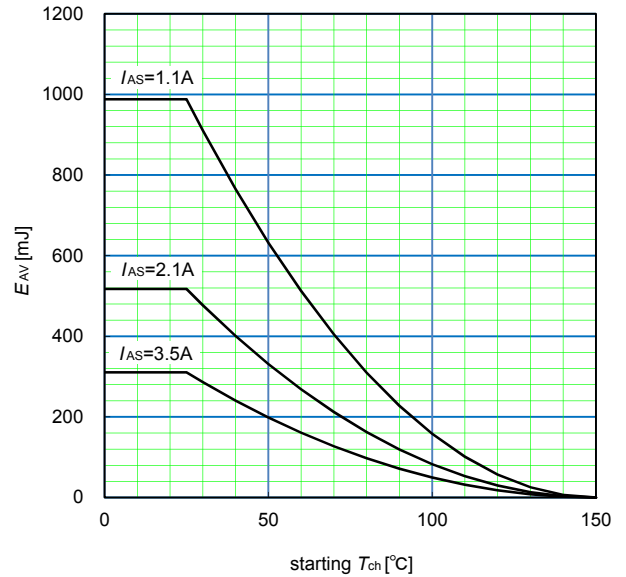
Typical switching times vs.  $I_D$   
 $t = f(I_D) : V_{DD} = 400 \text{ V}, V_{GS} = 10 \text{ V/0 V}, R_G = 24 \Omega, T_{ch} = 25^\circ\text{C}$



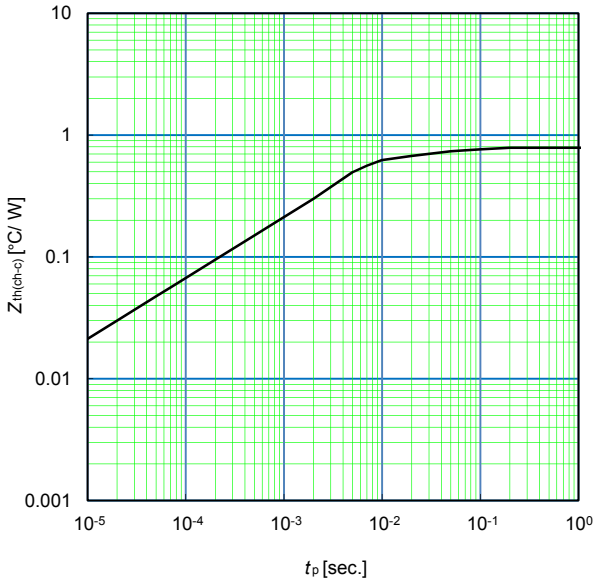
Typical gate charge  
 $V_{GS} = f(Q_G) : I_D = 22.7 \text{ A}, T_{ch} = 25^\circ\text{C}$



Maximum Avalanche Energy  
 $E_{AV} = f(\text{starting } T_{ch}) : V_{DD} = 60 \text{ V}, I_{AS} \leq 3.5 \text{ A}$



Transient Thermal Impedance  
 $Z_{th(ch-c)} = f(t) : D = 0$



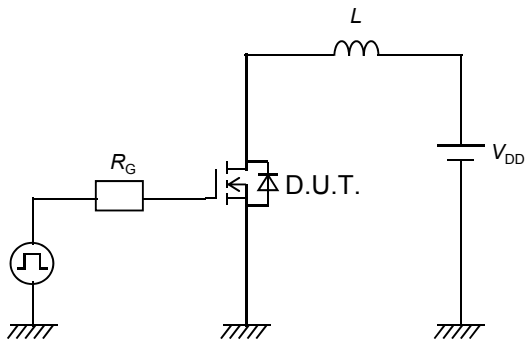


Figure 1. Unclamped inductive load test circuit

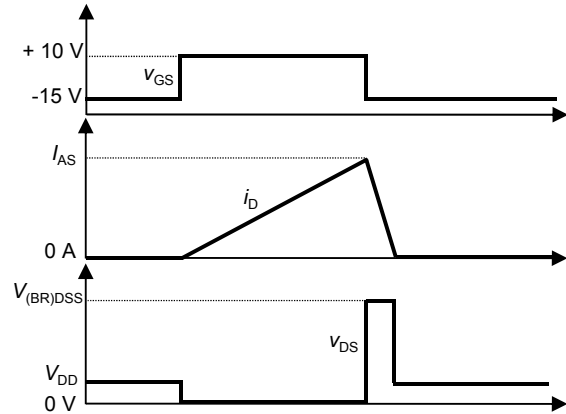


Figure 2. Unclamped inductive waveform

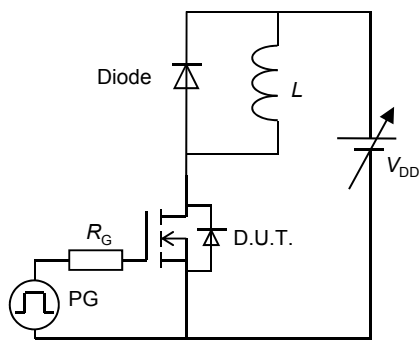


Figure 3. Switching test circuit

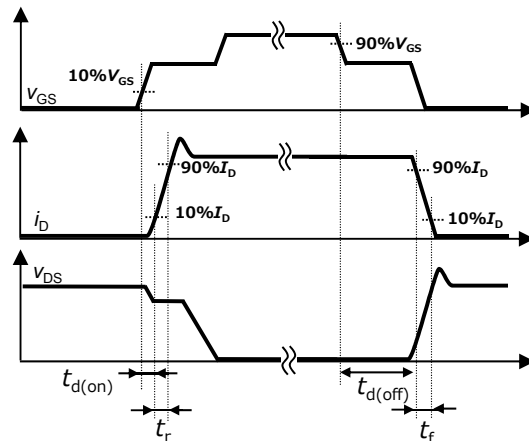


Figure 4. Switching times waveform

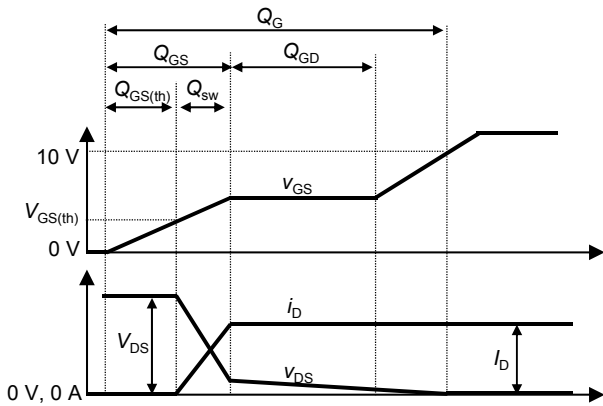


Figure 5. Gate charge waveform

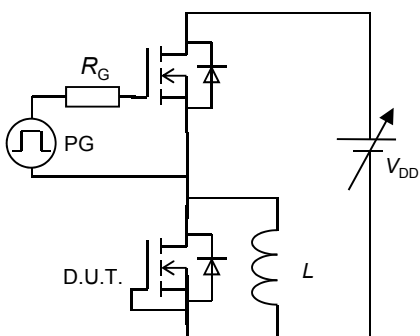


Figure 6. Diode reverse recovery test circuit

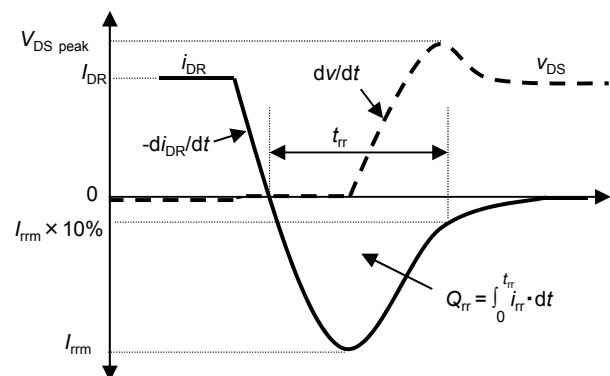
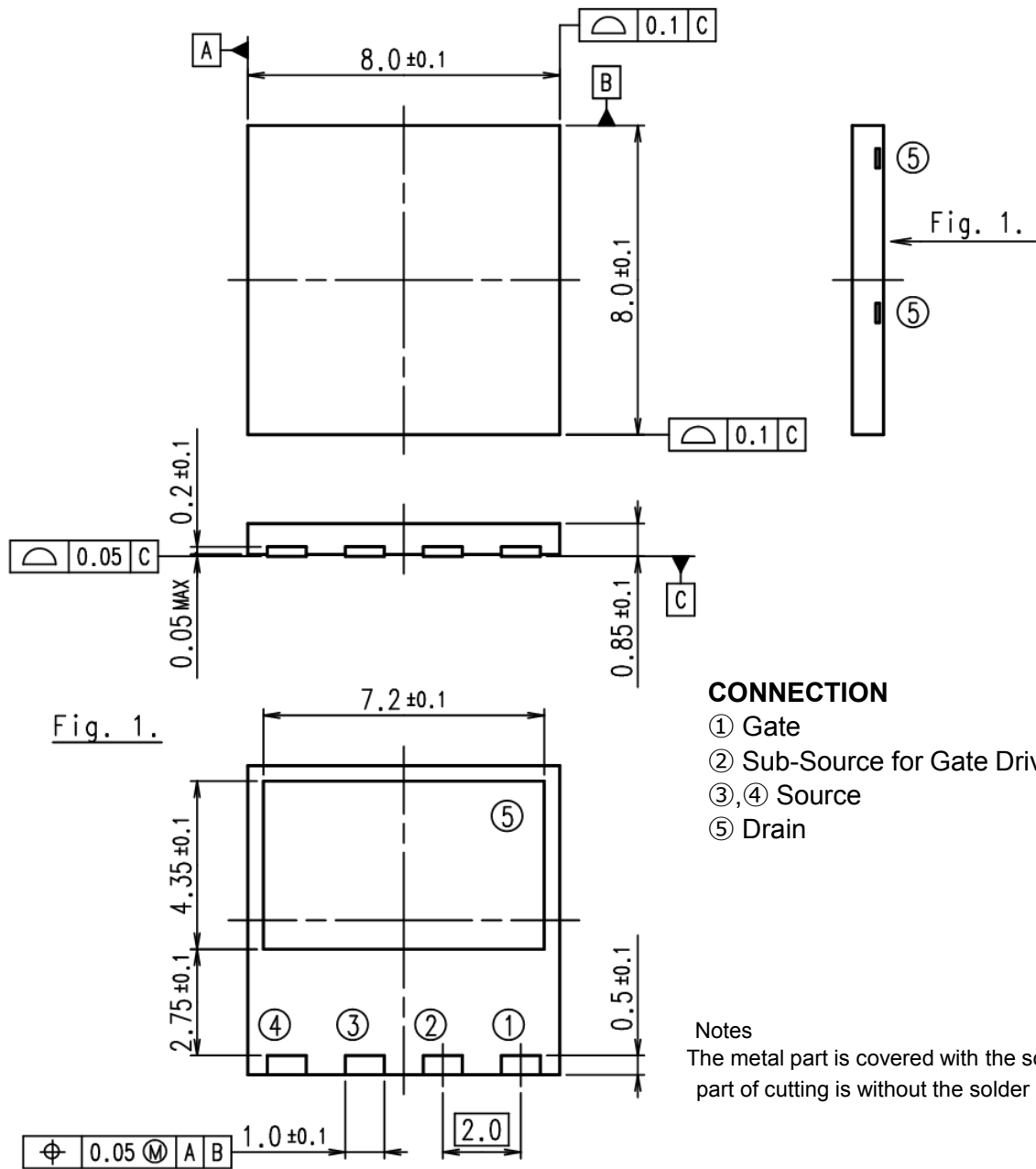


Figure 7. Diode reverse recovery waveform

■ Package Dimensions : DFN8x8 Package



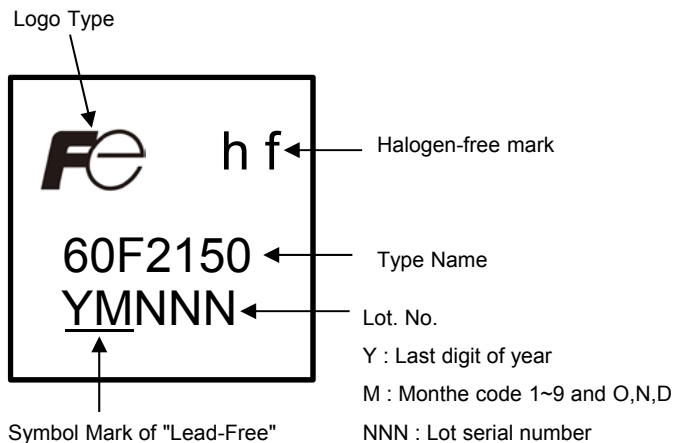
**CONNECTION**

- ① Gate
- ② Sub-Source for Gate Drive
- ③,④ Source
- ⑤ Drain

**Notes**

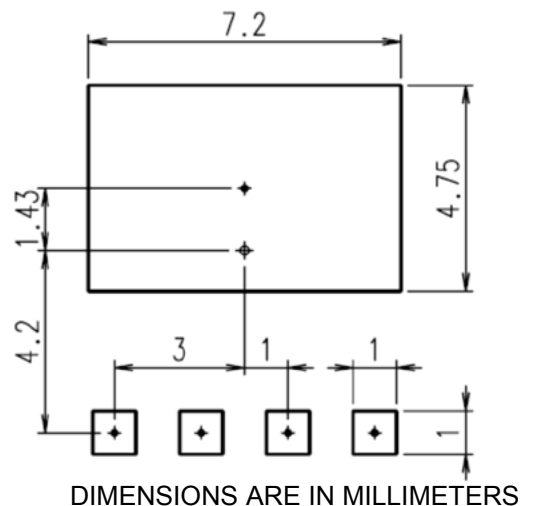
The metal part is covered with the solder plating, part of cutting is without the solder plating.

■ Marking



\* The font (font type,size) and the trademark-size might be actually different.

■ Recommended footprint



DIMENSIONS ARE IN MILLIMETERS

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