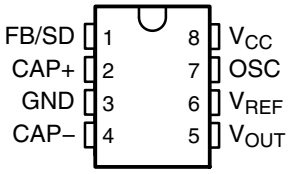
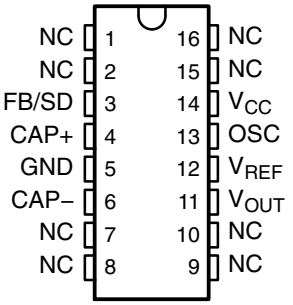
- **Output Current . . . 100 mA**
- **Low Loss . . . 1.1 V at 100 mA**
- **Operating Range . . . 3.5 V to 15 V**
- **Reference and Error Amplifier for Regulation**
- **External Shutdown**
- **External Oscillator Synchronization**
- **Devices Can Be Paralleled**
- **Pin-to-Pin Compatible With the LTC1044/7660**

P PACKAGE
(TOP VIEW)



DW PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The LT1054 is a bipolar, switched-capacitor voltage converter with regulator. It provides higher output current and significantly lower voltage losses than previously available converters. An adaptive-switch drive scheme optimizes efficiency over a wide range of output currents. Total voltage drop at 100-mA output current typically is 1.1 V. This applies to the full supply-voltage range of 3.5 V to 15 V. Quiescent current typically is 2.5 mA.

The LT1054 also provides regulation, a feature previously not available in switched-capacitor voltage converters. By adding an external resistive divider, a regulated output can be obtained. This output is regulated against changes in both input voltage and output current. The LT1054 also can be shut down by grounding the feedback terminal. Supply current in shutdown typically is 100 μA.

The internal oscillator of the LT1054 runs at a nominal frequency of 25 kHz. The oscillator terminal can be used to adjust the switching frequency or to externally synchronize the LT1054.

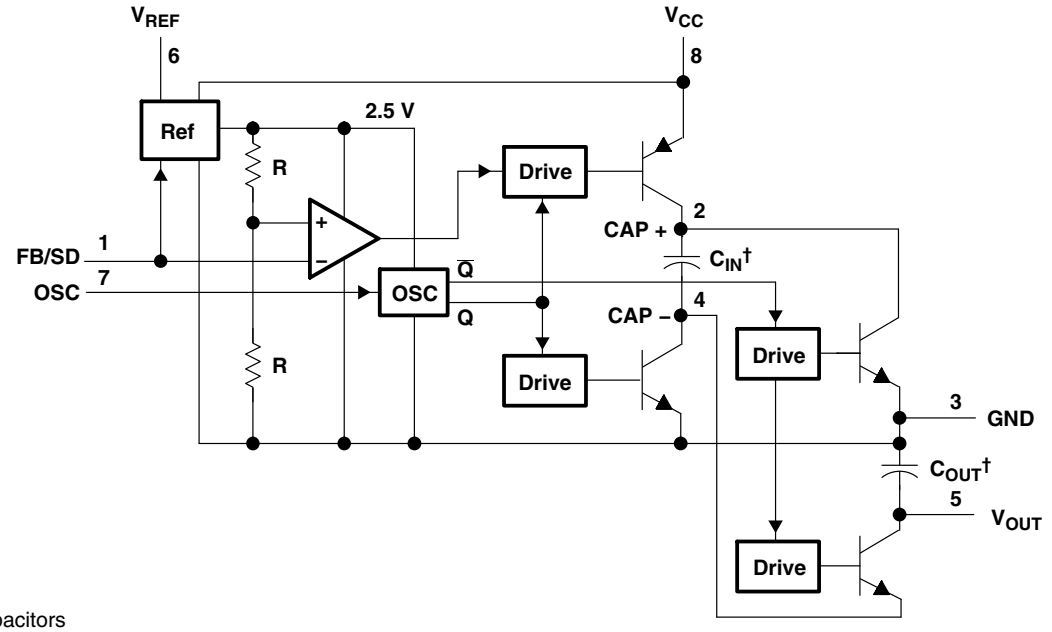
The LT1054C is characterized for operation over a free-air temperature range of 0°C to 70°C. The LT1054I is characterized for operation over a free-air temperature range of –40°C to 85°C.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP (P)	Tube of 50	LT1054IP	LT1054IP
	SOIC (DW)	Tube of 40	LT1054IDW	LT1054I
		Reel of 2000	LT1054IDWR	
0°C to 70°C	PDIP (P)	Tube of 50	LT1054CP	LT1054CP
	SOIC (DW)	Tube of 40	LT1054CDW	LT1054C
		Reel of 2000	LT1054CDWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

functional block diagram



† External capacitors
Pin numbers shown are for the P package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} (see Note 1) . . . . . 16 V
Input voltage range, V_I: FB/SD . . . . . 0 V to V_{CC}
OSC . . . . . 0 V to V_{ref}
Junction temperature, T_J (see Note 2): LT1054C . . . . . 125°C
LT1054I . . . . . 135°C
Package thermal impedance, θ_{JA} (see Notes 3 and 4): DW package . . . . . 57°C/W
P package . . . . . 85°C/W
Storage temperature range, T_{stg} . . . . . –55°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The absolute maximum supply-voltage rating of 16 V is for unregulated circuits. For regulation-mode circuits with $V_{OUT} \leq 15$ V, this rating may be increased to 20 V.
2. The devices are functional up to the absolute maximum junction temperature.
3. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
4. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3.5	15	V
T_A	Operating free-air temperature range	LT1054C	0	70	°C
		LT1054I	–40	85	

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	LT1054C LT1054I			UNIT
					MIN	TYP‡	MAX	
V_O	Regulated output voltage	V_{CC} = 7 V, T_J = 25°C, R_L = 500 Ω, See Note 5		25°C	–4.7	–5	–5.2	V
	Input regulation	V_{CC} = 7 V to 12 V, R_L = 500 Ω, See Note 5		Full range		5	25	mV
	Output regulation	V_{CC} = 7 V, R_L = 100 Ω to 500 Ω, See Note 5		Full range		10	50	mV
	Voltage loss, $V_{CC} - \lvert V_O \rvert$ (see Note 6)	$C_I = C_O$ = 100-μF tantalum	I_O = 10 mA	Full range		0.35	0.55	V
			I_O = 100 mA			1.1	1.6	
	Output resistance	ΔI_O = 10 mA to 100 mA,	See Note 7	Full range		10	15	Ω
	Oscillator frequency	V_{CC} = 3.5 V to 15 V		Full range	15	25	35	kHz
V_{ref}	Reference voltage	$I_{(REF)}$ = 60 μA		25°C	2.35	2.5	2.65	V
				Full range	2.25		2.75	
	Maximum switch current			25°C		300		mA
I_{CC}	Supply current	I_O = 0	V_{CC} = 3.5 V	Full range		2.5	4	mA
			V_{CC} = 15 V			3	5	
	Supply current in shutdown	$V_{(FB/SD)}$ = 0 V		Full range		100	200	μA

† Full range is 0°C to 70°C for the LT1054C and –40°C to 85°C for the LT1054I.
‡ All typical values are at T_A = 25°C.

NOTES: 5. All regulation specifications are for a device connected as a positive-to-negative converter/regulator with R1 = 20 kΩ, R2 = 102.5 kΩ, external capacitor C_{IN} = 10 μF (tantalum), external capacitor C_{OUT} = 100 μF (tantalum) and C1 = 0.002 μF (see Figure 15).
6. For voltage-loss tests, the device is connected as a voltage inverter, with terminals 1, 6, and 7 unconnected. The voltage losses may be higher in other configurations. C_{IN} and C_{OUT} are external capacitors.
7. Output resistance is defined as the slope of the curve (ΔV_O versus ΔI_O) for output currents of 10 mA to 100 mA. This represents the linear portion of the curve. The incremental slope of the curve is higher at currents less than 10 mA due to the characteristics of the switch transistors.

TYPICAL CHARACTERISTICS

Table of Graphs

Table of Figures

TYPICAL CHARACTERISTICS†

SHUTDOWN THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE

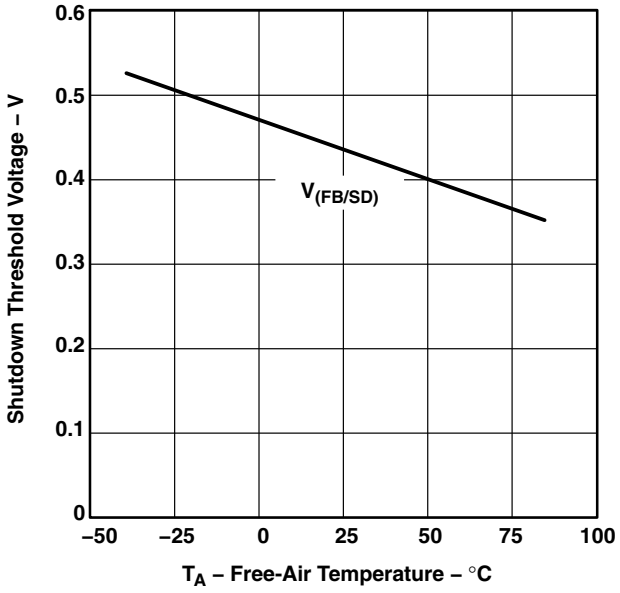


Figure 1

SUPPLY CURRENT vs INPUT VOLTAGE

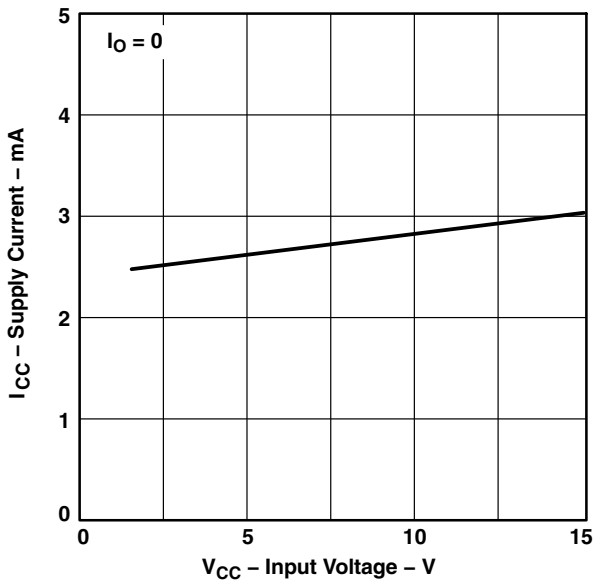


Figure 2

OSCILLATOR FREQUENCY vs FREE-AIR TEMPERATURE

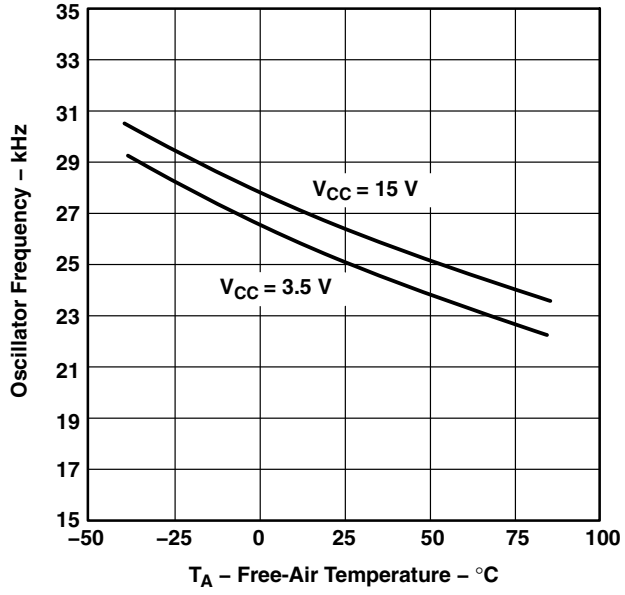


Figure 3

SUPPLY CURRENT IN SHUTDOWN vs INPUT VOLTAGE

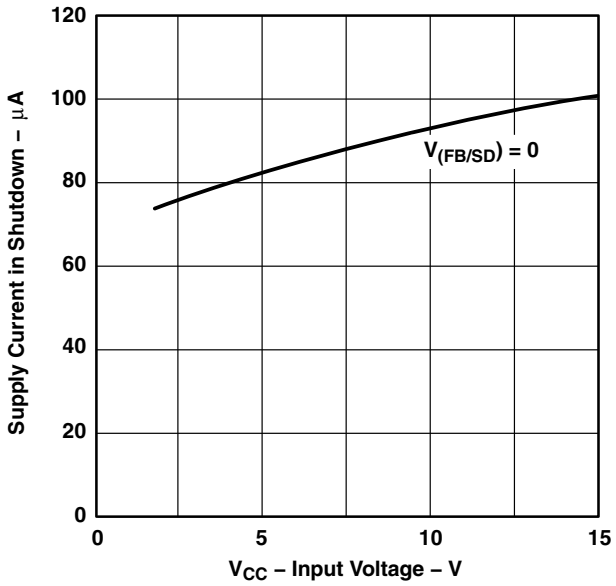


Figure 4

† Data at high and low temperatures are applicable only within the recommended operating free-air temperature range.

TYPICAL CHARACTERISTICS

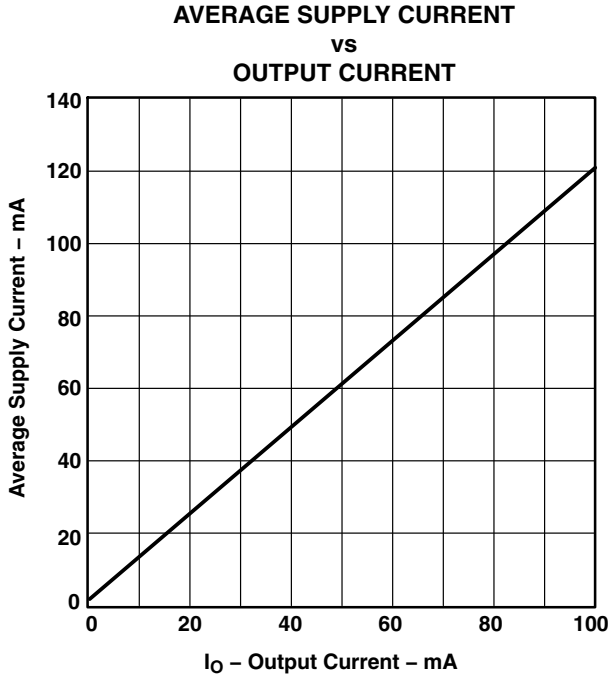


Figure 5

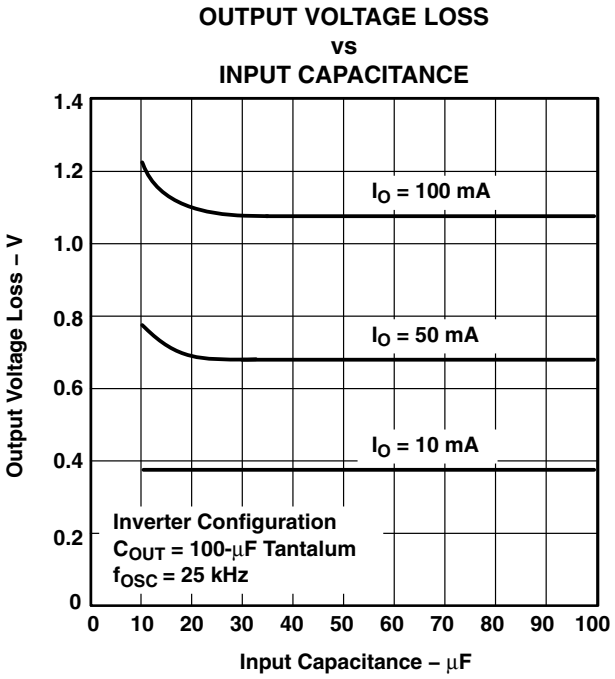


Figure 6

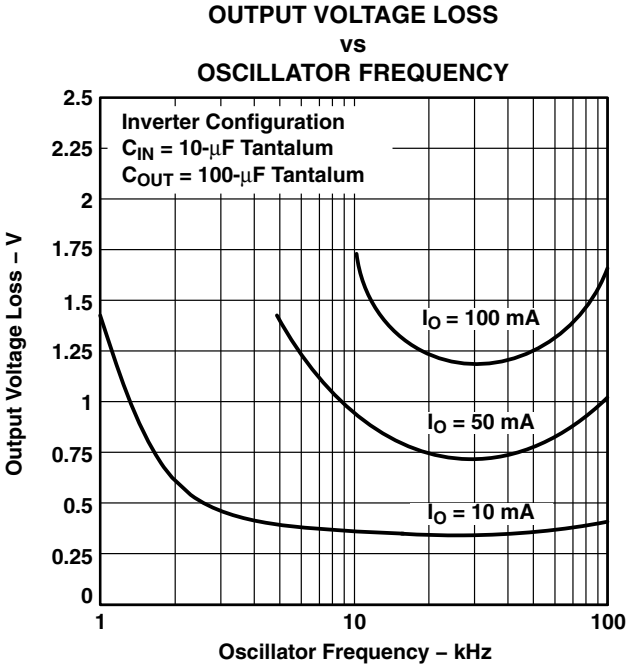


Figure 7

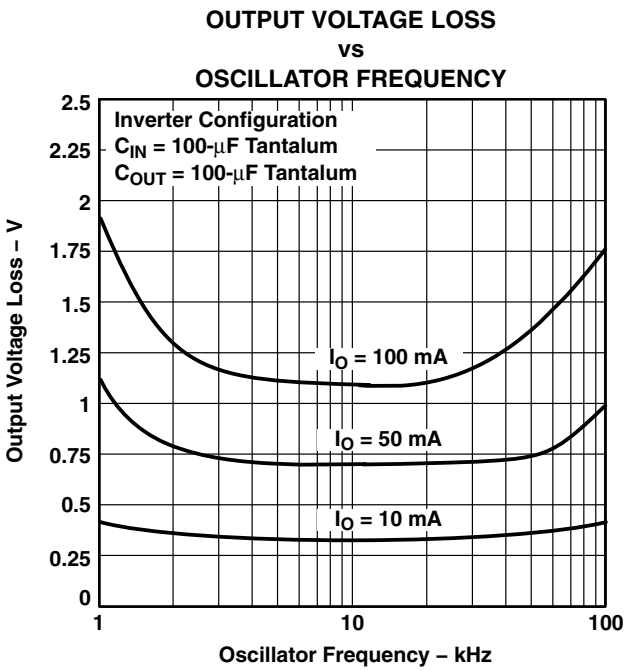


Figure 8

TYPICAL CHARACTERISTICS†

REGULATED OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

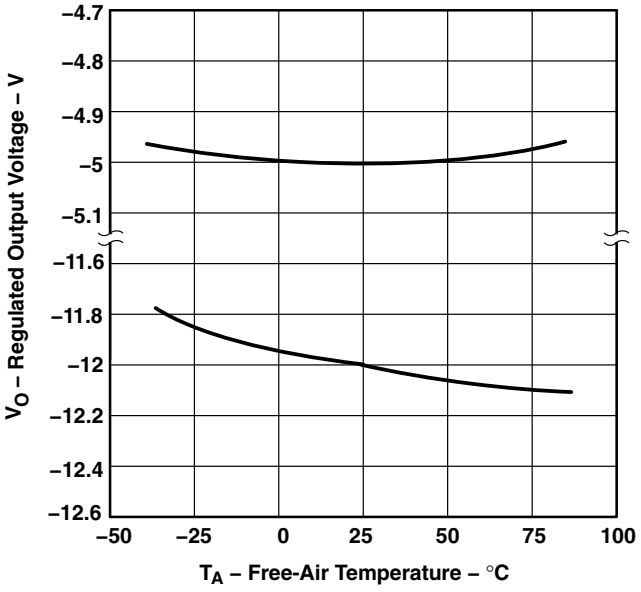


Figure 9

REFERENCE VOLTAGE CHANGE
vs
FREE-AIR TEMPERATURE

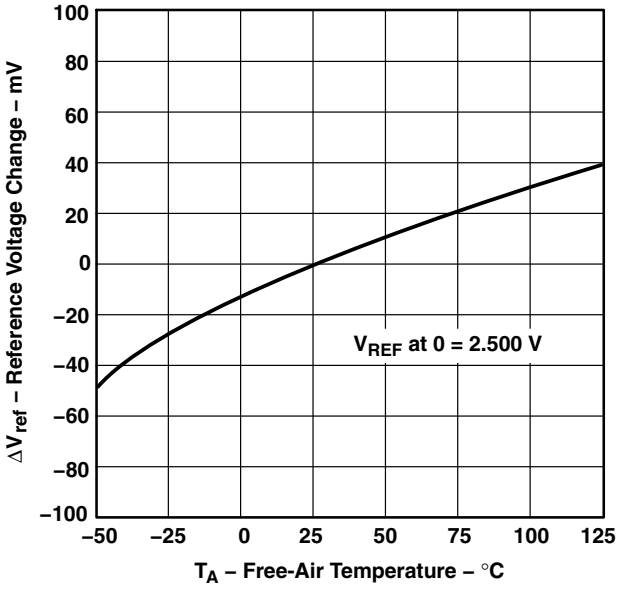


Figure 10

VOLTAGE LOSS
vs
OUTPUT CURRENT

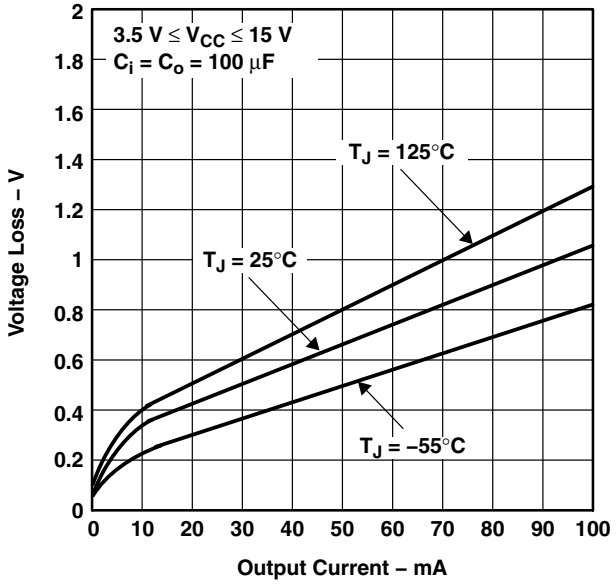


Figure 11

† Data at high and low temperatures are applicable only within the recommended operating free-air temperature range.

PRINCIPLES OF OPERATION

A review of a basic switched-capacitor building block is helpful in understanding the operation of the LT1054. When the switch shown in Figure 12 is in the left position, capacitor C1 charges to the voltage at V1. The total charge on C1 is q1 = C1V1. When the switch is moved to the right, C1 is discharged to the voltage at V2. After this discharge time, the charge on C1 is q2 = C1V2. The charge has been transferred from the source V1 to the output V2. The amount of charge transferred is shown in equation 1.

$$\Delta q = q1 - q2 = C1(V1 - V2) \tag{1}$$

If the switch is cycled f times per second, the charge transfer per unit time (i.e., current) is as shown in equation 2.

$$I = f \times \Delta q = f \times C1(1 - V2) \tag{2}$$

To obtain an equivalent resistance for a switched-capacitor network, this equation can be rewritten in terms of voltage and impedance equivalence as shown in equation 3.

$$I = \frac{V1 - V2}{(1/fC1)} = \frac{V1 - V2}{R_{EQUIV}} \tag{3}$$

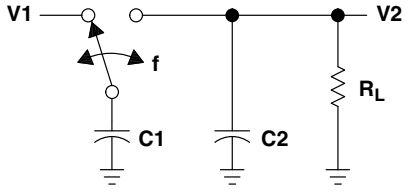


Figure 12. Switched-Capacitor Building Block

A new variable, R_{EQUIV}, is defined as $R_{EQUIV} = 1 \div fC1$. The equivalent circuit for the switched-capacitor network is shown in Figure 13. The LT1054 has the same switching action as the basic switched-capacitor building block. Even though this simplification does not include finite switch-on resistance and output-voltage ripple, it provides an insight into how the device operates.

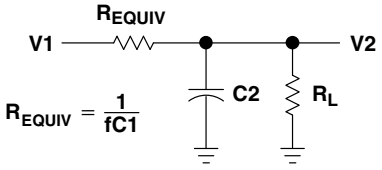


Figure 13. Switched-Capacitor Equivalent Circuit

These simplified circuits explain voltage loss as a function of oscillator frequency (see Figure 7). As oscillator frequency is decreased, the output impedance eventually is dominated by the 1/fC1 term, and voltage losses rise.

Voltage losses also rise as oscillator frequency increases. This is caused by internal switching losses that occur due to some finite charge being lost on each switching cycle. This charge loss per-unit-cycle, when multiplied by the switching frequency, becomes a current loss. At high frequency, this loss becomes significant and voltage losses again rise.

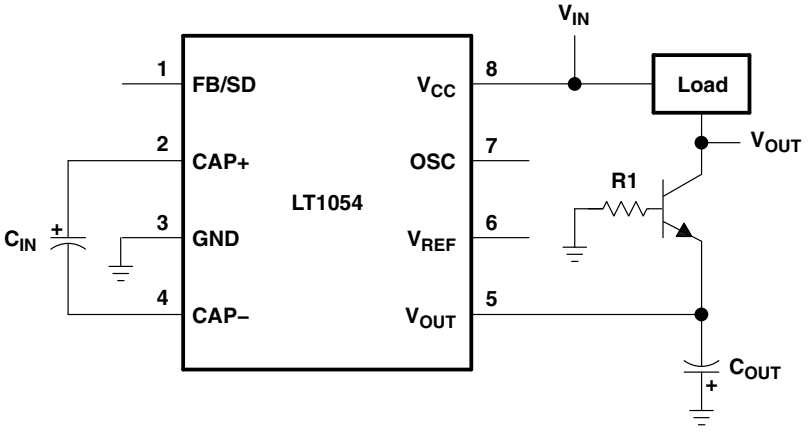
The oscillator of the LT1054 is designed to operate in the frequency band where voltage losses are at a minimum.

PRINCIPLES OF OPERATION

Supply voltage V_{CC} alternately charges C_{IN} to the input voltage when C_{IN} is switched in parallel with the input supply and then transfers charge to C_{OUT} when C_{IN} is switched in parallel with C_{OUT}. Switching occurs at the oscillator frequency. During the time that C_{IN} is charging, the peak supply current is approximately 2.2 times the output current. During the time that C_{IN} is delivering a charge to C_{OUT}, the supply current drops to approximately 0.2 times the output current. An input supply bypass capacitor supplies part of the peak input current drawn by the LT1054 and averages the current drawn from the supply. A minimum input-supply bypass capacitor of 2 μF, preferably tantalum or some other low equivalent-series-resistance (ESR) type, is recommended. A larger capacitor is desirable in some cases. An example of this would be when the actual input supply is connected to the LT1054 through long leads or when the pulse currents drawn by the LT1054 might affect other circuits through supply coupling.

In addition to being the output terminal, V_{OUT} is tied to the substrate of the device. Special care must be taken in LT1054 circuits to avoid making V_{OUT} positive with respect to any of the other terminals. For circuits with the output load connected from V_{CC} to V_{OUT} or from some external positive supply voltage to V_{OUT}, an external transistor must be added (see Figure 14). This transistor prevents V_{OUT} from being pulled above GND during startup. Any small general-purpose transistor such as a 2N2222 or a 2N2219 device can be used. Resistor R1 should be chosen to provide enough base drive to the external transistor so that it is saturated under nominal output voltage and maximum output current conditions.

$$R1 \leq \frac{(|V_{OUT}|)\beta}{I_{OUT}} \tag{4}$$



Pin numbers shown are for the P package.

Figure 14. Circuit With Load Connected from V_{CC} to V_{OUT}

PRINCIPLES OF OPERATION

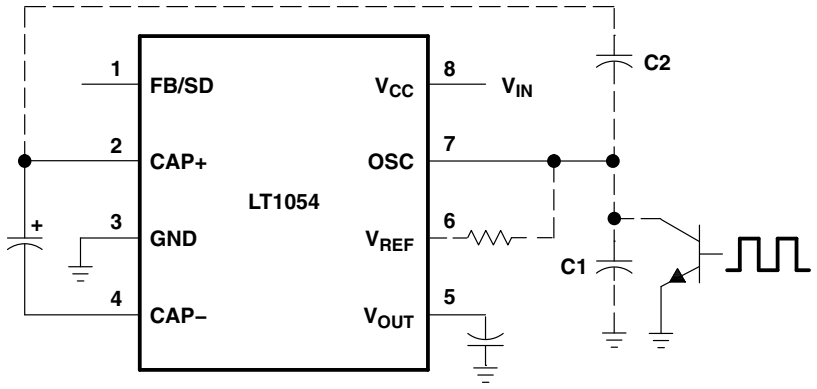
The voltage reference (V_{ref}) output provides a 2.5-V reference point for use in LT1054-based regulator circuits. The temperature coefficient (TC) of the reference voltage has been adjusted so that the TC of the regulated output voltage is near zero. As seen in the typical performance curves, this requires the reference output to have a positive TC. This nonzero drift is necessary to offset a drift term inherent in the internal reference divider and comparator network tied to the feedback terminal. The overall result of these drift terms is a regulated output that has a slight positive TC at output voltages below 5 V and a slight negative TC at output voltages above 5 V. For regulator feedback networks, reference output current should be limited to approximately 60 μA. V_{ref} draws approximately 100 μA when shorted to ground and does not affect the internal reference/regulator. This terminal also can be used as a pullup for LT1054 circuits that require synchronization.

CAP+ is the positive side of input capacitor C_{IN} and is driven alternately between V_{CC} and ground. When driven to V_{CC}, CAP+ sources current from V_{CC}. When driven to ground, CAP+ sinks current to ground. CAP– is the negative side of the input capacitor and is driven alternately between ground and V_{OUT}. When driven to ground, CAP– sinks current to ground. When driven to V_{OUT}, CAP– sources current from C_{OUT}. In all cases, current flow in the switches is unidirectional, as should be expected when using bipolar switches.

OSC can be used to raise or lower the oscillator frequency or to synchronize the device to an external clock. Internally, OSC is connected to the oscillator timing capacitor ($C_t \approx 150$ pF), which is charged and discharged alternately by current sources of ±7 μA, so that the duty cycle is approximately 50%. The LT1054 oscillator is designed to run in the frequency band where switching losses are minimized. However, the frequency can be raised, lowered, or synchronized to an external system clock if necessary.

The frequency can be increased by adding an external capacitor (C2 in Figure 15) in the range of 5–20 pF from CAP+ to OSC. This capacitor couples a charge into C_t at the switch transitions. This shortens the charge and discharge times and raises the oscillator frequency. Synchronization can be accomplished by adding an external pullup resistor from OSC to V_{ref}. A 20-kΩ pullup resistor is recommended. An open-collector gate or an npn transistor then can be used to drive OSC at the external clock frequency as shown in Figure 15.

The frequency can be lowered by adding an external capacitor (C_1 in Figure 15) from OSC to ground. This increases the charge and discharge times, which lowers the oscillator frequency.



Pin numbers shown are for the P package.

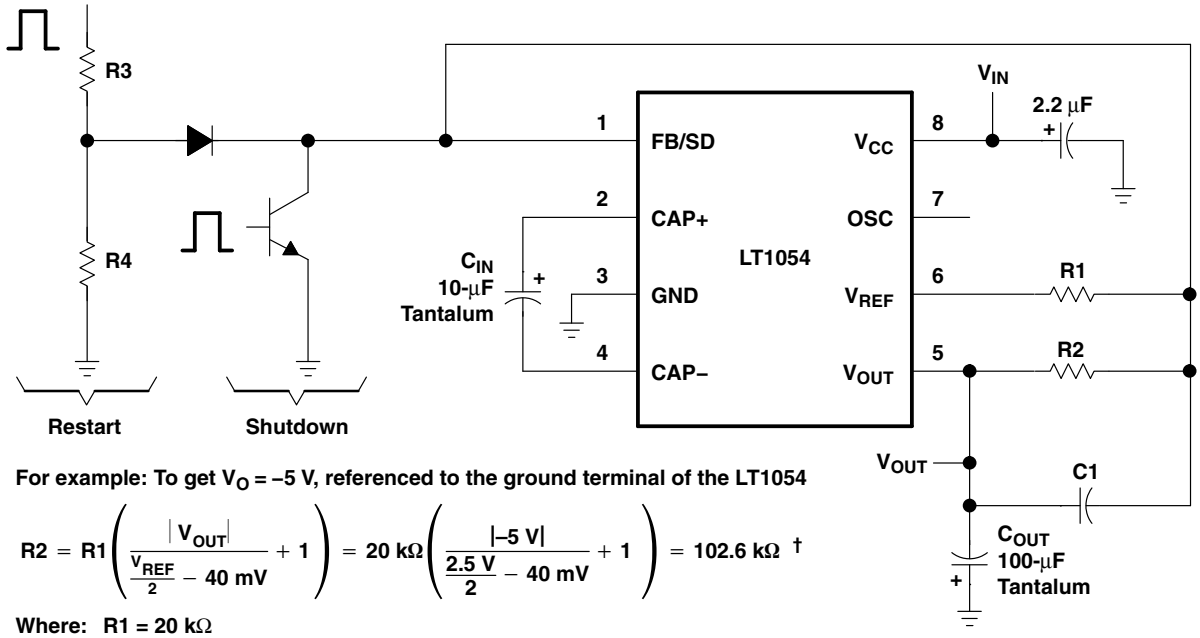
Figure 15. External-Clock System

APPLICATION INFORMATION

regulation

The feedback/shutdown (FB/SD) terminal has two functions. Pulling FB/SD below the shutdown threshold (≈ 0.45 V) puts the device into shutdown. In shutdown, the reference/regulator is turned off and switching stops. The switches are set such that both C_{IN} and C_{OUT} are discharged through the output load. Quiescent current in shutdown drops to approximately 100 μA. Any open-collector gate can be used to put the LT1054 into shutdown. For normal (unregulated) operation, the device will restart when the external gate is shut off. In LT1054 circuits that use the regulation feature, the external resistor divider can provide enough pulldown to keep the device in shutdown until the output capacitor (C_{OUT}) has fully discharged. For most applications, where the LT1054 is run intermittently, this does not present a problem because the discharge time of the output capacitor is short compared to the off time of the device. In applications where the device has to start up before the output capacitor (C_{OUT}) has fully discharged, a restart pulse must be applied to FB/SD of the LT1054. Using the circuit shown in Figure 16, the restart signal can be either a pulse (t_p > 100 μs) or a logic high. Diode coupling the restart signal into FB/SD allows the output voltage to rise and regulate without overshoot. The resistor divider R3/R4 shown in Figure 16 should be chosen to provide a signal level at FB/SD of 0.7–1.1 V.

FB/SD also is the inverting input of the LT1054 error amplifier and, as such, can be used to obtain a regulated output voltage.



For example: To get V_O = –5 V, referenced to the ground terminal of the LT1054

$$R2 = R1\left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40\text{ mV}} + 1\right) = 20\text{ k}\Omega\left(\frac{|-5\text{ V}|}{\frac{2.5\text{ V}}{2} - 40\text{ mV}} + 1\right) = 102.6\text{ k}\Omega\ ^{\dagger}$$

Where: R1 = 20 kΩ
V_{REF} = 2.5 V Nominal

† Choose the closest 1% value.
Pin numbers shown are for the P package.

Figure 16. Basic Regulation Configuration

APPLICATION INFORMATION

regulation (continued)

The error amplifier of the LT1054 drives the pnp switch to control the voltage across the input capacitor (C_{IN}), which determines the output voltage. When the reference and error amplifier of the LT1054 are used, an external resistive divider is all that is needed to set the regulated output voltage. Figure 16 shows the basic regulator configuration and the formula for calculating the appropriate resistor values. R1 should be 20 kΩ or greater because the reference current is limited to ±100 μA. R2 should be in the range of 100 kΩ to 300 kΩ. Frequency compensation is accomplished by adjusting the ratio of C_{IN} to C_{OUT}.

For best results, this ratio should be approximately 1:10. Capacitor C1, required for good load regulation, should be 0.002 μF for all output voltages.

The functional block diagram shows that the maximum regulated output voltage is limited by the supply voltage. For the basic configuration, $|V_{OUT}|$ referenced to the ground terminal of the LT1054 must be less than the total of the supply voltage minus the voltage loss due to the switches. The voltage loss versus output current due to the switches can be found in the typical performance curves. Other configurations, such as the negative doubler, can provide higher voltages at reduced output currents.

capacitor selection

While the exact values of C_{IN} and C_{OUT} are noncritical, good-quality low-ESR capacitors, such as solid tantalum, are necessary to minimize voltage losses at high currents. For C_{IN}, the effect of the ESR of the capacitor is multiplied by four, because switch currents are approximately two times higher than output current. Losses occur on both the charge and discharge cycle, which means that a capacitor with 1 Ω of ESR for C_{IN} has the same effect as increasing the output impedance of the LT1054 by 4 Ω. This represents a significant increase in the voltage losses. C_{OUT} alternately is charged and discharged at a current approximately equal to the output current. The ESR of the capacitor causes a step function to occur in the output ripple at the switch transitions. This step function degrades the output regulation for changes in output load current and should be avoided. A technique used to gain both low ESR and reasonable cost is to parallel a smaller tantalum capacitor with a large aluminum electrolytic capacitor.

output ripple

The peak-to-peak output ripple is determined by the output capacitor and the output current values. Peak-to-peak output ripple is approximated as:

$$\Delta V = \frac{I_{OUT}}{2fC_{OUT}} \quad (5)$$

Where:
ΔV = peak-to-peak ripple
f_{OSC} = oscillator frequency

For output capacitors with significant ESR, a second term must be added to account for the voltage step at the switch transitions. This step is approximately equal to:

$$(2I_{OUT})(\text{ESR of } C_{OUT}) \quad (6)$$

APPLICATION INFORMATION

power dissipation

The power dissipation of any LT1054 circuit must be limited so that the junction temperature of the device does not exceed the maximum junction-temperature ratings. The total power dissipation is calculated from two components–the power loss due to voltage drops in the switches, and the power loss due to drive-current losses. The total power dissipated by the LT1054 is calculated as:

$$P \approx (V_{CC} - |V_{OUT}|)\, I_{OUT} + (V_{CC})(I_{OUT})(0.2) \quad (7)$$

where both V_{CC} and V_{OUT} are referenced to ground. The power dissipation is equivalent to that of a linear regulator. Limited power-handling capability of the LT1054 packages causes limited output-current requirements, or steps can be taken to dissipate power external to the LT1054 for large input or output differentials. This is accomplished by placing a resistor in series with C_{IN} as shown in Figure 17. A portion of the input voltage is dropped across this resistor without affecting the output regulation. Since switch current is approximately 2.2 times the output current and the resistor causes a voltage drop when C_{IN} is both charging and discharging, the resistor chosen is as shown:

$$R_X = \frac{V_X}{4.4\ I_{OUT}} \quad (8)$$

Where:

$V_X \approx V_{CC}$ – [(LT1054 voltage loss)(1.3) + $|V_{OUT}|$]

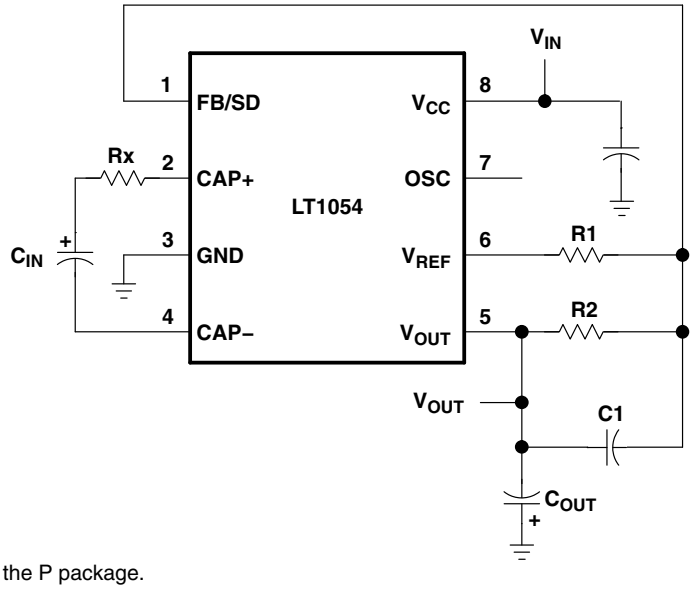
and

I_{OUT} = maximum required output current

The factor of 1.3 allows some operating margin for the LT1054.

When using a 12-V to –5-V converter at 100-mA output current, calculate the power dissipation without an external resistor.

$$P = (12\ V - |-5\ V|)(100\ mA) + (12\ V)(100\ mA)(0.2)$$
$$P = 700\ mW + 240\ mW = 940\ mW \quad (9)$$



Pin numbers shown are for the P package.

Figure 17. Power-Dissipation-Limiting Resistor in Series With C_{IN}

APPLICATION INFORMATION

power dissipation (continued)

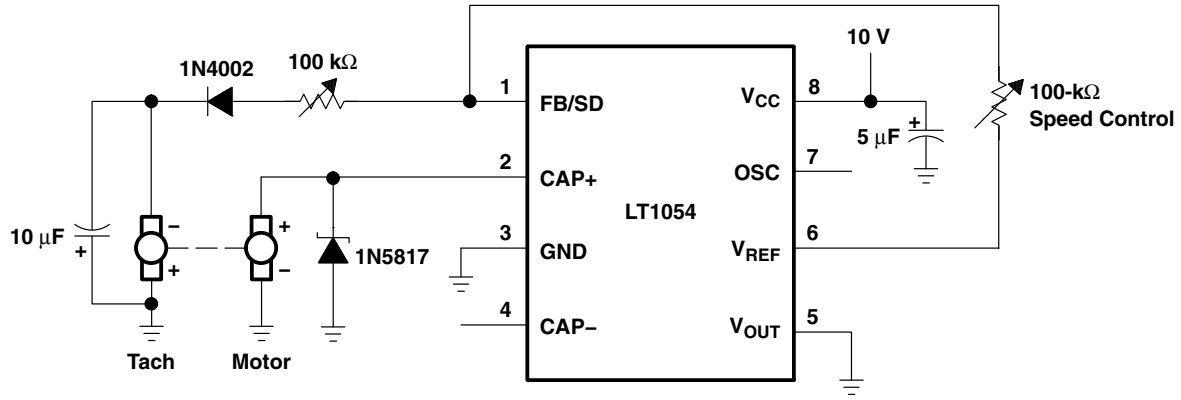
At $R_{\theta JA}$ of 130°C/W for a commercial plastic device, a junction temperature rise of 122°C occurs. The device exceeds the maximum junction temperature at an ambient temperature of 25°C. To calculate the power dissipation with an external resistor (R_X), determine how much voltage can be dropped across R_X. The maximum voltage loss of the LT1054 in the standard regulator configuration at 100 mA output current is 1.6 V.

$$V_X = 12\ V - [(1.6\ V)(1.3) + |-5\ V|] = 4.9\ V \tag{10}$$

and

$$R_X = \frac{4.9\ V}{(4.4)(100\ mA)} = 11\ \Omega \tag{11}$$

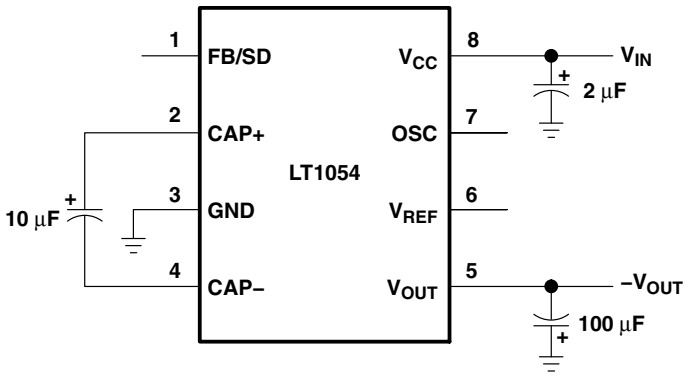
The resistor reduces the power dissipated by the LT1054 by (4.9 V)(100 mA) = 490 mW. The total power dissipated by the LT1054 is equal to (940 mW – 490 mW) = 450 mW. The junction-temperature rise is 58°C. Although commercial devices are functional up to a junction temperature of 125°C, the specifications are tested to a junction temperature of 100°C. In this example, this means limiting the ambient temperature to 42°C. To allow higher ambient temperatures, the thermal resistance numbers for the LT1054 packages represent worst-case numbers, with no heat sinking and still air. Small clip-on heat sinks can be used to lower the thermal resistance of the LT1054 package. Airflow in some systems helps to lower the thermal resistance. Wide printed circuit board traces from the LT1054 leads help remove heat from the device. This is especially true for plastic packages.



NOTE: Motor-Tach is Canon CKT26-T5-3SAE.
Pin numbers shown are for the P package.

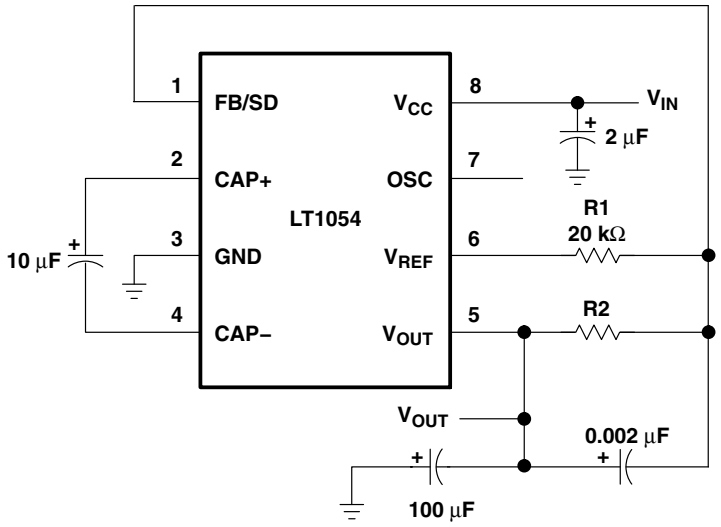
Figure 18. Motor-Speed Servo

APPLICATION INFORMATION



Pin numbers shown are for the P package.

Figure 19. Basic Voltage Inverter

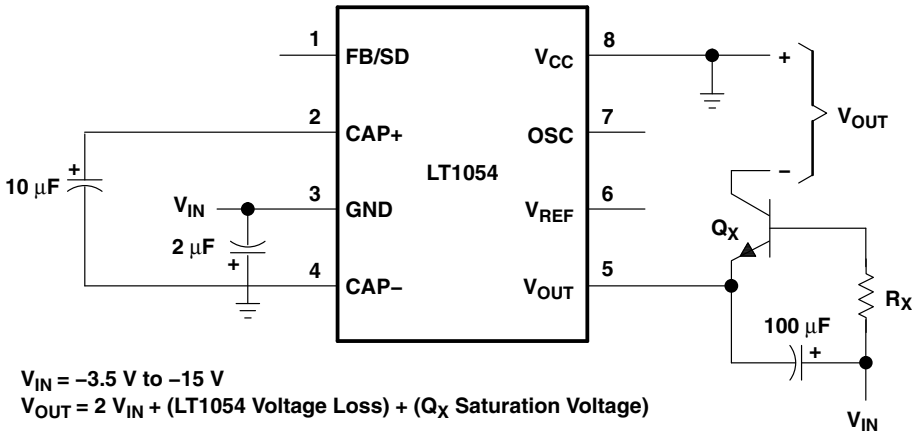


$$R2 = R1\left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40\ mV} + 1\right) = 20\ k\Omega\left(\frac{|V_{OUT}|}{1.21\ V} + 1\right)$$

Pin numbers shown are for the P package.

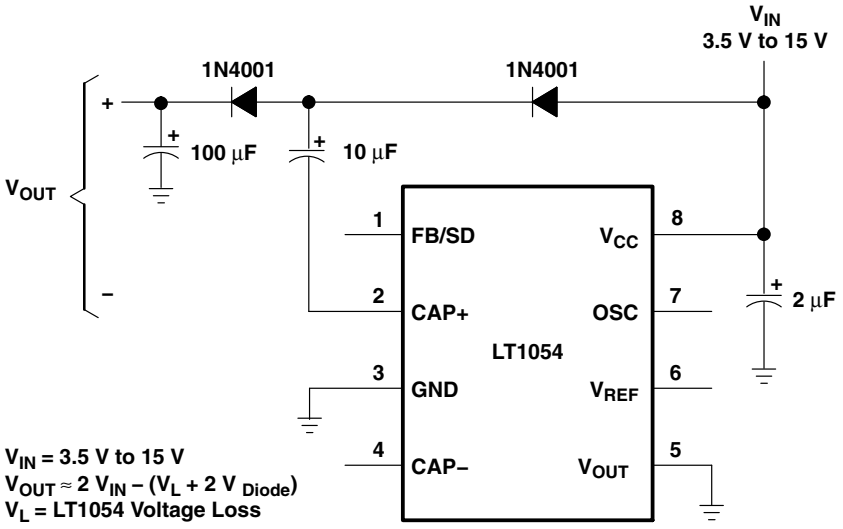
Figure 20. Basic Voltage Inverter/Regulator

APPLICATION INFORMATION



Pin numbers shown are for the P package.

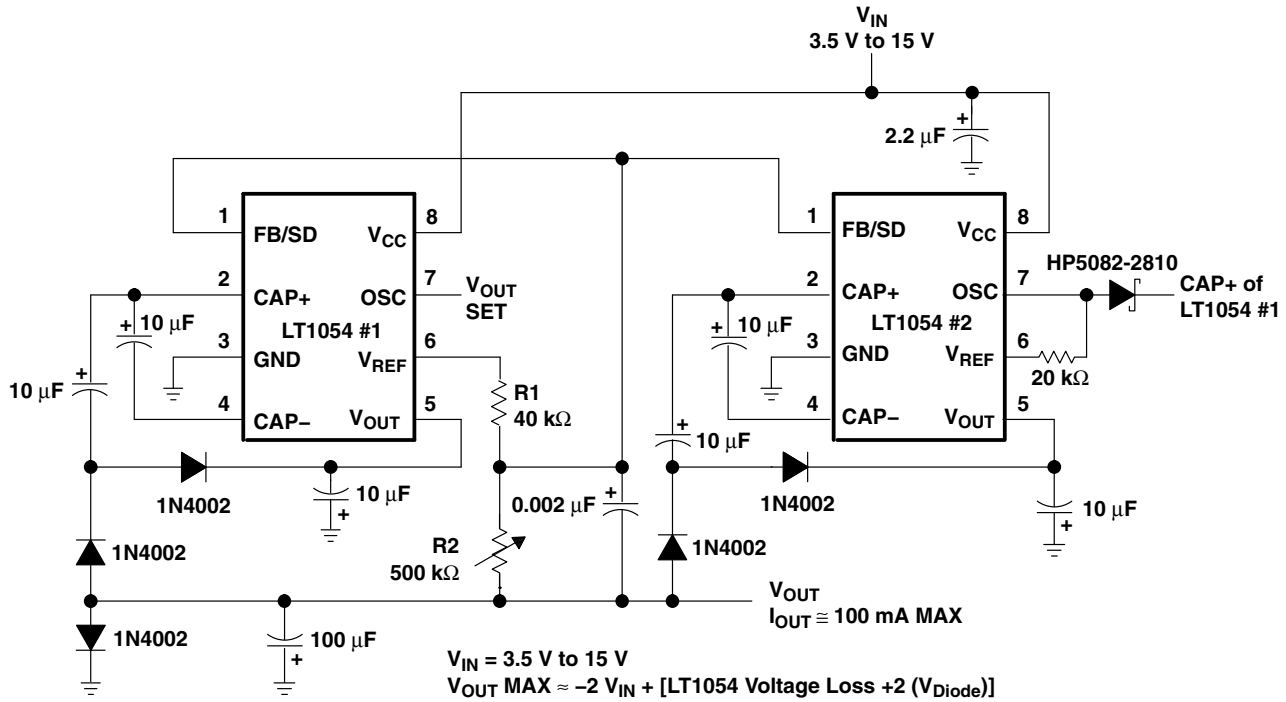
Figure 21. Negative-Voltage Doubler



Pin numbers shown are for the P package.

Figure 22. Positive-Voltage Doubler

APPLICATION INFORMATION



V_{IN} = 3.5 V to 15 V

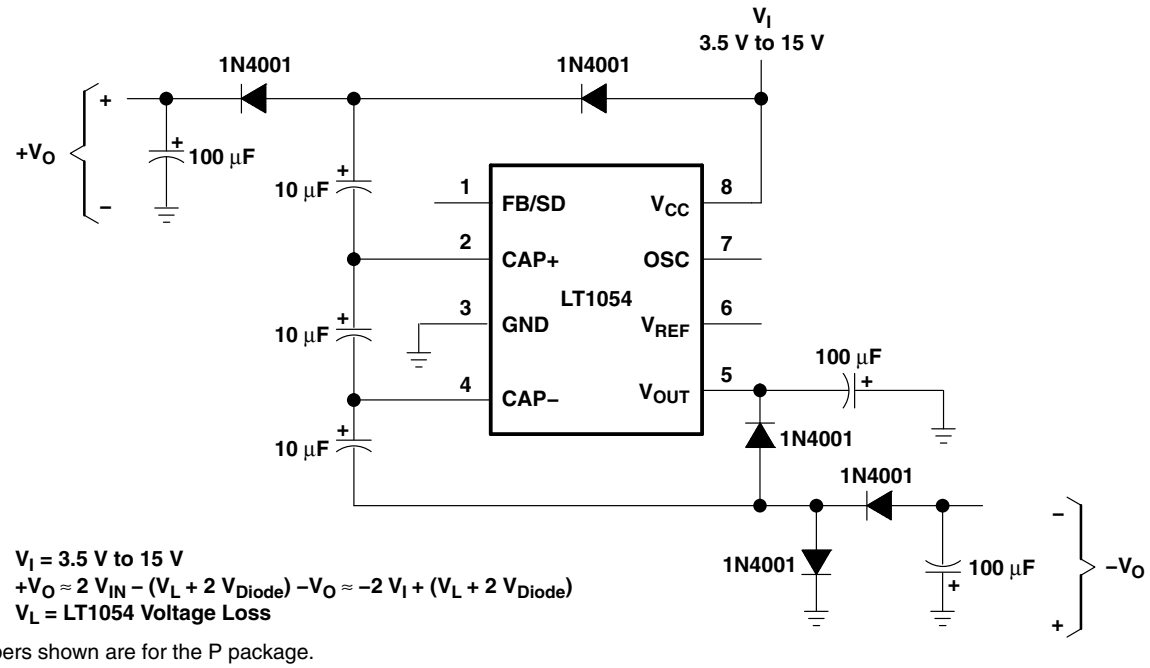
V_{OUT} MAX ≈ –2 V_{IN} + [LT1054 Voltage Loss +2 (V_{Diode})]

$$R2 = R1\left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40\ mV} + 1\right) = R1\left(\frac{|V_{OUT}|}{1.21\ V} + 1\right)$$

Pin numbers shown are for the P package.

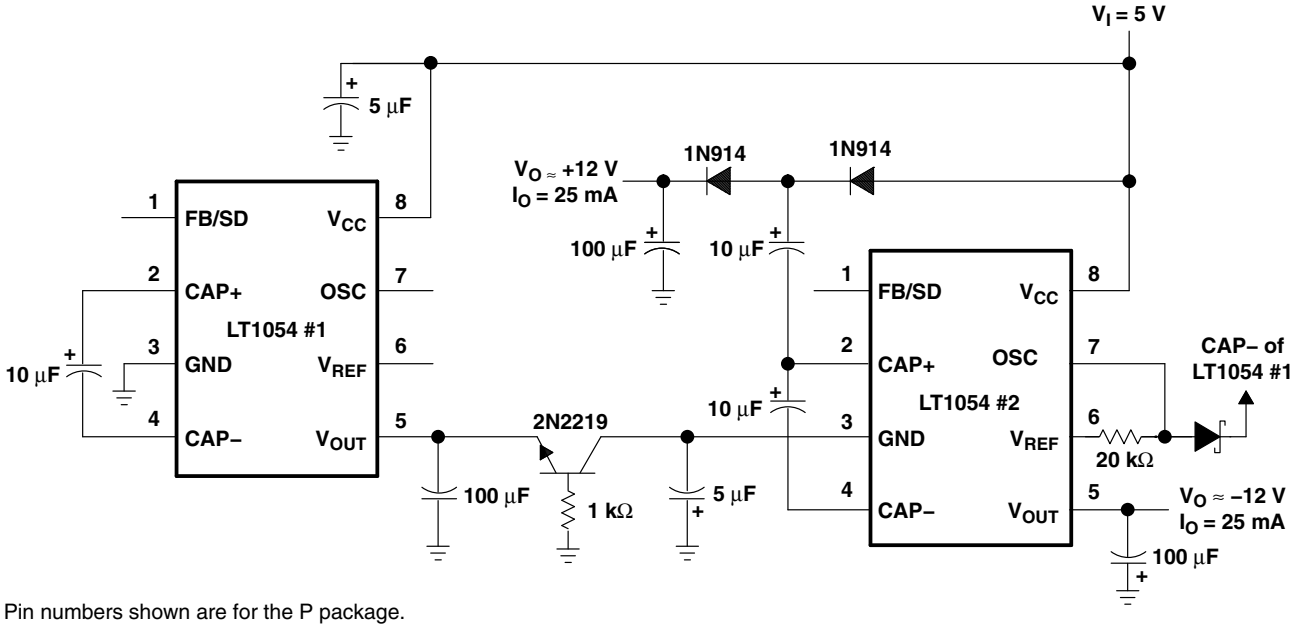
Figure 23. 100-mA Regulating Negative Doubler

APPLICATION INFORMATION



Pin numbers shown are for the P package.

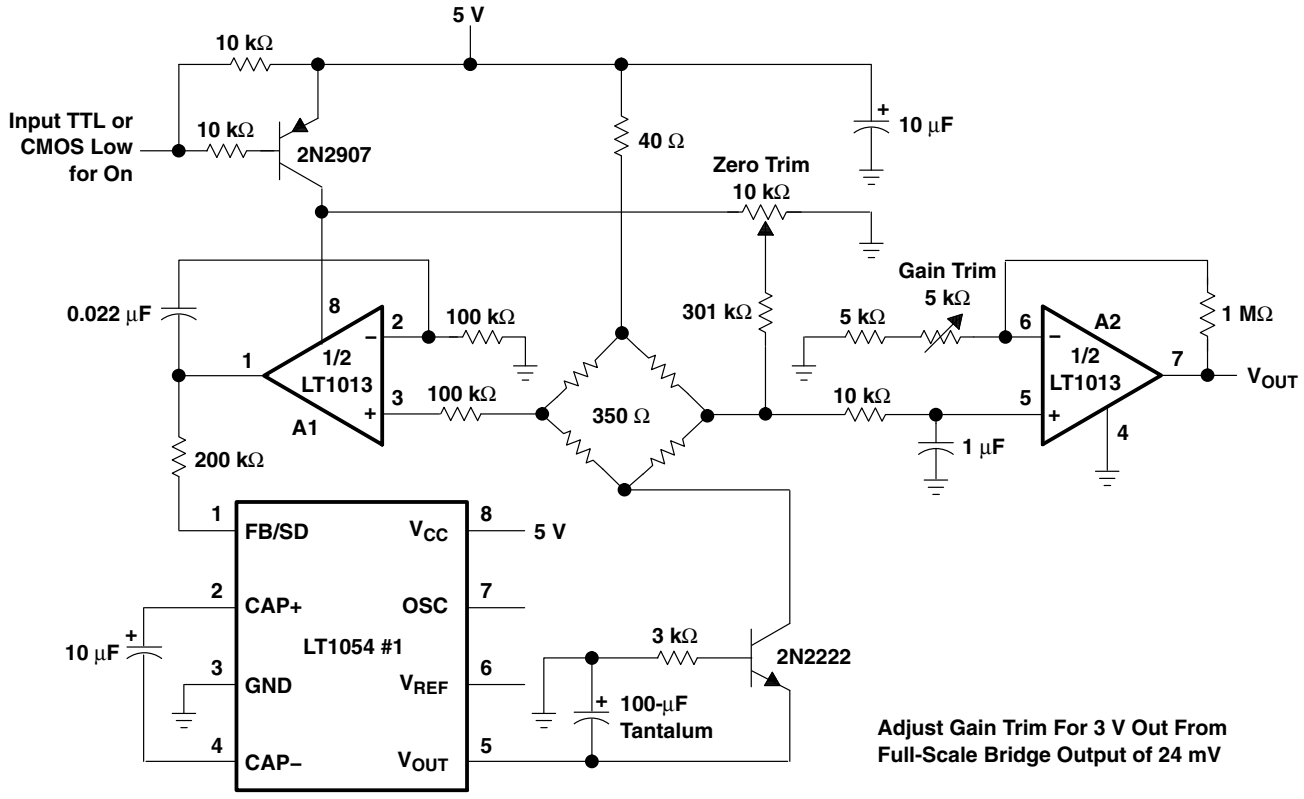
Figure 24. Dual-Output Voltage Doubler



Pin numbers shown are for the P package.

Figure 25. 5-V to ±12-V Converter

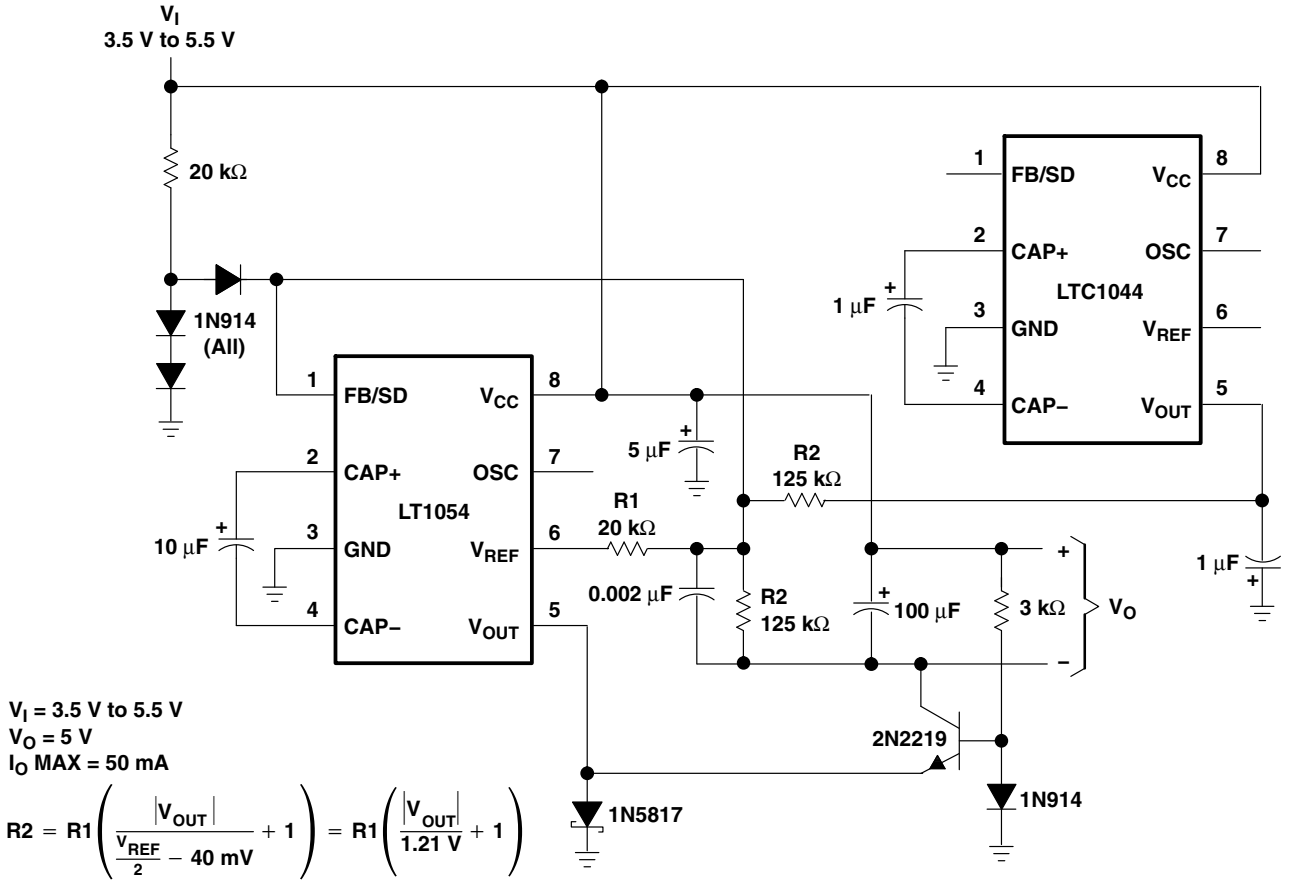
APPLICATION INFORMATION



Pin numbers shown are for the P package.

Figure 26. Strain-Gage Bridge Signal Conditioner

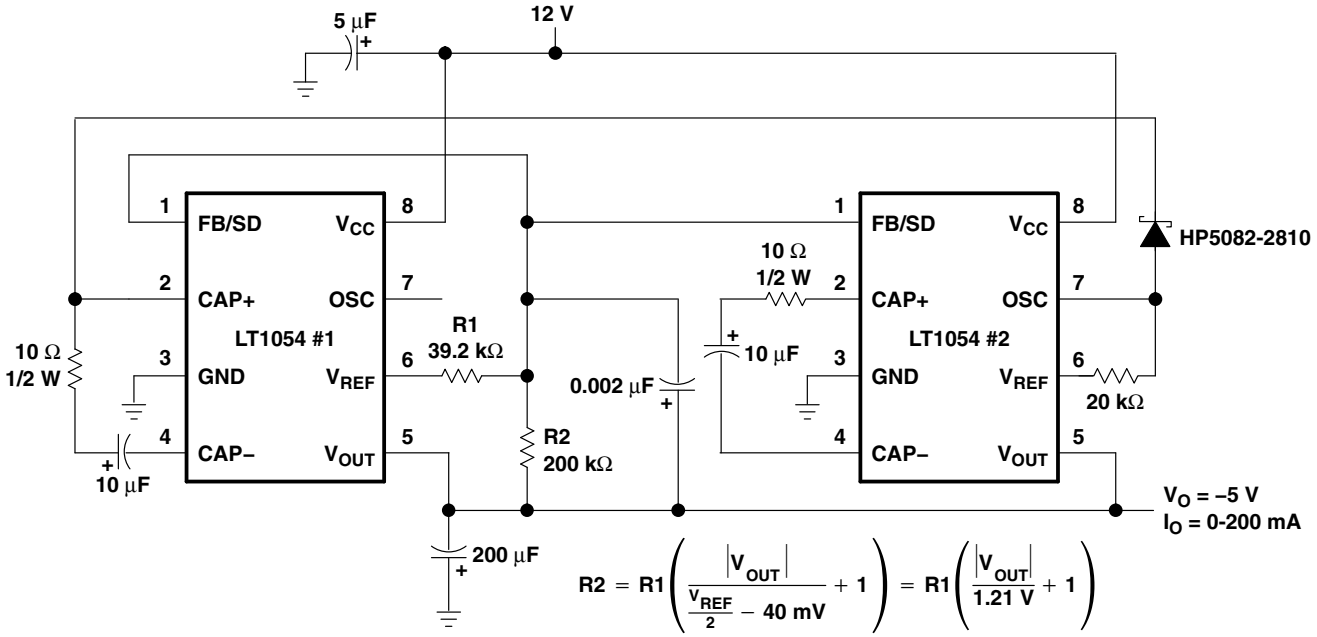
APPLICATION INFORMATION



Pin numbers shown are for the P package.

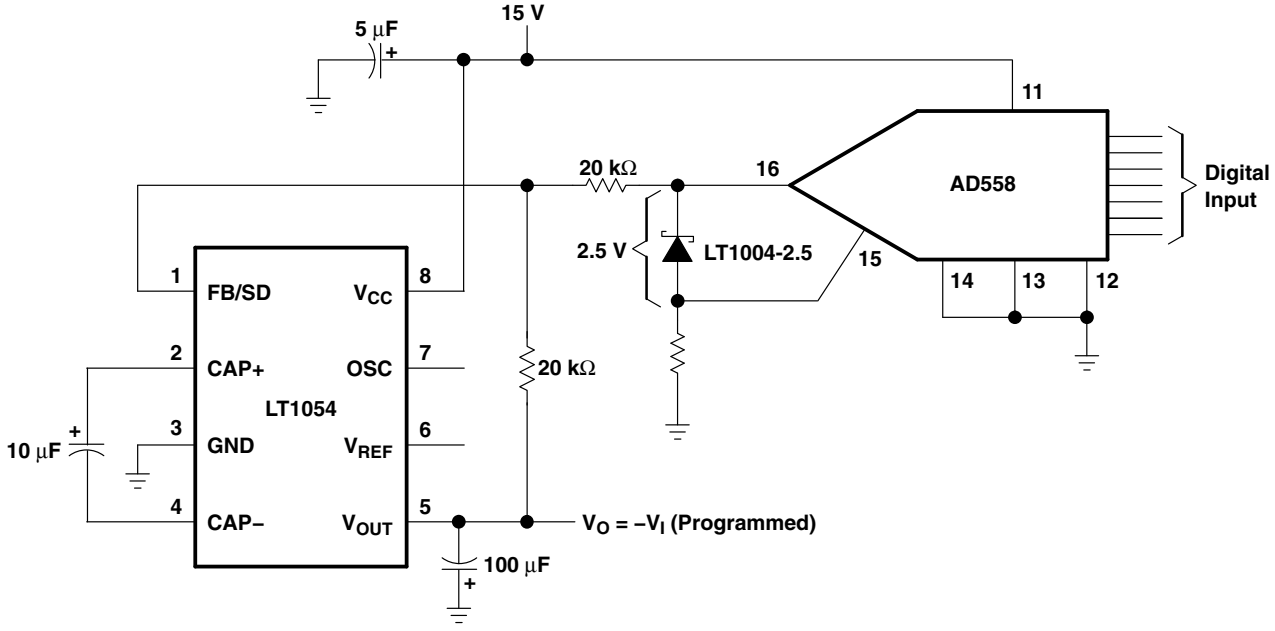
Figure 27. 3.5-V to 5-V Regulator

APPLICATION INFORMATION



Pin numbers shown are for the P package.

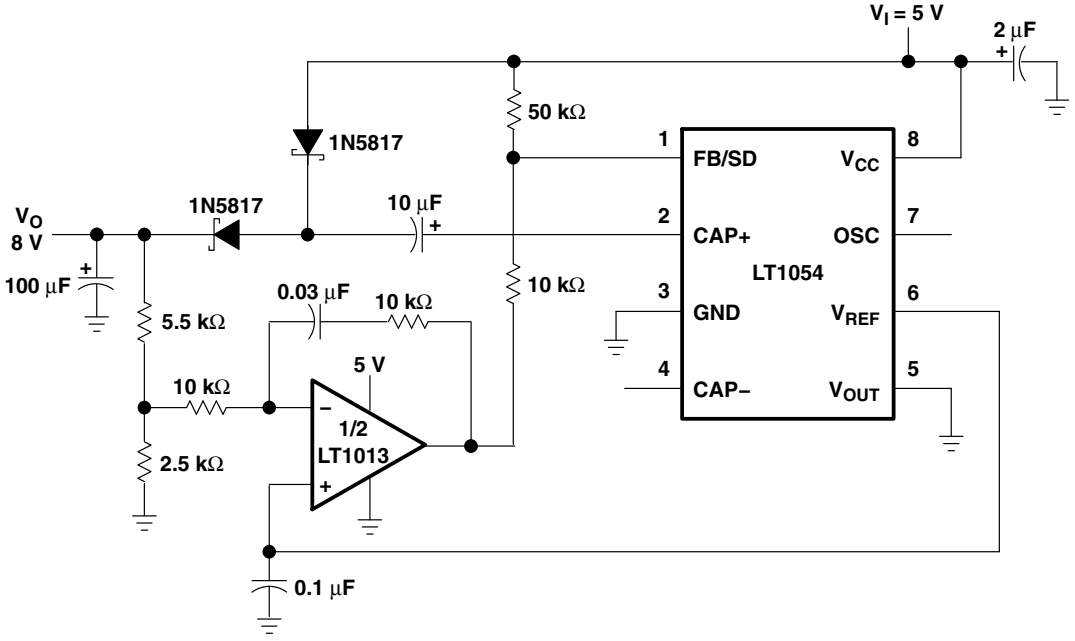
Figure 28. Regulating 200-mA +12-V to –5-V Converter



Pin numbers shown are for the P package.

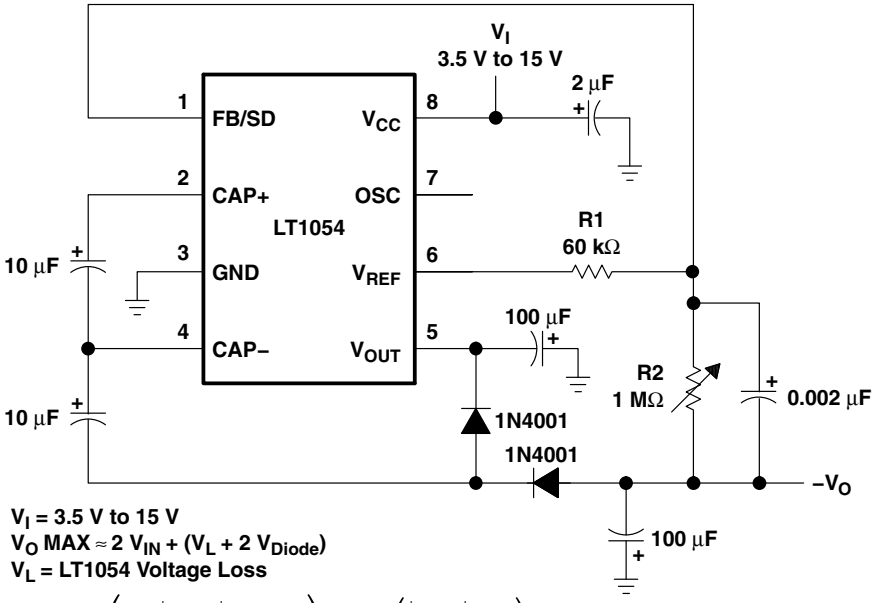
Figure 29. Digitally Programmable Negative Supply

APPLICATION INFORMATION



Pin numbers shown are for the P package.

Figure 30. Positive Doubler With Regulation (5-V to 8-V Converter)



V_I = 3.5 V to 15 V
V_O MAX ≈ 2 V_{IN} + (V_L + 2 V_{Diode})
V_L = LT1054 Voltage Loss

$$R2 = R1\left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40\ mV} + 1\right) = R1\left(\frac{|V_{OUT}|}{1.21\ V} + 1\right)$$

Pin numbers shown are for the P package.

Figure 31. Negative Doubler With Regulator

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LT1054CDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LT1054C	Samples
LT1054CDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LT1054C	Samples
LT1054CDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LT1054C	Samples
LT1054CDWRE4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LT1054C	Samples
LT1054CDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LT1054C	Samples
LT1054CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	LT1054CP	Samples
LT1054CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	LT1054CP	Samples
LT1054IDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LT1054I	Samples
LT1054IDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LT1054I	Samples
LT1054IDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LT1054I	Samples
LT1054IDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LT1054I	Samples
LT1054IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	LT1054IP	Samples
LT1054IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	LT1054IP	Samples
LT1054Y	OBSOLETE	DIESALE	Y	0		TBD	Call TI	Call TI			

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

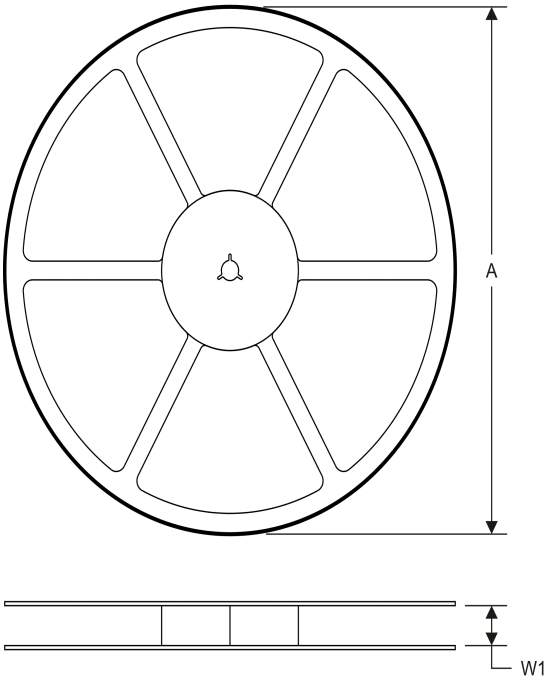
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

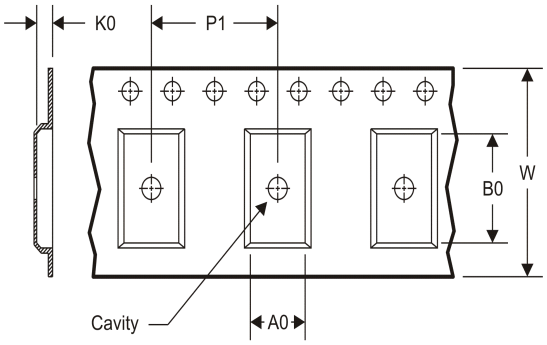
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



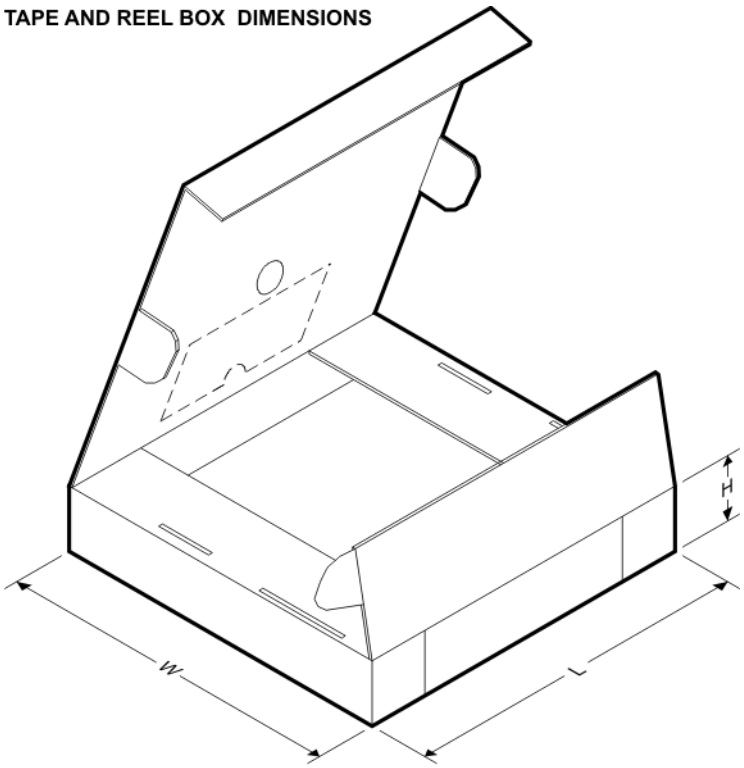
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LT1054CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
LT1054IDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

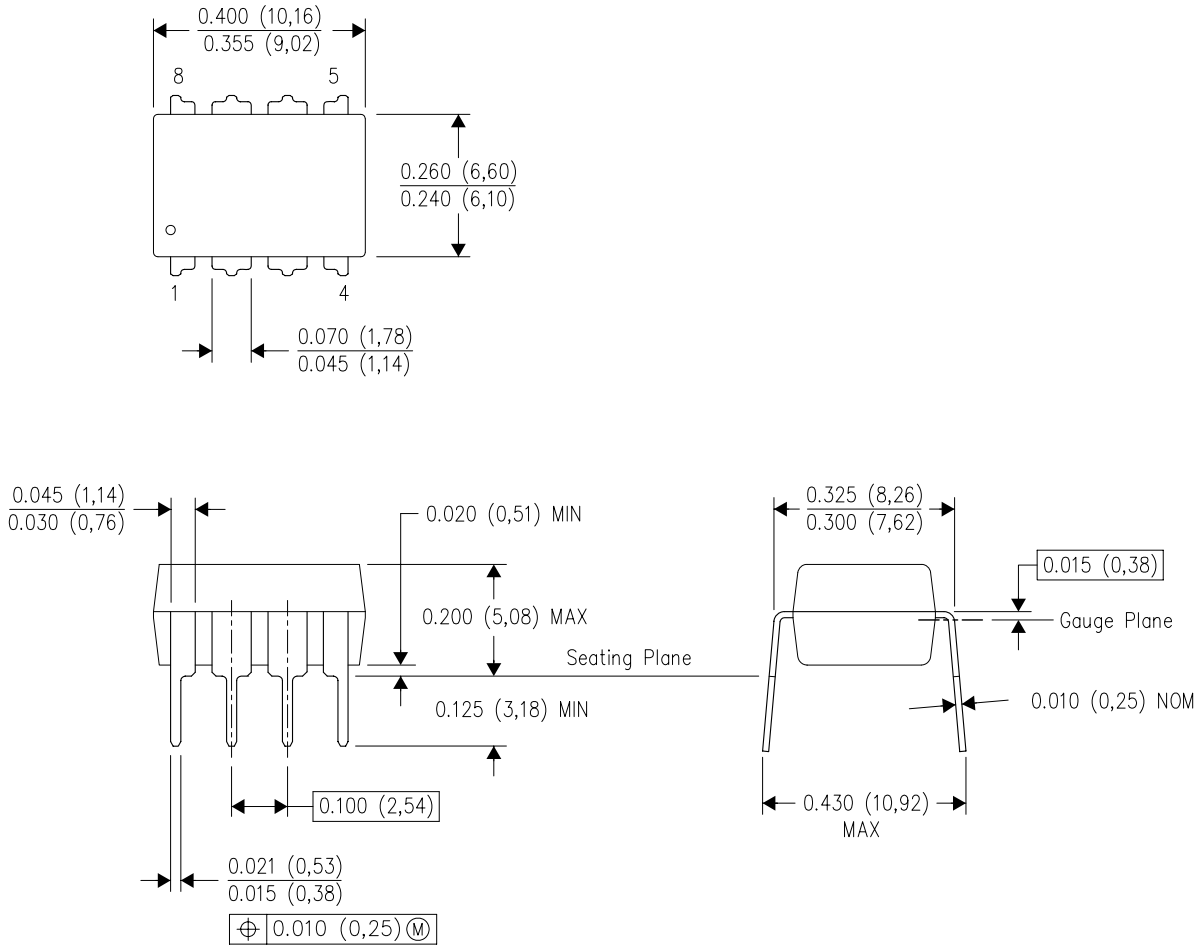
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

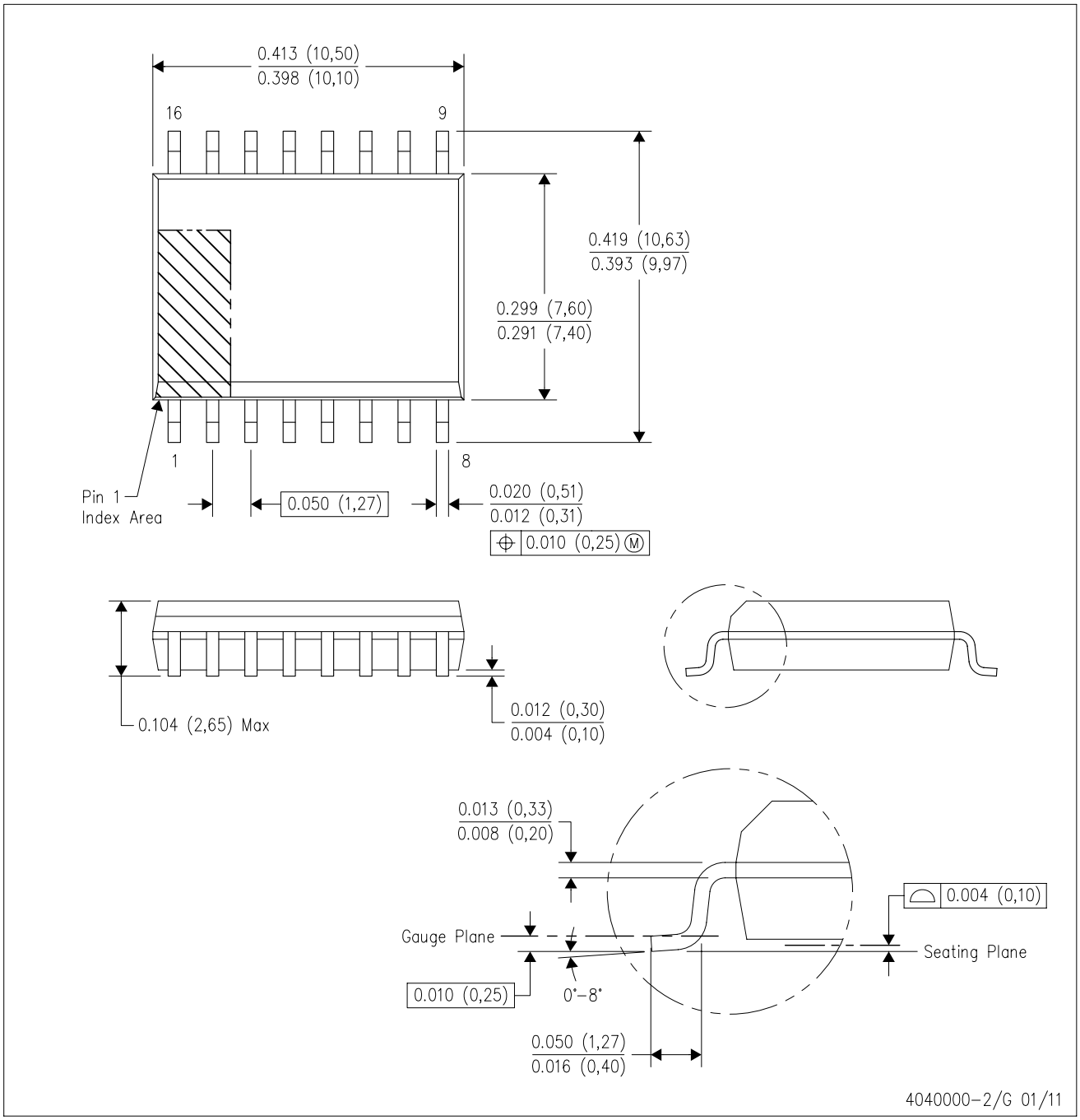
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LT1054CDWR	SOIC	DW	16	2000	367.0	367.0	38.0
LT1054IDWR	SOIC	DW	16	2000	367.0	367.0	38.0

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



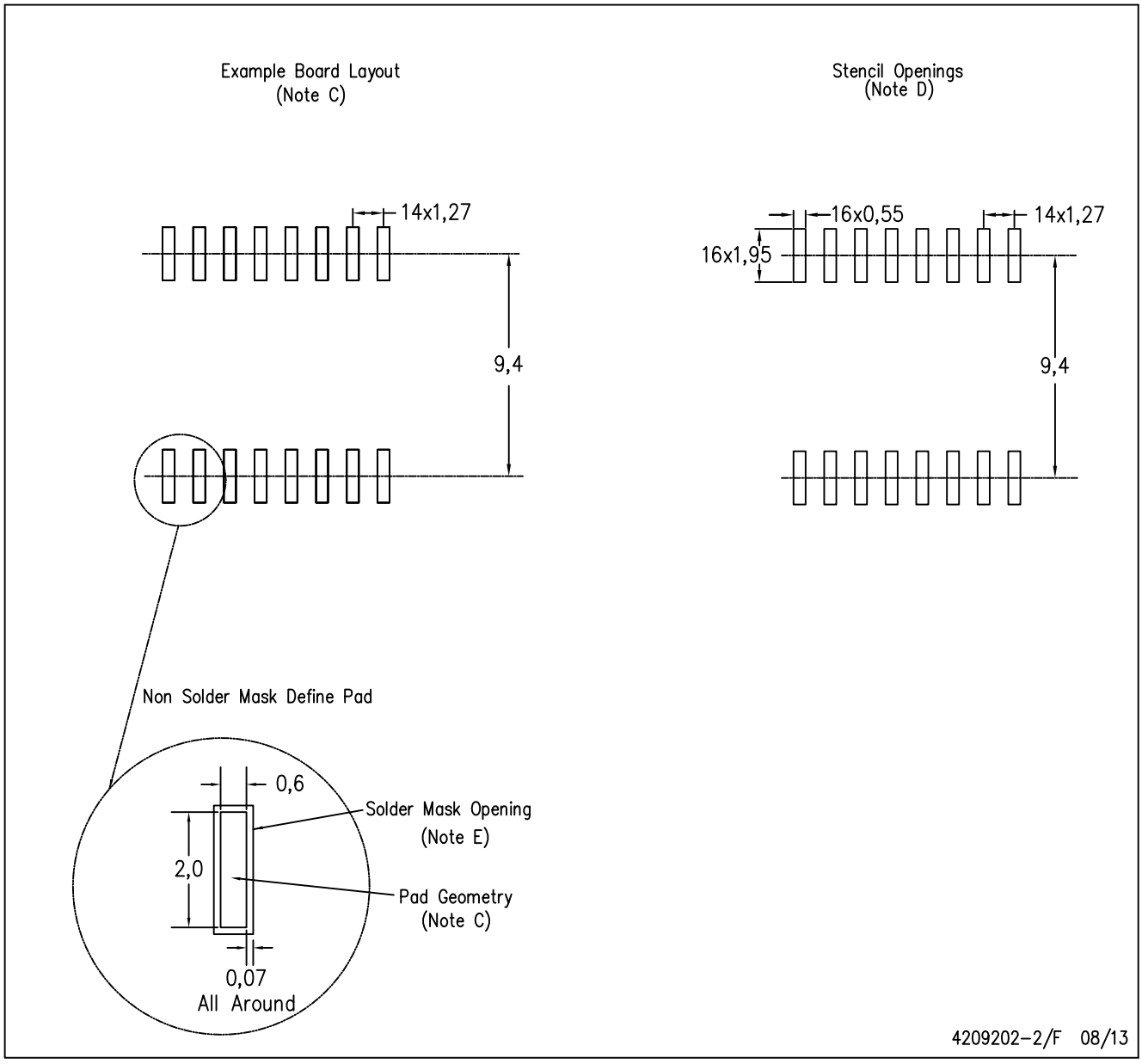
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AA.

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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