

MCZ5601SC

Driver IC

Feature

- Floating Channel for Bootstrap Operation to +600V
- Output Source / Sink Current : 400mA/400mA
- 3.3 V and 5 V input logic compatible
- Halogen free
- Pb free
- RoHS:Yes

Outline

House Name: SOP8J



1. 絶対最大定格

Absolute Maximum Ratings

以下、IN1,IN2=IN と省略する
Abridgement each as follows IN1,IN2=IN

1-1 入出力定格

Input Output Ratings

特に指定のない場合はTj=25°C
Tj=25°C unless otherwise specified.

項目 Item	記号 Symbol	規格値 Ratings	単位 Units
Vcc端子最大印加電圧 Vcc maximum applied voltage	Vcc	-0.3 ~ 22	V
IN端子最大印加電圧 IN maximum applied voltage	VIN	-0.3 ~ 6.0	V
VB端子最大印加電圧 VB maximum applied voltage	VB	-0.3 ~ 600	V
VS端子最大印加電圧 VS maximum applied voltage	VS	VB-22 ~ VB+0.3	V
VB-VS最大印加電圧 VB-VS maximum applied voltage	VBS	-0.3 ~ 22	V
HO端子最大印加電圧 HO maximum applied voltage	VHO	VS-0.3 ~ VB+0.3	V
dVS/dt 最大許容オフセット電圧 dVS/dt maximum offset voltage	dVS/dt	50	V/ns

注意：本仕様書に記載されていない項目、使用条件、論理の組み合わせでの使用は保証していません。

記載されている以外の条件で使用する場合は必ず事前に当社担当営業部門までご相談下さい。

記載内容は改良などのためにお断り無しに変更することがあります。

Notes：Using with parameters, condition of use and logic controls that are not specified in the specifications are not assured.

When used with the conditions that are not specified, please consult us in advance.

The contents described herein are subject to change without notice.

1-2 熱規格

Thermal Ratings

特に指定のない場合はVcc=VB=16V,VS=GND,Tj=25°C
Vcc=VB=16V, VS=GND and Tj=25°C unless otherwise specified.

項目 Item	記号 Symbol	規格値 Ratings	単位 Units
保存温度 Storage temperature	Tstg	-55 ~ 150	°C
接合部温度 Junction temperature	Tj	-40 ~ 150	°C
許容損失 Total power dissipation	Pd	1.5 (※1)	W
熱抵抗 Thermal Resistance	θ_{ja}	83.3 (※1)	°C/W

※1 ガラエポ基板:114.3mm×76.2mm、厚さ:1.6mm、内面銅箔サイズ:74.2mm×74.2mm、厚さ:35 μ m

Glass-Epoxy Board:114.3×76.2mm、Thickness:1.6mm、Inside copper foil:74.2mm×74.2mm、Thickness:35 μ m

5SK-175030-1

2 推奨動作条件

Recommended Operation Conditions

特に指定のない場合は $V_{CC}=V_B=16V, V_S=GND, T_j=25^{\circ}C$
 $V_{CC}=V_B=16V, V_S=GND$ and $T_j=25^{\circ}C$ unless otherwise specified.

項目 Item	記号 Symbol	推奨値 Recommended value			単位 Units
		min	typ	max	
動作温度 Operating temperature	$T_j(ope)$	-20	---	120	$^{\circ}C$
V_{CC} 端子印加電圧 V_{CC} applied voltage	V_{CC}	10	---	20	V
IN端子印加電圧 IN applied voltage	V_{IN}	0	---	5.5	V
VB端子印加電圧 VB applied voltage	V_B	V_S+10	---	V_S+20	V
VS端子印加電圧 VS applied voltage	V_S	0	---	500	V
VB-VS端子印加電圧 VB-VS applied voltage	V_{BS}	10	---	20	V
HO端子印加電圧 HO applied voltage	V_{HO}	V_S	---	V_B	V

注意 : 上記の規格範囲内においても、製品寿命に関しましてはお客様の使用環境により異なりますので、長寿命を期待される製品
 にご使用される場合には、 $T_j=105^{\circ}C$ 以下でご使用頂く事を推奨致します。

Notes : The product life depends on the condition of use even within the above operating conditions.
 Using at $T_j = 105^{\circ}C$ or less is recommended for the equipment where a long life is expected.

3 電気的特性

Electrical Characteristics

特に指定のない場合はV_{CC}=V_B=16V, V_S=GND, T_J=25°C
V_{CC}=V_B=16V, V_S=GND and T_J=25°C unless otherwise specified.

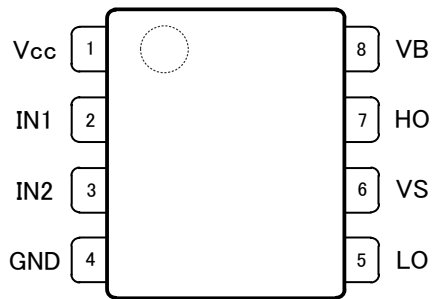
項目 Item	記号 Symbol	条件 Conditions	規格値 Ratings			単位 Units
			min	typ	max	
V _{CC} 起動電圧 V _{CC} start-up voltage	V _{CC_start}		8.50	9.00	9.50	V
V _{CC} 停止電圧 V _{CC} stop voltage	V _{CC_stop}		7.75	8.20	8.60	V
V _{CC} UVLOヒステリシス V _{CC} UVLO hysteresis voltage	V _{CC_UVLO_Δ}	Δ = V _{CC_start} - V _{CC_stop}	0.50	0.80	1.10	V
V _{CC} 消費電流 V _{CC} operating current	I _{CC}	IN1,2=0V	0.3	0.6	0.9	mA
V _B -V _S 起動電圧 V _B S start-up voltage	V _{B_S_start}		7.50	8.00	8.50	V
V _B -V _S 停止電圧 V _B S stop voltage	V _{B_S_stop}		6.70	7.20	7.70	V
V _B SUVLOヒステリシス V _B S UVLO hysteresis voltage	V _{B_S_UVLO_Δ}	Δ = V _{B_S_start} - V _{B_S_stop}	0.50	0.80	1.10	V
V _B S消費電流 V _B S operating current	I _{B_S}	IN1,2=0V	0.3	0.6	0.9	mA
ハイサイド最低動作電圧(※1) High side minimum operating voltage	V _{B_S_min}				5.0	V
ローサイド最低動作電圧(※1) Low side minimum operating voltage	V _{CC_min}				5.0	V
固定デッドタイム Dead time	DT		70	160	250	ns
ターンオン伝達遅延時間 Turn-on propagation delay time	ton	IN ↑ ~HO ↑, CL=1000pF	100	210	400	ns
ターンオフ伝達遅延時間 Turn-off propagation delay time	toff	IN ↓ ~HO ↓, CL=1000pF	100	195	400	ns
遅延時間差 propagation delay time	DM	(IN1 ↑ ~HO ↑)-(IN2 ↑ ~HO2 ↑) (IN1 ↓ ~HO ↓)-(IN2 ↓ ~HO2 ↓)	-50	0	50	ns
IN端子上側しきい値電圧 Input upper threshold voltage	V _{IH}		1.6	2.0	2.4	V
IN端子下側しきい値電圧 Input lower threshold voltage	V _{IL}		0.9	1.2	1.6	V
IN端子しきい値ヒステリシス電圧 Input threshold hysteresis voltage	V _{INhys}	V _{INhys} =V _{IH} -V _{IL}	0.4	0.8	1.2	V
IN端子抵抗値 Input terminal resistance	R _{IN}		240	400	560	kΩ
出力ソース電流 Output source current	I _{HO_H} I _{LO_H}	IN1=5V, HO-V _S =0V IN2=5V, LO-GND=0V	0.30	0.40	0.65	A
出力シンク電流 Output sink current	I _{HO_L} I _{LO_L}	IN1=0V, HO-V _S =16V IN2=0V, LO-GND=16V	-0.65	-0.40	-0.30	A
出力立上り時間(※1)(※2) Output rise time	tr	CL=1000pF		33		ns
出力立下がり時間(※1)(※2) Output fall time	tf	CL=1000pF		30		ns

(※1)設計保証

Design assurance.

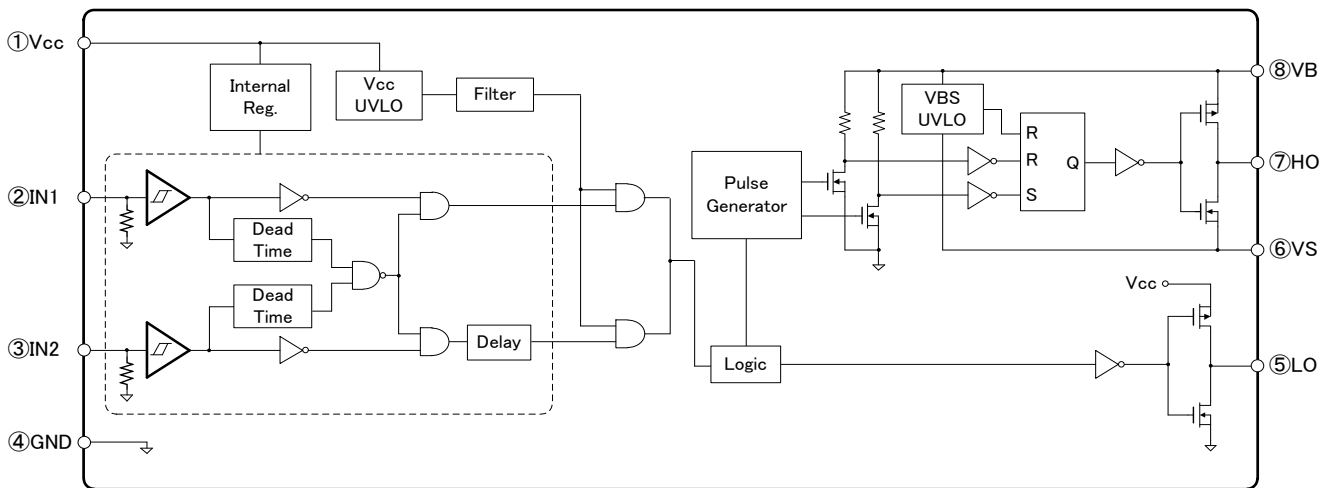
(※2)V_{CC}=16V(10%→1.6V, 90%→14.4V)

4 端子配置および端子機能
Pin Assignment & Pin Function



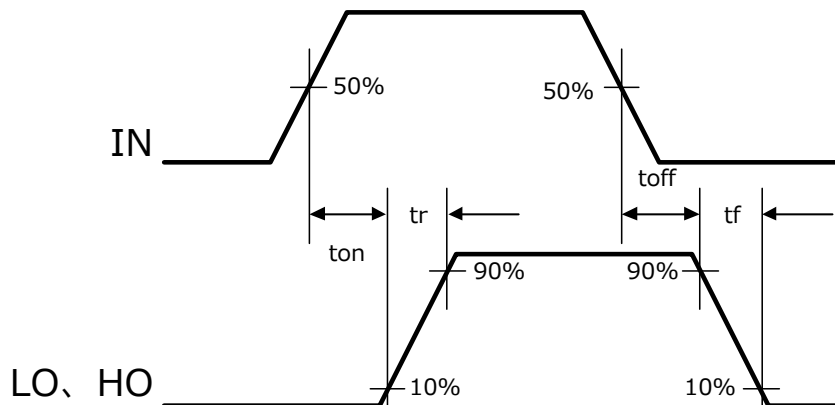
端子番号 Pin No.	端子名 Name	機能 Function
1	Vcc	電源端子 Input terminal for power supply
2	IN1	入力端子1 Input1 terminal
3	IN2	入力端子2 Input2 terminal
4	GND	GND端子 Ground terminal
5	LO	ドライバ2出力端子 Driver2 output terminal
6	VS	ドライバ1基準端子 Driver1 ground terminal
7	HO	ドライバ1出力端子 Driver1 output terminal
8	VB	ドライバ1電源端子 Driver1 input terminal for power supply

5 ブロック図
Block Diagram



6 タイミングチャートおよび真理値表
Timing diagram & Truth table

6-1 タイミングチャート
Timing diagram



6-2 真理値表
Truth table

IN1	IN2	V _{CC}	V _{BS}	HO	LO
-	-	L	L	L	L
-	-	L	H	L	L
-	L	H	L	L	L
L	L	H	H	L	L
L	H	H	L	L	H
L	H	H	H	L	H
H	L	H	H	H	L
H	H	H	L	L	L
H	H	H	H	L	L

V_{CC}(V_{BS}):『H』は、V_{CC}(V_{BS})がV_{CC_start}(V_{BS_start})以上、またはV_{CC_stop}(V_{BS_stop})以上 (UVLO解除後)
V_{CC}(V_{BS}):『L』は、V_{CC}(V_{BS})がV_{CC_stop}(V_{BS_stop})以下、またはV_{CC_start}(V_{BS_start})以下 (UVLO解除前)

UVLO解除後: V_{CC_start}(V_{BS_start})以上の電圧印加をした状態

UVLO解除前: 起動時、またはUVLO解除後に、V_{CC_stop}(V_{BS_stop})以下の電圧印加をした状態

V_{CC}(V_{BS}):『H』 is the case where V_{CC}(V_{BS}) is V_{CC_start}(V_{BS_start}) or more, or more than V_{CC_stop}(V_{BS_stop}) (After UVLO is released.)

V_{CC}(V_{BS}):『L』 is the case where V_{CC}(V_{BS}) is V_{CC_stop}(V_{BS_stop}) or less, or less than V_{CC_start}(V_{BS_start}). (Before UVLO is released.)

After UVLO release: In a state where a voltage of V_{CC_start}(V_{BS_start}) or more is applied.

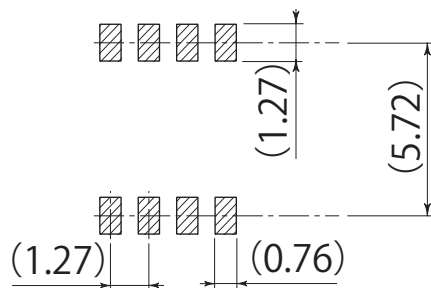
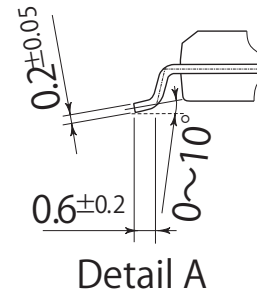
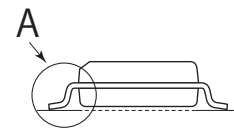
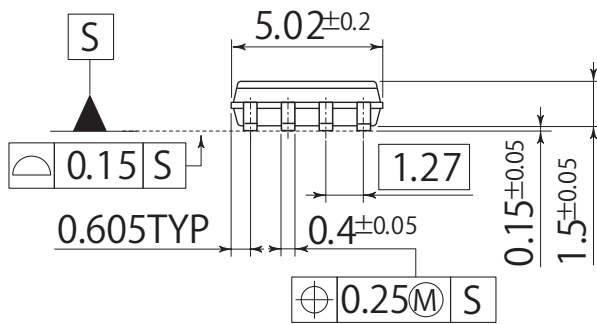
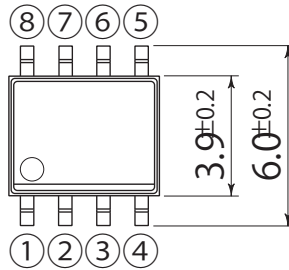
Before UVLO release: At the time of startup or after UVLO released, a state in which a voltage of V_{CC_stop} (V_{BS_stop}) or less is applied.

Package Outline-Dimensions

unit : mm
scale: 4/1

L2

JEDEC Code	-
JEITA Code	-
House Name	SOP8J



Referential Soldering Pad

- 量産時には、適正化を図って下さい
- Optimize soldering pad to the board design and soldering condition.

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