

DM413

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3-CHANNEL CONSTANT CURRENT LED DRIVERS WITH PROGRAMMABLE PWM OUTPUTS



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3-CHANNEL CONSTANT CURRENT LED DRIVERS WITH PROGRAMMABLE PWM OUTPUTS

General Description

DM413 is a PWM enabled LED driver specifically designed for LED lighting or display applications. It incorporates shift registers, data latches, 3-channel constant current circuitry with current value set by 3 external resistors, and built-in oscillator for PWM functioning. Data and clock buffer outputs are designed for cascading another chip. Additionally the Output Polarity Reverse function is designed to adapt to more high power LED applications.

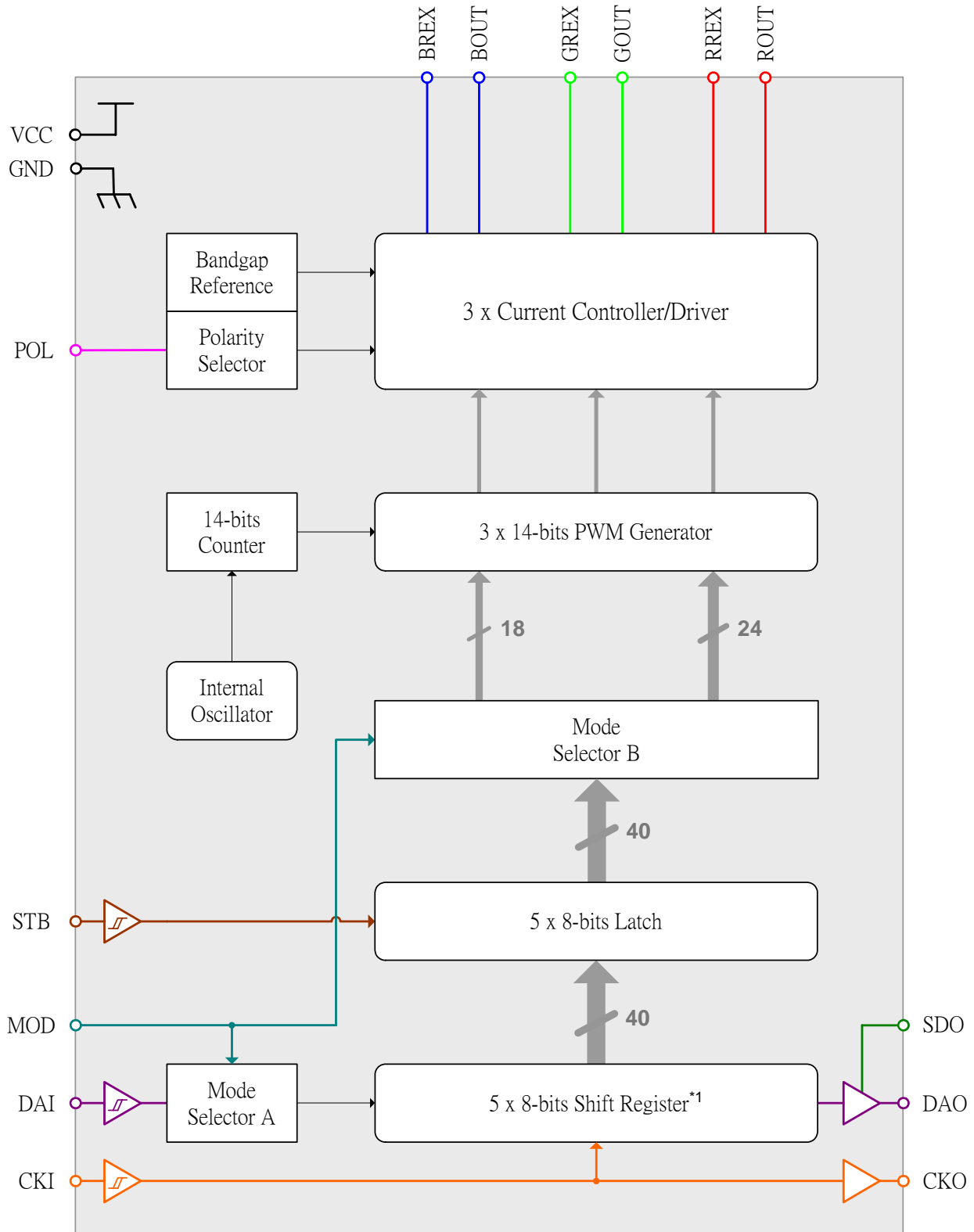
Features

- Maximum constant current outputs: 100mA determined by three external resistors
- Maximum sinking output voltage: 17V
- Maximum serial-in clock frequency: 20 MHz
- Built-in buffers for cascading clock and data to next driver
- PWM free-running capability (refresh rate (~ 400 Hz) with internal oscillator (~ 6.5 MHz))
- Selectable modes for PWM control:
 - ◆ 8-bits luminance data with PWM current outputs (8 bits mode)
 - ◆ 8-bits luminance data and 6-bits global brightness data (14 bits mode)
 - ◆ 8-bits luminance data and 5-bits individual color correction data (13 bits mode)
- Output polarity reverse function
- TTL/CMOS compatible input

Applications

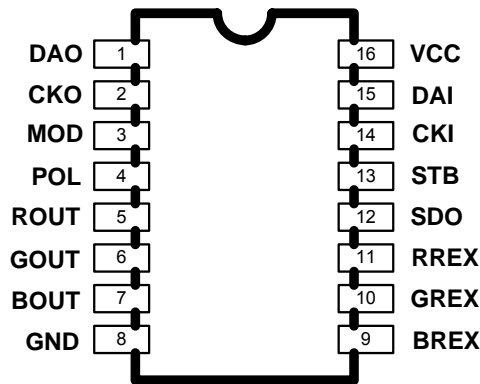
- LED Decorative Lighting
- Indoor/Outdoor LED Video or Message Display
- PWM Signal Generator

Block Diagram



*1 For 13-bits/5byte mode. For 14-bits/4byte mode, there are 4 x 8-bits S-Rs. For 8-bits/3byte mode, there are 3 x 8-bits S-Rs.

Pin Connection



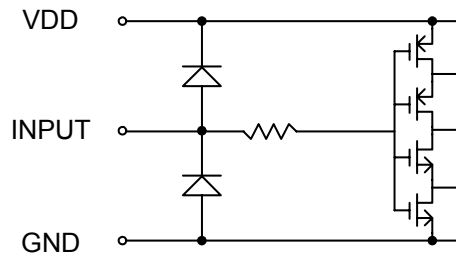
Pin Description

PIN No.	PIN NAME	FUNCTION
1	DAO	Serial data output terminal.
2	CKO	Clock output terminal.
3	MOD	Input mode selection: 'H' for 13bits/5byte mode, 'L' for 14bits/4byte mode, 'Floating' ^{*1} for 8bits/3byte mode.
4	POL	PWM current output polarity selection: 'H' for positive polarity, 'L' for negative polarity.
5~7	R(G、B)OUT	Sink constant current outputs (open-drain).
8	GND	Ground terminal.
9~11	R(G、B)REX	External resistors connected between REXTR(G、B) and GND for driver current value setting.
12	SDO	Serial data output trigger mode selection: 'H' means data is shifted out on synchronization to falling edge of CKO, 'L' means data is shifted out on synchronization to rising edge of CKO.
13	STB	Input terminal of data strobe: 'H' means data is latched, 'L' means data on shift register goes through latch (level latch).
14	CKI	Synchronous clock input terminal for serial data transfer. Data is sampled at the rising edge of CKI.
15	DAI	Serial data input terminal.
16	VCC	Power supply terminal.

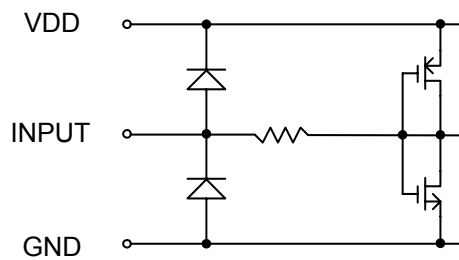
^{*1} When choosing "floating" mode, a capacitor (>100pF) should be connected between MOD and GND.

Equivalent Circuit of Inputs and Outputs

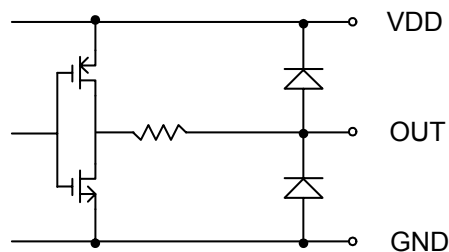
1. CKI, DAI, STB, SDO terminals



2. MOD, POL terminals



3. CKO, DAO terminal



Maximum Ratings (Ta=25°C, Tj(max) = 140°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	VDD	-0.3 ~ 7.0	V
Input Voltage	VIN	-0.3 ~ VDD+0.3	V
Output Current	IOUT	110	mA
Output Voltage	VOUT	-0.3 ~ 17	V
Input Clock Frequency	FCKI	25	MHz
GND Terminal Current	IGND	330	mA
Power Dissipation	PD	0.82 (SSOP16 : Ta=25°C) 0.86 (SOP16 : Ta=25°C)	W
Thermal Resistance	Rth(j-a)	115.9 (SSOP16) 110.9 (SOP16)	°C/W
Operating Temperature	Top	-40 ~ 85	°C
Storage Temperature	Tstg	-55 ~ 150	°C

Recommended Operating Condition

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	VDD	—	3.3	5.0	5.5	V
Output Voltage	VOUT	Driver On *1	1.0	—	10	V
Output Voltage	VOUT	Driver Off *2	—	—	17	
Output Current	IO	OUT (R, G, B)	5	—	100	mA
	IOH	SERIAL-OUT	—	—	1.5	
	IOL		—	—	-10	
Input Voltage	VIH	VDD = 3.3 V ~ 5.5V	min{2.0 or 0.8VDD}	—	VDD	V
	VIL		0.0	—	max{0.8 or 0.2VDD}	
Input Clock Frequency	FCKI	Single Chip Operation	—	—	20M	Hz
STB Pulse Width	tw STB	VDD = 3.3 V ~ 5.5V	20	—	—	ns
CKI Pulse Width	tw CLK		20	—	—	
Set-up Time for DAI	tsetup(D)		25	—	—	
Hold Time for DAI	thold(D)		25	—	—	
Set-up Time for STB	tsetup(L)		20	—	—	
Internal Oscillator Frequency	FOSC		5.2	6.5	7.8	

*1 Notice that the power dissipation is limited to its package and ambient temperature.

*2 The driver output voltage including any overshoot stress has to be compliant with the maximum voltage (17V).

Electrical Characteristics (VDD = 5.0 V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage "H" Level	VIH	TTL/CMOS logic level	min{2.0 or 0.8VDD}	—	VDD	V
Input Voltage "L" Level	VIL	TTL/CMOS logic level	GND	—	max{0.8 or 0.2VDD}	
Output Leakage Current	IOL	VOH = 17 V	—	—	1.0	uA
Output Voltage (S-OUT)	VOL	IOL = 10 mA	—	—	0.2	V
	VOH	IOH = -1.5 mA	VDD-0.2	—	—	
Output Current Skew (Channel-to-Channel) *1	IOL1	VOUT = 1.0 V REX = 120 Ω	—	±0.5	±1	%
Output Current Skew (Chip-to-Chip) *2	IOL2		4.5	5	5.5	mA
Output Voltage Regulation	% / VOUT	REX = 120 Ω VOUT = 1 V ~ 3 V	—	0.1	0.5	% / V
Supply Voltage Regulation	% / VDD	REX = 120 Ω	—	—	2	
Supply Current *3	I _{DD} (analog)	VOUT = 1.0 V REX = 6 Ω all outputs turn on	—	1.9	—	mA
	I _{DD} (digital)	CKI = 20MHz	—	1.6	—	

*1 Channel-to-channel skew is defined as the ratio between (any I_{out} – average I_{out}) and average I_{out}, where average I_{out} = (I_{max} + I_{min}) / 2.

*2 Chip-to-Chip skew is defined as the range into which any output current of any IC falls.

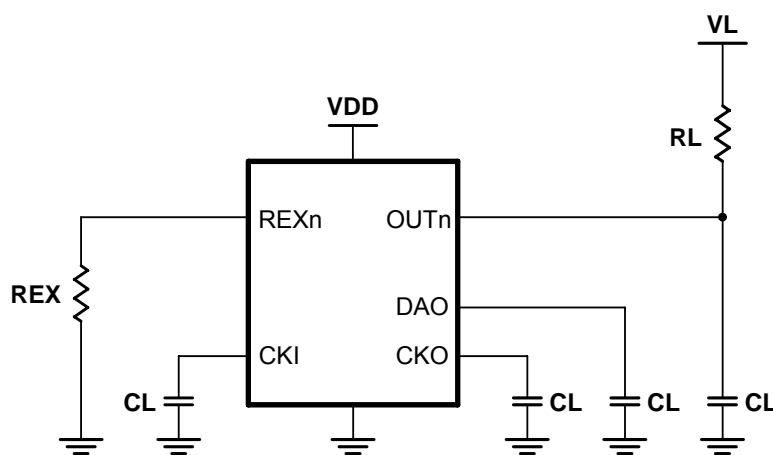
*3 IO excluded.

Switching Characteristics (VDD = 5.0V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay (‘L’ to ‘H’)	CKI-to-CKO	tpLH	VIH = VDD VIL = GND REXs = 33 Ω VL = 5.0 V RL = 180 Ω CL = 13 pF	—	6.0	—	ns
	CKO-to-DAO (SDO = ‘L’)			—	7.8	—	
Propagation Delay (‘H’ to ‘L’)	CKI-to-CKO	tpHL		—	7.0	—	
	CKO-to-DAO (SDO = ‘H’)			—	3.6	—	
Output Current Rise Time		tor		—	7.2	—	
Output Current Fall Time		tof		—	17.5	—	
Output Current (Propagation Delay after STB low)		top ^{*1}	—	—	3	ms	

Switching Characteristics (VDD = 4V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay (‘L’ to ‘H’)	CKI-to-CKO	tpLH	VIH = VDD VIL = GND REXs = 33 Ω VL = 5.0 V RL = 180 Ω CL = 13 pF	—	9.0	—	ns
	CKO-to-DAO (SDO = ‘L’)			—	13.2	—	
Propagation Delay (‘H’ to ‘L’)	CKI-to-CKO	tpHL		—	9.2	—	
	CKO-to-DAO (SDO = ‘H’)			—	7.0	—	
Output Current Rise Time		tor		—	32.5	—	
Output Current Fall Time		tof		—	23.5	—	
Output Current (Propagation Delay after STB low)		top ^{*1}	—	—	3	ms	



Switching Characteristics Test Circuit

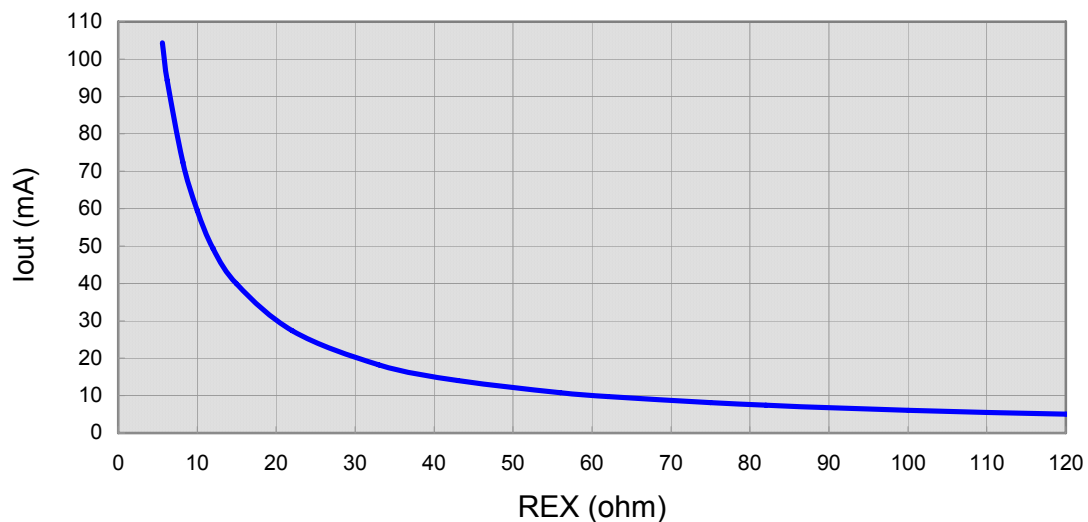
^{*1} Reload the new PWM data at the end of the front PWM frame.

Constant-Current Output

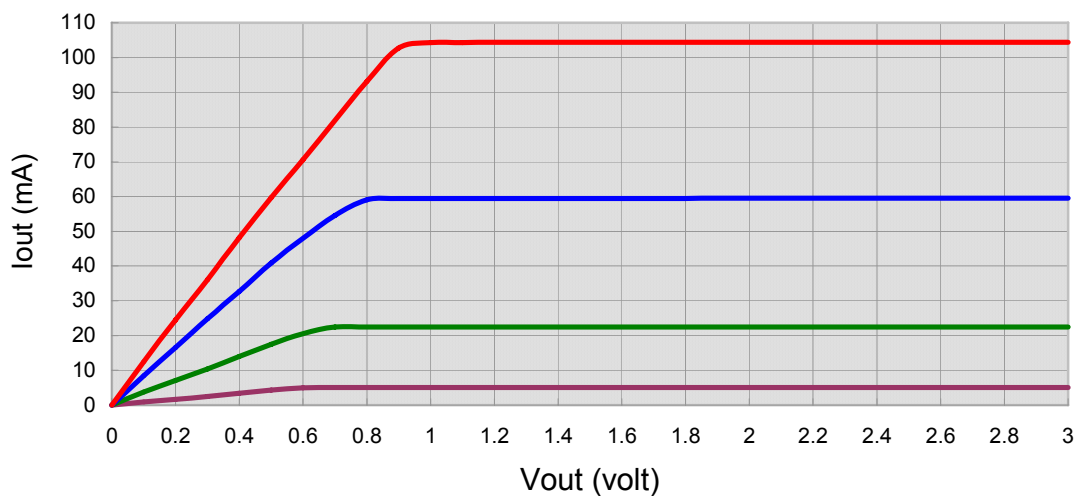
Constant-current value of each output channel is set by an external resistor connected between the R(G · B)REX pin and GND individually. Varying the resistor value can adjust the current scale ranging from 5mA to 100mA. The output current value is calculated roughly by the following equation:

$$I_{out}(mA) \approx \frac{0.6 V}{R_{EX} (ohm)} \times 1000$$

Output Current as a Function of REX value

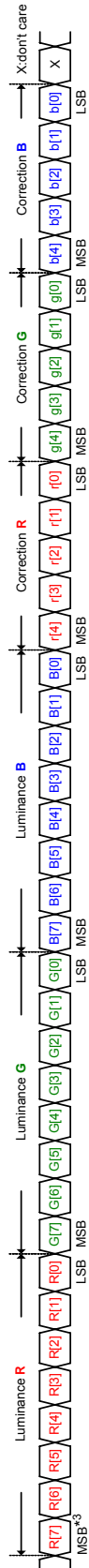


Output Current as a Function of Output Voltage

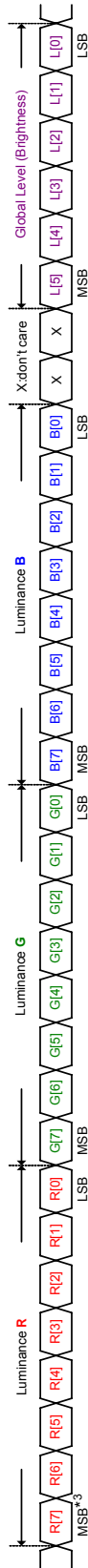


Data Format

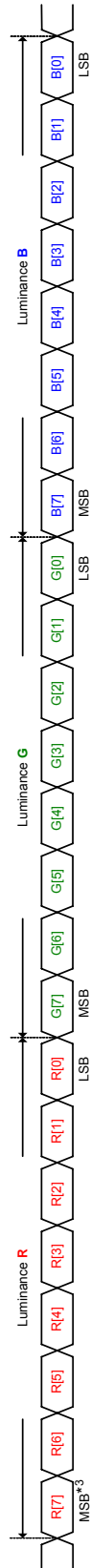
Active clocks per frame*1 = $Luminance[7:0] \times (Correction[4:0]^2 + 33)$



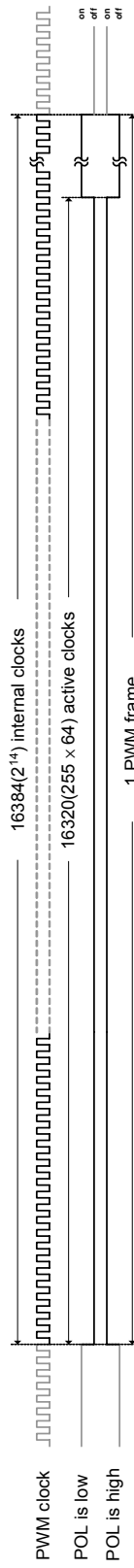
Active clocks per frame*1 = $Luminance[7:0] \times (Global Level[5:0] + 1)$



Active clocks per frame*1 = $Luminance[7:0] \times 64$



*1 Example for the maximum active clocks : $(Luminance [1,1,1,1,1,1,1,1] \times Brightness [1,1,1,1,1,1])$

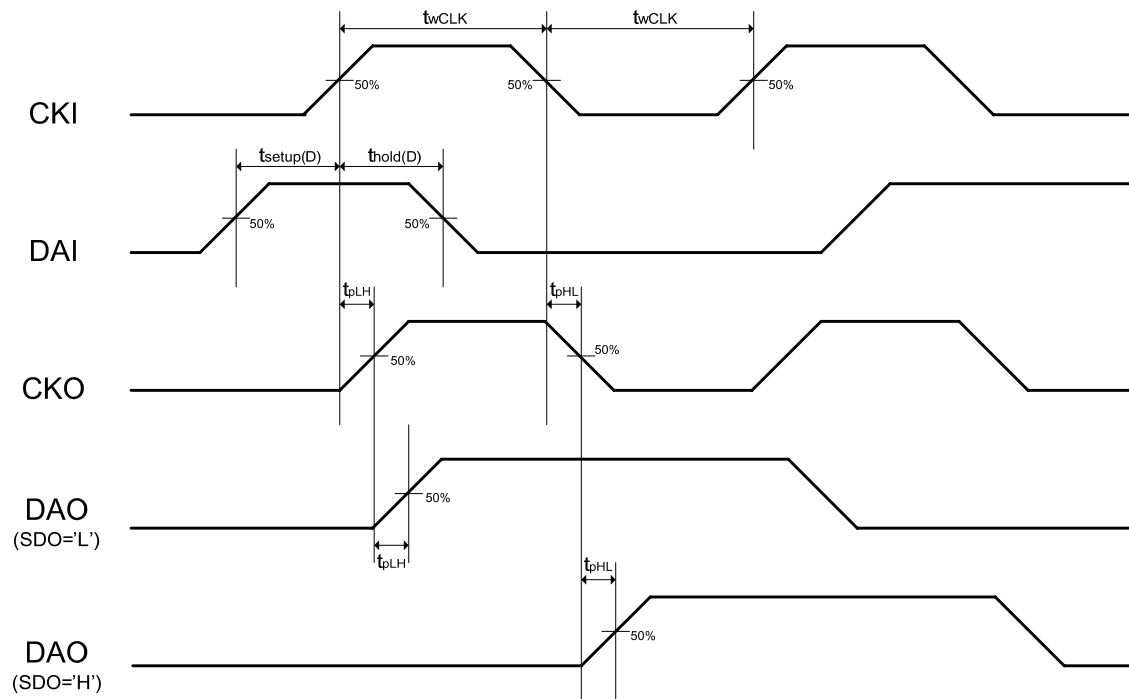


*2 Correction R(G · B) is correlated with Luminance R(G · B).

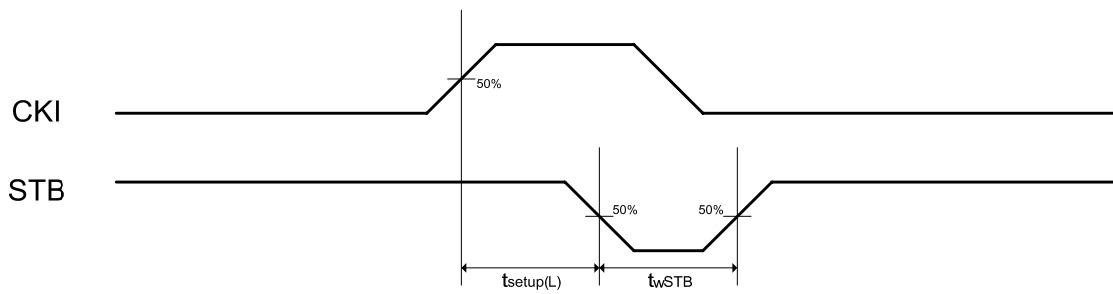
*3 The MSB, R[7], is the first serial input bit in all modes.

Timing Diagram

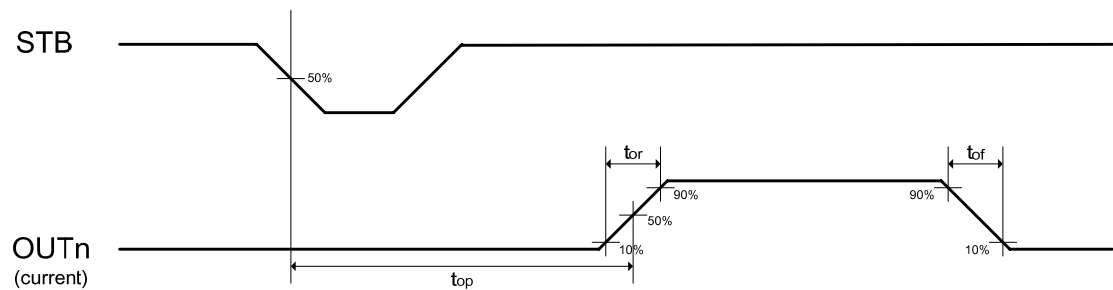
1. CKI-DAI, CKO, DAO



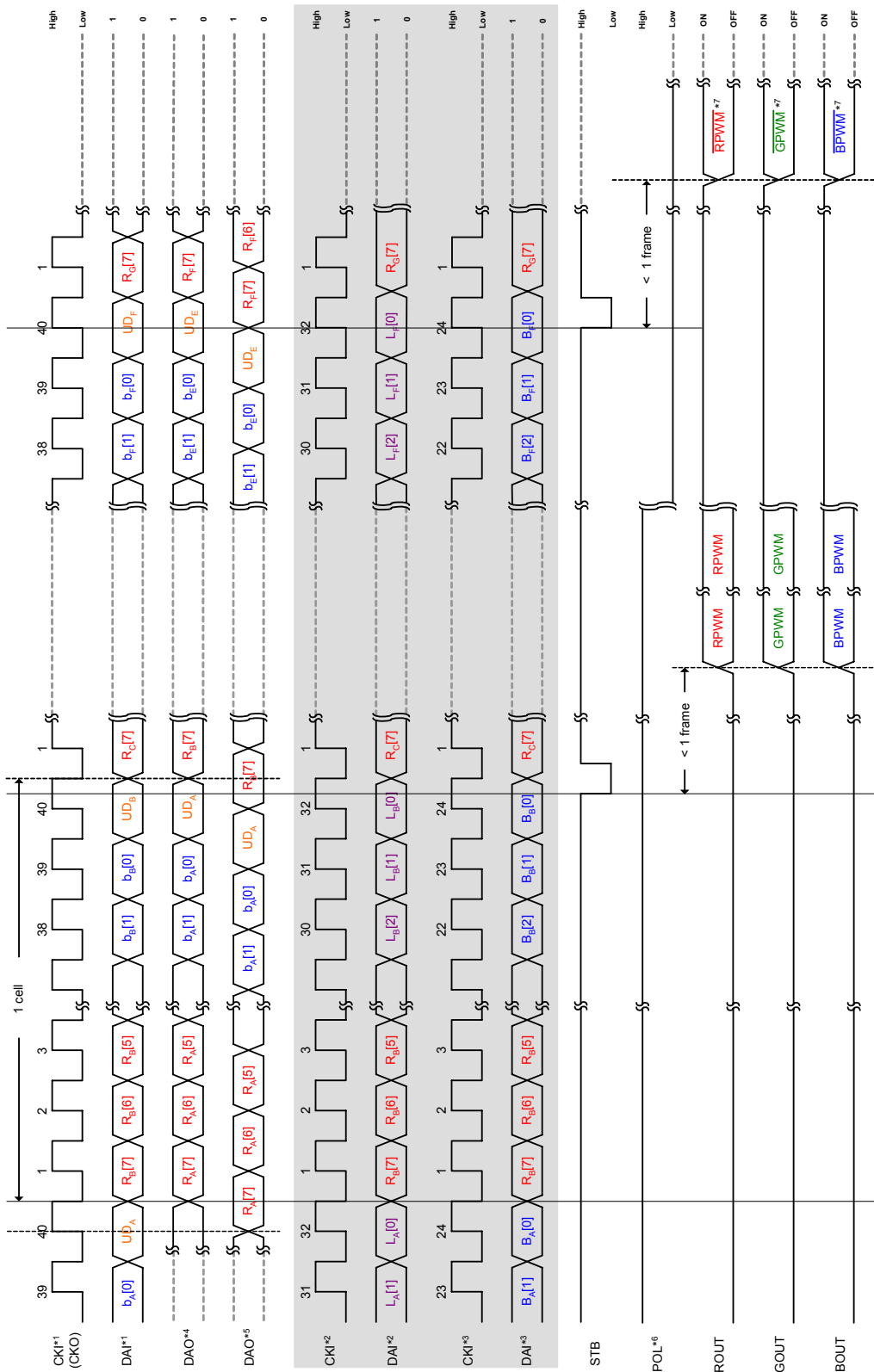
2. CKI-STB



3. STB-OUTn



Timing Diagram

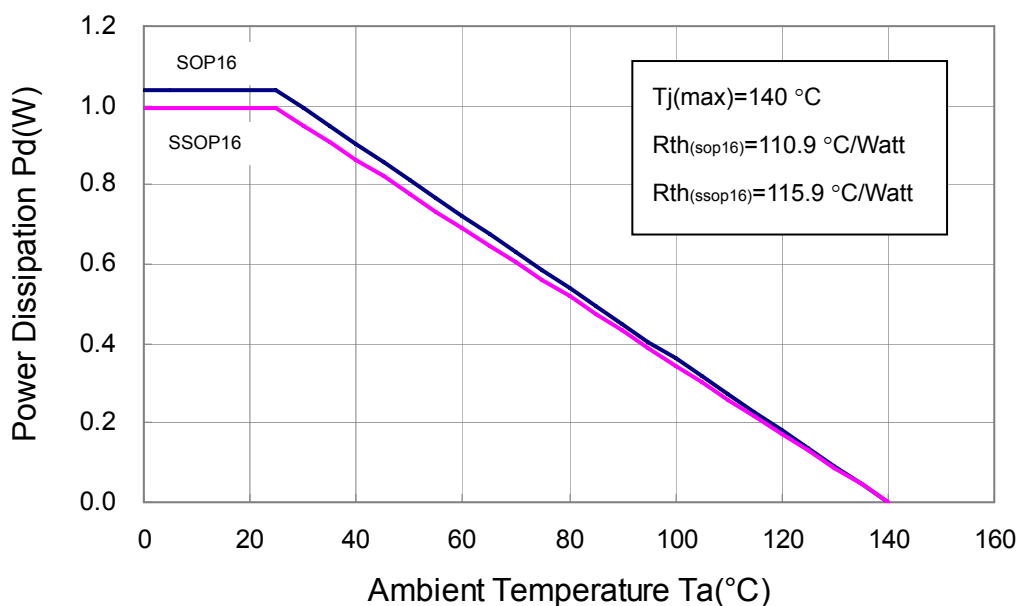


Power Dissipation

Notice that the power dissipation of a semiconductor chip is limited to its package and ambient temperature, in which the device requires the maximum output current calculated for given operating conditions. The maximum allowable power consumption can be calculated by the following equation:

$$Pd(max)(Watt) = \frac{Tj(junction\ temperature)(max)(\text{ }^{\circ}C) - Ta(ambient\ temperature)(\text{ }^{\circ}C)}{Rth(junction\text{-}to\text{-}air\ thermal\ resistance)(\text{ }^{\circ}C/Watt)}$$

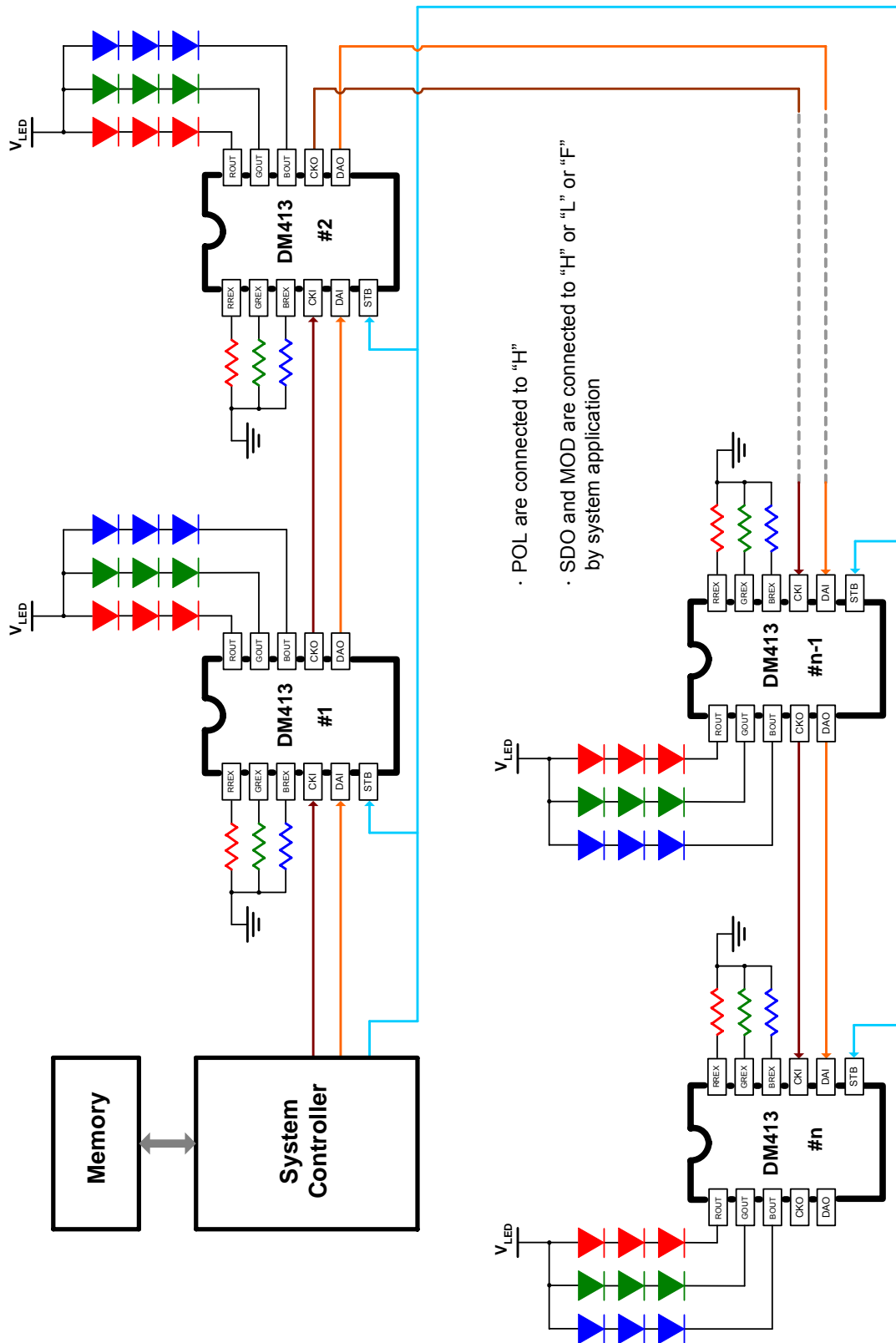
The relationship between power dissipation and operating temperature can be refer to the figure below:



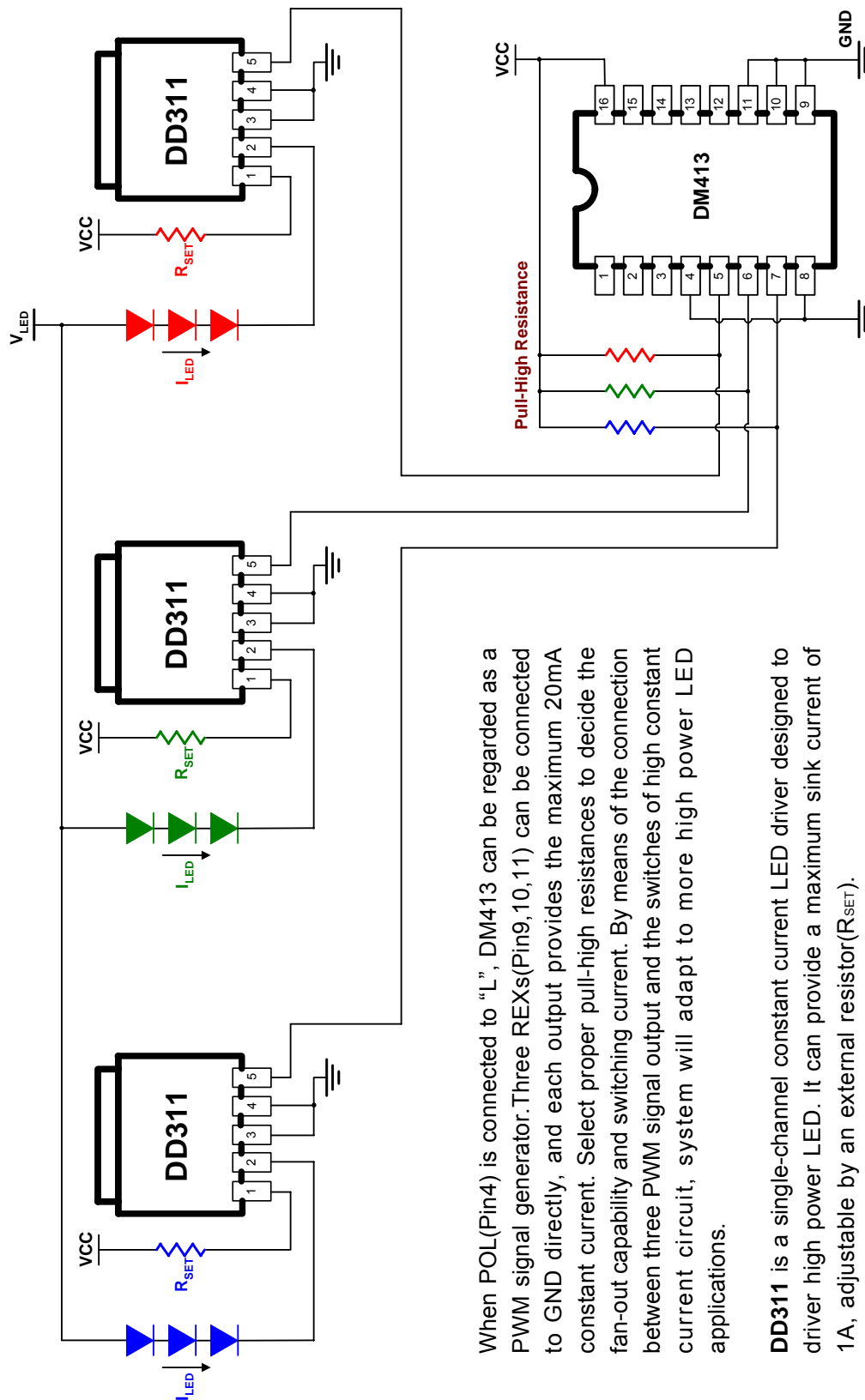
Based on the Pd(max), the maximum allowable voltage of output terminal can be determined by the following equation:

$$VoutR \times IoutR \times DutyR + VoutG \times IoutG \times DutyG + VoutB \times IoutB \times DutyB \leq Pd(max)(W) - Vcc(V) \times IdD(A)$$

Typical Application



Typical Application

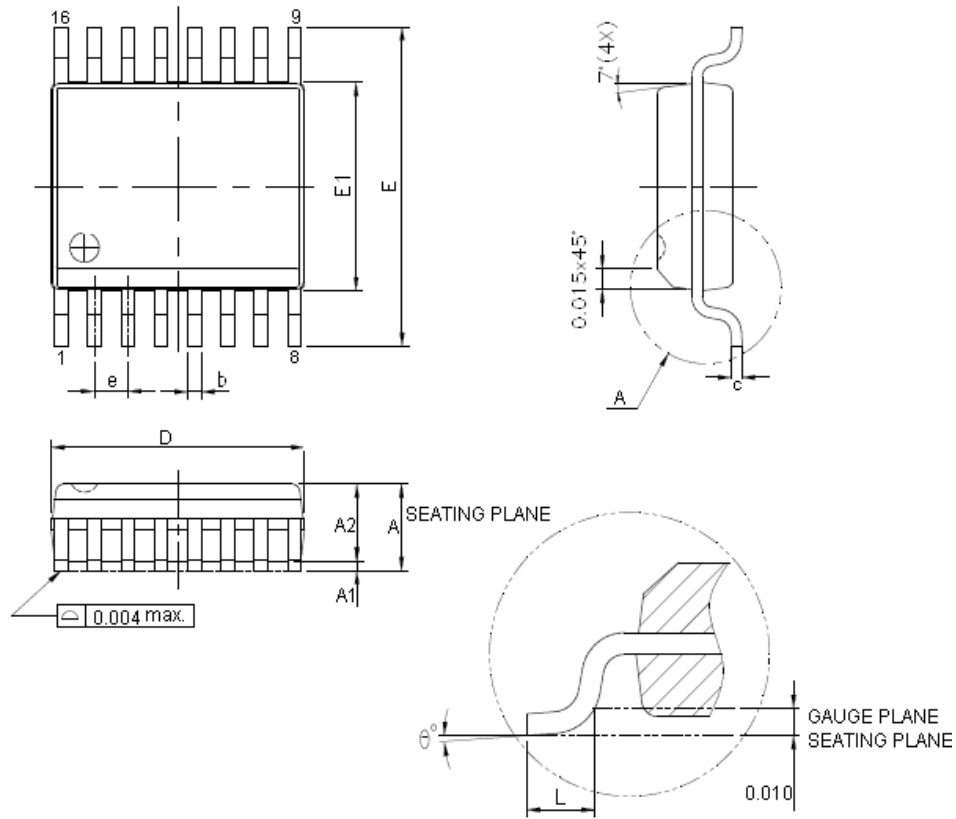


When POL (Pin4) is connected to "L", DM413 can be regarded as a PWM signal generator. Three REXs (Pin9, 10, 11) can be connected to GND directly, and each output provides the maximum 20mA constant current. Select proper pull-high resistances to decide the fan-out capability and switching current. By means of the connection between three PWM signal output and the switches of high constant current circuit, system will adapt to more high power LED applications.

DD311 is a single-channel constant current LED driver designed to driver high power LED. It can provide a maximum sink current of 1A, adjustable by an external resistor (R_{SET}).

Package Outline Dimension

SSOP16

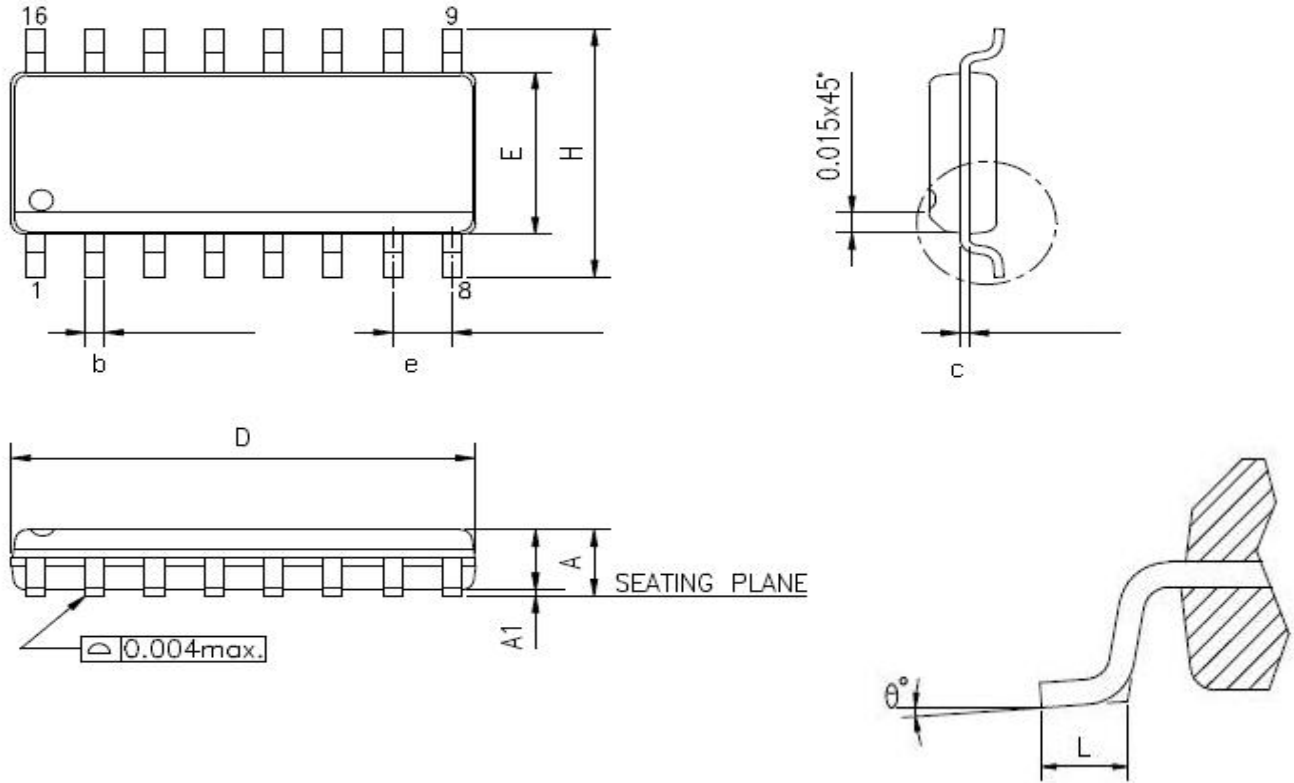


SYMBOLS	Min.	Typ.	Max.
A	1.346	-	1.753
A1	0.102	-	0.254
A2	1.245	-	1.499
b	0.190	-	0.305
c	0.178	-	0.350
D	4.801	4.902	5.004
E	5.791	-	6.200
e	0.635 BSC		
E1	3.800	-	4.000
L	0.400	-	1.270
θ°	0	-	8

unit:mm

Package Outline Dimension

SOP16



SYMBOLS	Min.	Typ.	Max.
A	1.346	-	1.753
A1	0.051	-	0.250
b	0.330	-	0.510
c	0.190	-	0.250
D	9.800	-	10.008
E	3.800	-	4.000
e	1.270 BSC		
H	5.791	-	6.200
L	0.400	-	1.270
θ°	0	-	8

unit:mm

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