

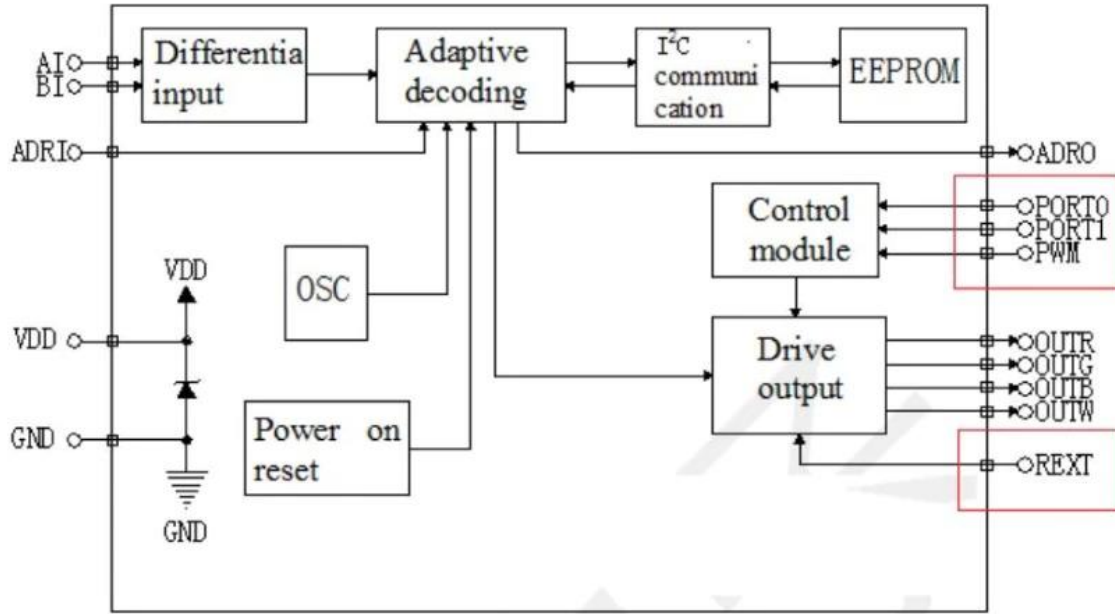
## Overview

TM512AC is a LED drive chip of DMX512 differential parallel protocol, Gray level 16 bits, gamma correction 2.2 enhancement, more suitable for human visual perception. With optional 1/2/3/4-channel high-precision constant current output and decoding forwarding function. TM512AC decoding technology can accurately decode DMX512 signals, compatible with and able to expand DMX512 protocol signals. TM512AC can perform complete adaptive decoding for DMX512 signals within the transmission frequency of 200Kbps-500Kbps, without the need for rate setting, addressing up to 4,096 channels. TM512AC has built-in E2PROM, without the need for external connection, supporting on-line code writing. The chip provides 4 voltage-withstand high-precision constant current output channels (30V, up to 80mA) and sets output current via 1 external resistor. And SSOP10 default each channel is 18 mA. TM512AC has the PWM reverse polarity underclocking output function, which fits for plug-in triode and MOS tube for current expansion driving. With a high port refresh rate, the picture refresh rate is greatly improved. Moreover, TM512AC can short out multiple constant current output interfaces to expand current driving capability. It is mainly designed for construction decoration and stage-lighting effect LED illuminating systems. The abnormality of one chip does not affect the normal operation of other chips. The maintenance is simple and convenient. The product boasts excellent performance and reliable quality.

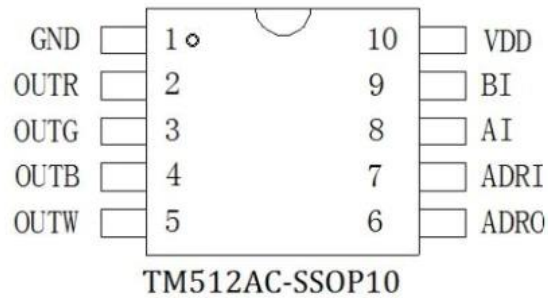
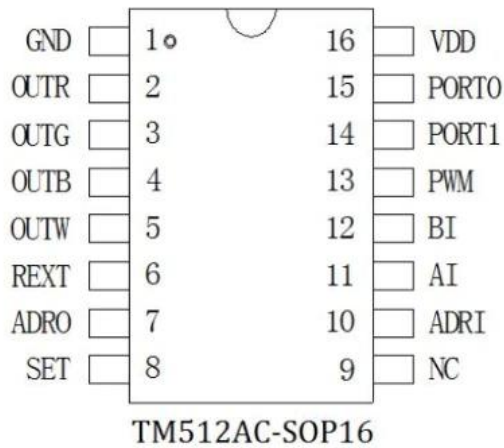
## Features

- Compatible with and able to expand DMX512(1990) signal protocol
- Control mode: differential parallel, addressing up to 4,096 channels
- Complete adaptive decoding for DMX512 signals within the transmission rate of 200Kbps-1000Kbps
- With built-in E2PROM, without the need for external connection
- The built-in 485 module has the advantages of high differential signal resolution and high differential input impedance, which can greatly enhance the carrying capacity.
- AB line on-line code writing, one-time automatic code writing, support installation before code writing mode
- E2 address code dual backup mode, part of E2 damage does not affect address code reading
- PWM reverse polarity underclocking output function, port refresh rate after underclocking is 250Hz
- PWM 256 gray level control
- Picture refresh rate over 2KHz
- With built-in 5V voltage-regulator tube
- 16-bit gray level control of output port, 2.2 enhancement of gamma correction, more suitable for human visual perception
- OTR/OUTG/OUTB/OUTW output withstand voltage over 30V
- OTR/OUTG/OUTB/OUTW four-bit constant current output channels
- With external output constant current adjustable resistance, the current range for each channel is 3-80mA
- SSOP10 default each channel is 18mA
- ±3% current difference value between channels, ±3% current difference value between chips
- Supporting the data reading mode of 1/2/3/4-set of fields
- Power on, self-check blue light, red light at the first address after successful coding, and white light at the other addresses for breakpoint identification
- Output channels delay step by step to lower surge current interference
- Industrial grade design, stable performance
- Packaging mode: SOP16 and SSOP10.

**Block diagram for internal structure**



**Pin configuration**



**Pin function**

Pin name	Pin number SOP16	Pin number SSOP10	I/O	Function description
VDD	16	10	--	Positive pole of power supply
GND	1	1	--	Negative pole of power supply
OULTR/OUTG/OUTB/OUTW	2~5	1~4	O	PWM output port
REXT	6	-	I	Constant current feedback end, with grounding resistance to adjust output current
ADRO	7	6	O	Address code writing wire output
SET	8	-	O	
NC	9	-	I	NC
ADRI	10	7	I	Address code writing wire input, built-in and pull-up
AI	11	8	I	Differential signal, positive
BI	12	9	I	Differential signal, negative
PWM	13	-	I	Output polarity selection, generally suspended, output polarity is opposite after connecting VDD, meanwhile, port refresh rate is dropped to 500Hz
PORT1	14	-	I	Field selection, built-in and pull-down
PORT0	15	-	I	Field selection, built-in and pull-down

## Input/output equivalent circuit

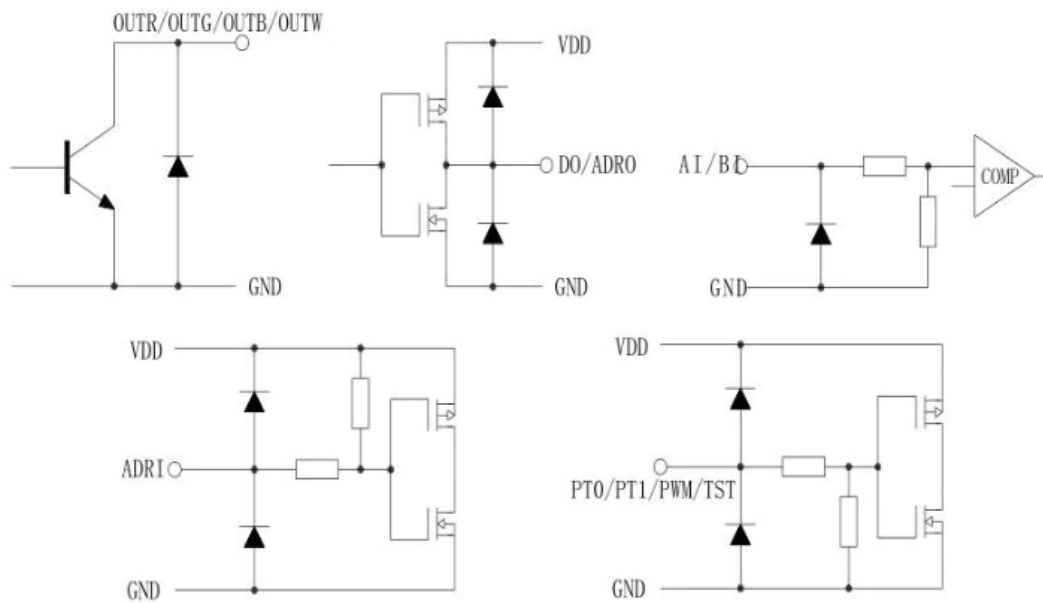


Figure 3

## Operating conditions

### 1. Limiting operating conditions

Tested under 25°C, VDD = 5V, unless otherwise specified		TM512AC	Unit
Parameter name	Parameter symbol	Limit value	
Logic supply voltage	Vdd	+5.5~+6.5	V
Output port withstand voltage	Vout	30	V
Logic input voltage	Vi	-0.5~Vdd+0.5	V
Operating temperature	Topt	-40~ +85	°C
Storage temperature	Tstg	-55~ +150	°C
Antistatic electricity	ESD	8000	V
Packaging power consumption	Pd	800	mW

- (1) When the chip works for a long time under the above limit parameters, it may cause device reliability reduction or permanent damage. Titan Micro Electronics does not suggest any parameter reaching or exceeding the limit value in practical use.
- (2) All voltage values are comparatively tested in a systematic way.

### 2. Recommended operating conditions

Tested under -40°C~+85°C, VDD = 5V, unless otherwise specified			TM512AC			Unit
Parameter name	Parameter symbol	Testing condition	Min. value	Typical value	Max. value	
Logical supply voltage	Vdd	--	2.6	5.5	6.5	V
High level input voltage	Vih	--	0.7Vdd	--	Vdd	V
Low level input voltage	Vil	—	0	—	0.3Vdd	V
Output port withstand voltage	Vout				30	V

# Chip parameters

## 1. Electrical characteristics

Tested under -40°C~+85°C, VDD = 4.5V-5.5V, GND = 0, unless otherwise specified			TM512AC			Unit
Parameter name	Parameter symbol	Testing condition	Min. value	Typical value	Max. value	
Low level output current	I <sub>ol</sub>	V <sub>o</sub> =0.4V, DO, ADRO	10	-	-	mA
High level output current	I <sub>oh</sub>	V <sub>o</sub> =4V, DO, ADRO	10	-	-	mA
Input current	I <sub>i</sub>		-	-	±1	µA
Differential input common mode voltage	V <sub>cm</sub>				12	V
Differential input current	I <sub>ab</sub>	VDD=5V			28	µA
Differential input threshold voltage	V <sub>th</sub>	0V<V <sub>cm</sub> <12V	-0.2		0.2	V
Differential input hysteresis voltage		V <sub>cm</sub> =0V		70		mV
Differential input impedance	R <sub>in</sub>			270		KΩ
Output pin current	I <sub>sink</sub>	OUTR, OUTG, OUTB, OUTW (SOP16 REXT grounding resistance 550Ω)	3		60	mA

Output pin current	I <sub>sink</sub>	OUTR, OUTG, OUTB, OUTW (SSOP10 REXT grounding resistance 550Ω)		18		mA
High level input voltage	V <sub>ih</sub>	ADRI	0.7V <sub>dd</sub>	-		V
Low level input voltage	V <sub>il</sub>	ADRI	-	-	0.3V <sub>dd</sub>	V
Current offset (between channels)	dI <sub>out</sub>	V <sub>ds</sub> =1V, I <sub>out</sub> =17mA		±1.5	±3.0	%
Current offset (between chips)	dI <sub>out</sub>	V <sub>ds</sub> =1V, I <sub>out</sub> =17mA		±3.0	±5.0	%
Voltage offset VS-V <sub>ds</sub>	%dV <sub>ds</sub>	1V<V <sub>ds</sub> <3V		±0.1	±0.5	%/V
Voltage offset VS-V <sub>dd</sub>	%dV <sub>ds</sub>	4.5V<V <sub>dd</sub> <5.5V		±1.0	±2.0	%/V
Dynamic current loss	IDD <sub>dyn</sub>	VDD=5V	No load		4	mA
Thermal resistance	R <sub>th(j-a)</sub>			80	150	°C/W

## Function description

### 1. Communication data protocol:

TM512AC data reception is compatible with standard DMX512(1990) protocol and able to expand DMX512 protocol. TM512AC can perform adaptive decoding for a data transmission rate of 200Kbps-1000Kbps. The protocol waveform is as follows: the chip is AI and Bi differentially input. The figure shows the time sequence waveform of AI which is opposite to that of BI.

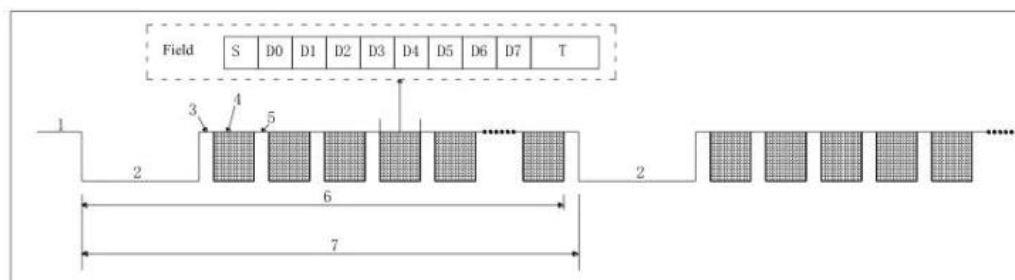


Figure 4

Symbol	Description	Min. value	Typical value	Max. value	Unit
	Bit rate	200	500	1000	Kbps
	Bit time	1	2	5	μs
S	Start bit	1	2	5	μs
D0~D7	8 data bits	1	2	5	μs
T	2 stop bits	2	4	10	μs
1	Mark before reset	0		1000000	μs
2	Reset signal	88		1000000	μs
3	Mark after reset	8		1000000	μs
4	Field (note1)	11	22	55	μs
5	Span between fields	0		1000000	μs
6	Length of data packet	1024		1000000	μs
7	Reset signal interval	4096		1000000	μs

Note1: The field totally contains 11 bits, including 0 start bit, 8 data bits and 2 stop bits, wherein the 0 start bit is low level and the stop bits are high levels. If the data in the data bits is 0, the corresponding time period is low levels; if the data is 1, the corresponding time period is high level. The bit time for the 0 start bit, the stop bits and the data bits should be the same.

## 2. IC reception description:

1. When reset signal appears on AIBI wire, IC enters the reception-ready state, and the address counter resets.

2. The first field in the data packet is start field. Its 8 data bits must be "0000\_0000". This field does not act as display data. The valid field used for display starts from the second field. The second field of DMX512 data packet is the first field of valid data. IC is self-adaptive to the data transmission rate of 200Kbps-1000Kbps. Different rates correspond to different field durations. However, no matter the transmission rate is 200Kbps or 500Kbps or 1000Kbps, it only needs to ensure that the durations of all valid fields are same to that of the start field.

3. IC cuts out the corresponding field in DMX512 data packet according to the address in its E2. For example, if the chip address is 0000\_0000\_0000, it starts to cut out from the first valid field of the data packet; if the address is 0000\_0000\_0001, it starts to cut out from the second valid field. How many fields are used by the chip is set by PT1 and PT0.

PT1 (built-in and pull-down)	PT0 (built-in and pull-down)	Mode and number of fields cut out
0	0	3-field mode: 3 fields are cut out, respectively corresponding to R, G and B (SOP16 default mode)
0	1	4-field mode: 4 fields are cut out, respectively corresponding to R, G, B and W(SSOP10 default mode)
1	0	2-field mode: 2 fields are cut out, respectively corresponding to RG and BW
1	1	1-field mode: 1 field is cut out, corresponding to RGBW

The 1-field mode and 2-field mode in the above table can achieve the current expansion function. For example, in the 1-field mode (generally monochrome application), the four output pins OUT/OUTR/OUTGB/OUTW can join up in parallel, when the maximum output current is up to 320mA. The said field selection is required only for data forwarding and current expansion. When current expansion is not required and under the point light source application (without the need for data forwarding), both PORT0 and PORT1 can be suspended from monochrome application and RGB trichromatic application.

4. When IC receives data, the interval of 2 reset signals cannot be less than 4ms. The frame frequency cannot be greater than 250Hz even though there are very few parallel connection points.

### 3. Precautions for the controller to send data:

1. As for standard DMX512(1990) protocol, if one subport of the controller connects 512 channels, that is to say, 170 pixel points, to achieve the refresh rate of 30Hz, the time width of each frame is 33.33ms and the time for transmitting 1bit is 4 $\mu$ s, the valid data time width will be  $88+4\mu s*11bit*512 = 22.7ms$  and the time interval of each frame of data will be  $33.33-22.7 = 10.63ms$ . In this time interval, the data line keeps at high level until the next reset signal.

2. TM512AC requires the reset signal code interval of each data packet of the controller cannot be less than 4ms, i.e., the highest frame frequency cannot not be more than 250Hz, or else it may fail to display in a normal way.

#### 4. Notes for Coding:

1. After the completion of coding, the IC driver of the first address code is always on, and the white driver of the other address IC is always on. The newly written address code is valid and can be used as a breakpoint discrimination.

2. Don't take AB line off after code writing is completed. Test it with the special test program of the code writer to confirm whether the code writing is correct or not.

3. Address input terminal lines on AI and BI ports should be pulled out from the coder after the completion of the code writing, so as to avoid erroneous code writing when the coder is out of order. The code writing line is suspended after being pulled out and wrapped with insulating tape, without special grounding.

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one point rather than grounded at double ends or multiple ends.

2. The protective resistors connected in parallel from AI and BI wires on the board to ICs should be consistent. The wiring mode of AI and BI wires on the board from bonding pad to ICs should try to be consistent.

3. AI and BI buses should try to adopt shielded twisted pair (especially in weak-current and heavy-current wiring duct sharing projects, nearby launching tower or the areas with more lightning) to reduce interference and lightning impulse. Cat. 5e shielded twisted pair can be used, but pay attention to purchase copper wire.

4. 485 node in 485 bus should try to reduce the distance with main line. It is generally suggested that 485 bus adopts hand-in-hand bus topology. Star configuration will produce reflected signals, which affect the quality of 485 communication. In the construction process, the distance between 485 node and 485 bus main line must be over 30cm. It is suggested to use 485 repeater as a bifurcation of 485 bus. If star topology is required to be used in the construction process, 485 concentrator should be used.

5. 485 bus will produce reflection echo signals along with the prolonging of transmission distance. If the transmission distance of 485 bus is long, it is suggested to connect a 120 $\Omega$  terminal matching resistor on AI and BI wires at 485 communication terminal when construction is in process.

## 6. Enhanced gamma correction 2.2 explains:

1. TM512C has its own gamma correction with a coefficient of 2.2. The 256-level gray level is corrected to 65536-level gray level.

2. TM512C adopts the enhanced design method. The RGBW output opening time is: basic opening time + corrected gray time. That is to say, a basic opening time is added on the basis of each level of gray level time. Its purpose is to compensate for the large difference of opening time between different high power constant current drive IC in actual opening delay and high power application, so as to ensure that the first level gray level can be clearly perceived by human eyes in most cases when cooperating with different high power constant current IC.

3. Positive polarity: foundation opening time is about 85 ns; negative polarity: foundation opening time is about 1035 ns. Inverse polarity sets a longer base opening time, in order to better compatible with most high power constant current drive IC, to compensate for its opening delay, so that the first gray level can be clearly perceived by the human eye.

## Constant current module

### 1. Output constant current setting:

OUTR, OUTG, OUTB and OUTW are constant current output. The maximum current can be up to 60mA. It is not suggested to set the current at the maximum value in practical application. The constant current value is determined by REXT grounding resistance. Current formula:

$$I_{out} = 48 / (400 + R_{ext}) \quad (1)$$

$$R_{ext} = (48 / I_{out}) - 400 \quad (2)$$

Rext is the resistor bridged between REXT pin and ground. Iout is the current output by OUTR, OUTG, OUTB and OUTW ports.

Current value (mA)	Rext resistance ( $\Omega$ )
18	2266
20	2000
36	933
60	400

Relationship between output current  $I_{out}$  and REXT of TM512AC-SOP16

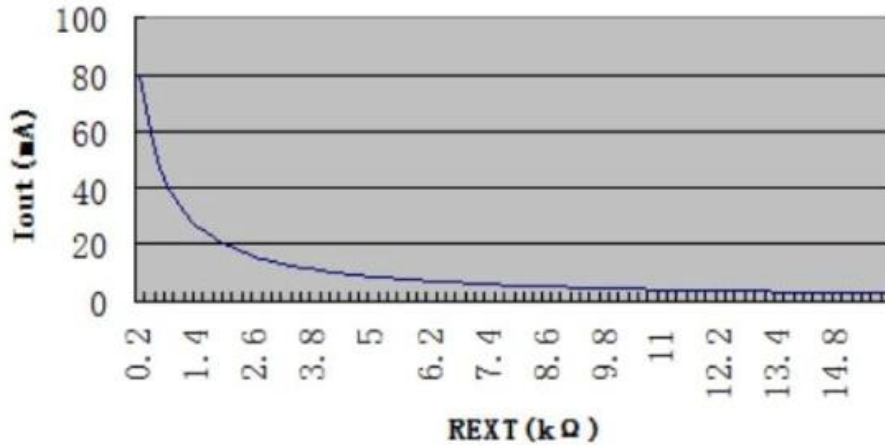


Figure 5

**Application information**

**1. Application drawing 1: RGBW tetrachromatic application**

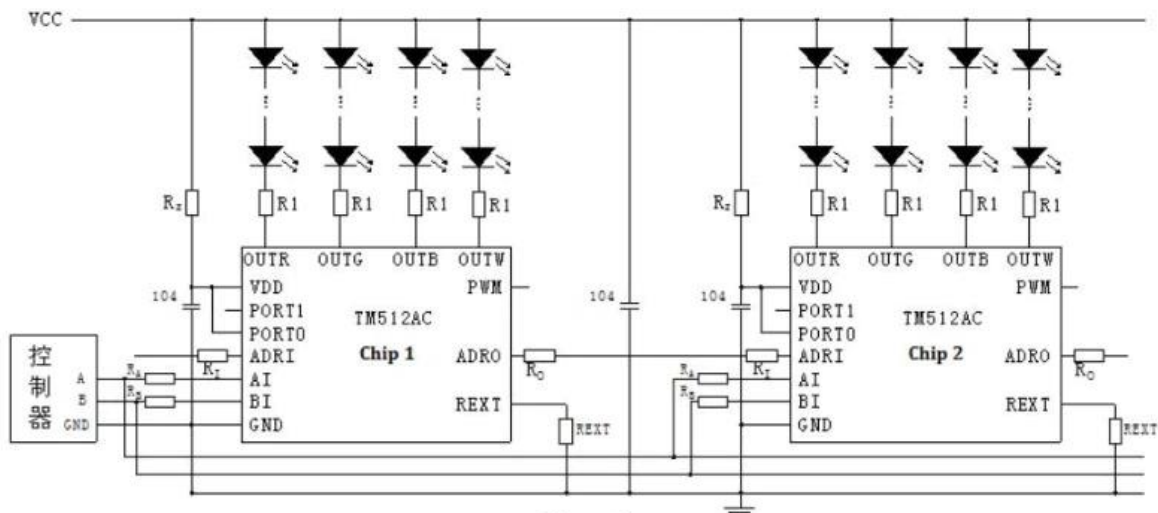


Figure 7

- Notes: 1.The coder/controller does not need to be connected to the ADRI of the first IC when the coder is written by line A and line B
- 2. Pay attention to the selection of divider resistor R to avoid excessive IC power consumption.
- 3. IC SOP16 packaging REXT port must add grounding resistance to set output current. This port cannot be suspended. IC SSOP10 default 18mA.



## 2. Application drawing 2: RGB trichromatic application

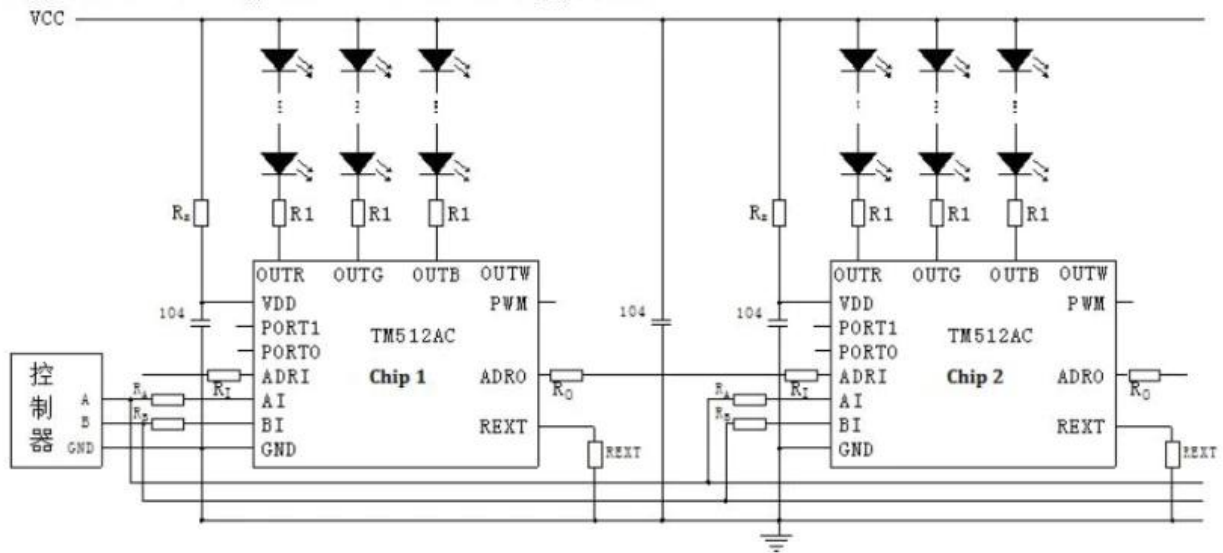


Figure 8

- Notes: 1. The coder/controller does not need to be connected to the ADRI of the first IC when the coder is written by line A and line B
2. Pay attention to the selection of divider resistor R to avoid excessive IC power consumption.
3. IC SOP16 packaging REXT port must add grounding resistance to set output current. This port cannot be suspended. IC SSOP10 default 18mA.

## 3. Application drawing 3: dichromatic application

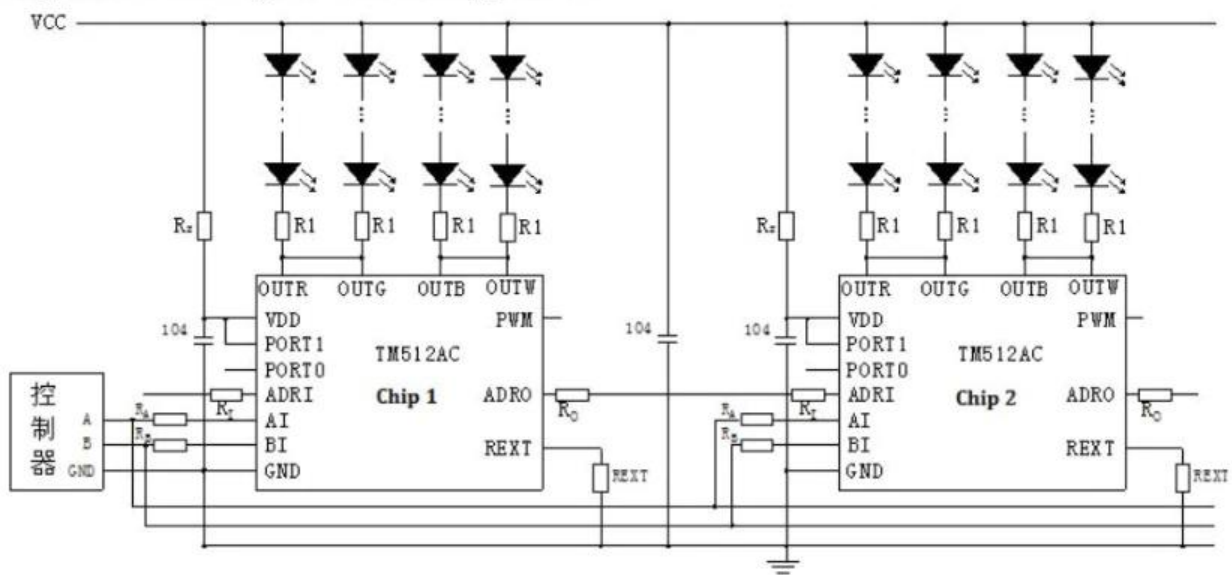


Figure 9

- Notes: 1. The coder/controller does not need to be connected to the ADRI of the first IC when the coder is written by line A and line B
2. In dual-color applications, the chip intercepts two bytes of data itself. The channel OUTR and OUTG data are the same, and the channel OUTB and OUTW data are the same. The figure shows parallel current expansion applications. The maximum output current of the two channels after parallel connection is 160mA.
3. Pay attention to the selection of divider resistor R to avoid excessive IC power consumption.
4. IC SOP16 packaging REXT port must add grounding resistance to set output current. This port cannot be suspended. IC SSOP10 cannot apply this mode.

#### 4. Application drawing 4: monochrome application

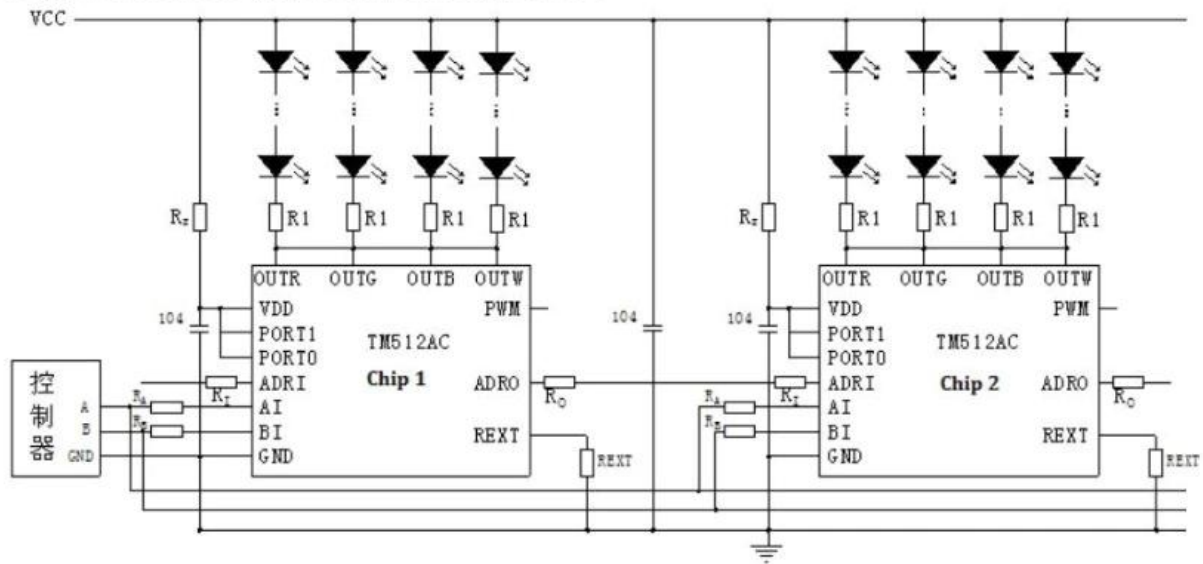
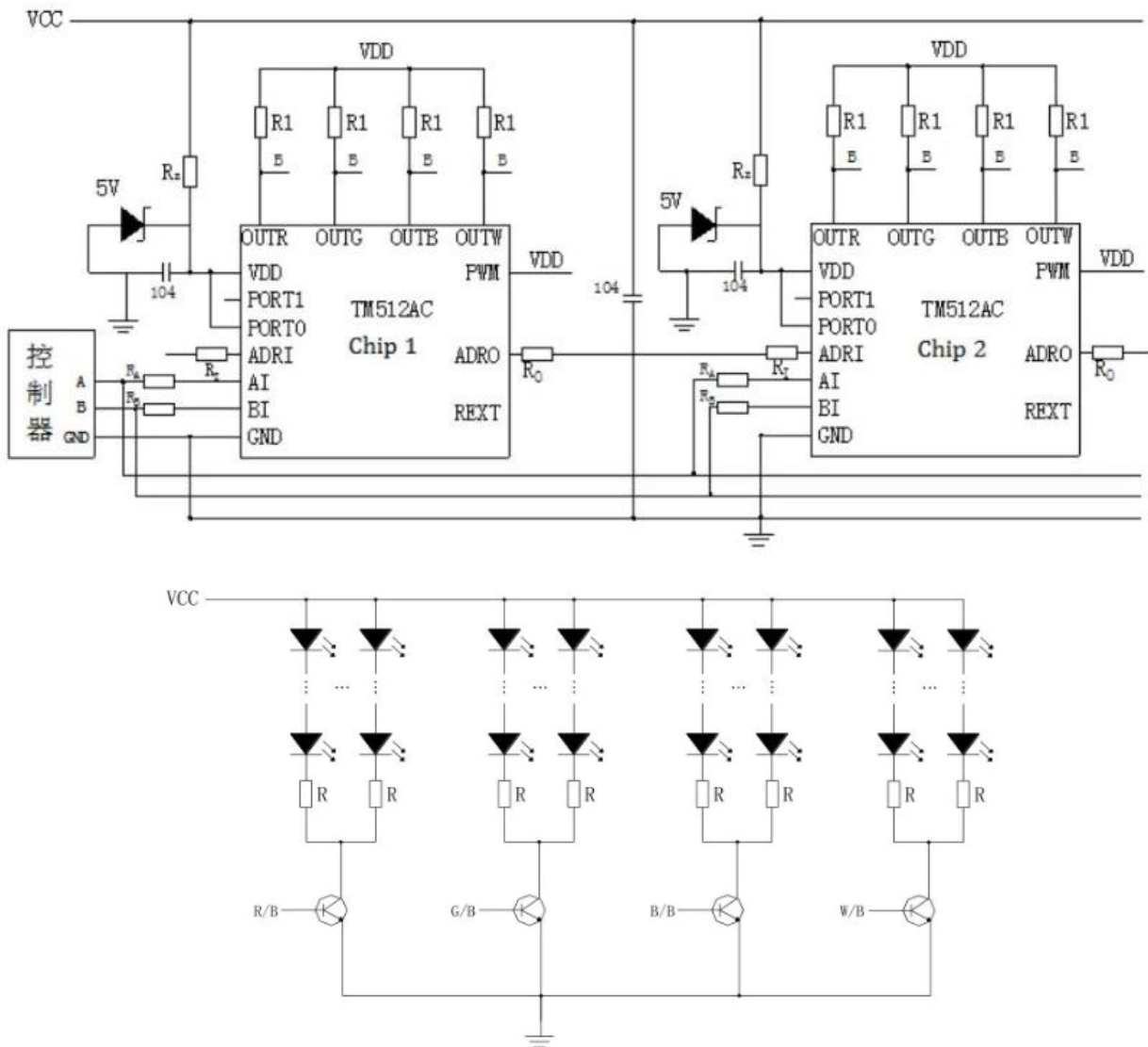


Figure 10

- Notes:
1. The coder/controller does not need to be connected to the ADRI of the first IC when the coder is written by line A and line B
  2. In monochrome applications, the chip itself intercepts 1 byte of data and 4 channels have the same data. The figure shows parallel current expansion applications. The maximum output current after 4 channels are parallel is 320 mA.
  3. Pay attention to the selection of divider resistor R to avoid excessive IC power consumption.
  4. IC SOP16 packaging REXT port must add grounding resistance to set output current. This port cannot be suspended. IC SSOP10 cannot apply this mode.

#### 5. Application drawing 5: plug-in triode application (can also be connected with external MOS tube)



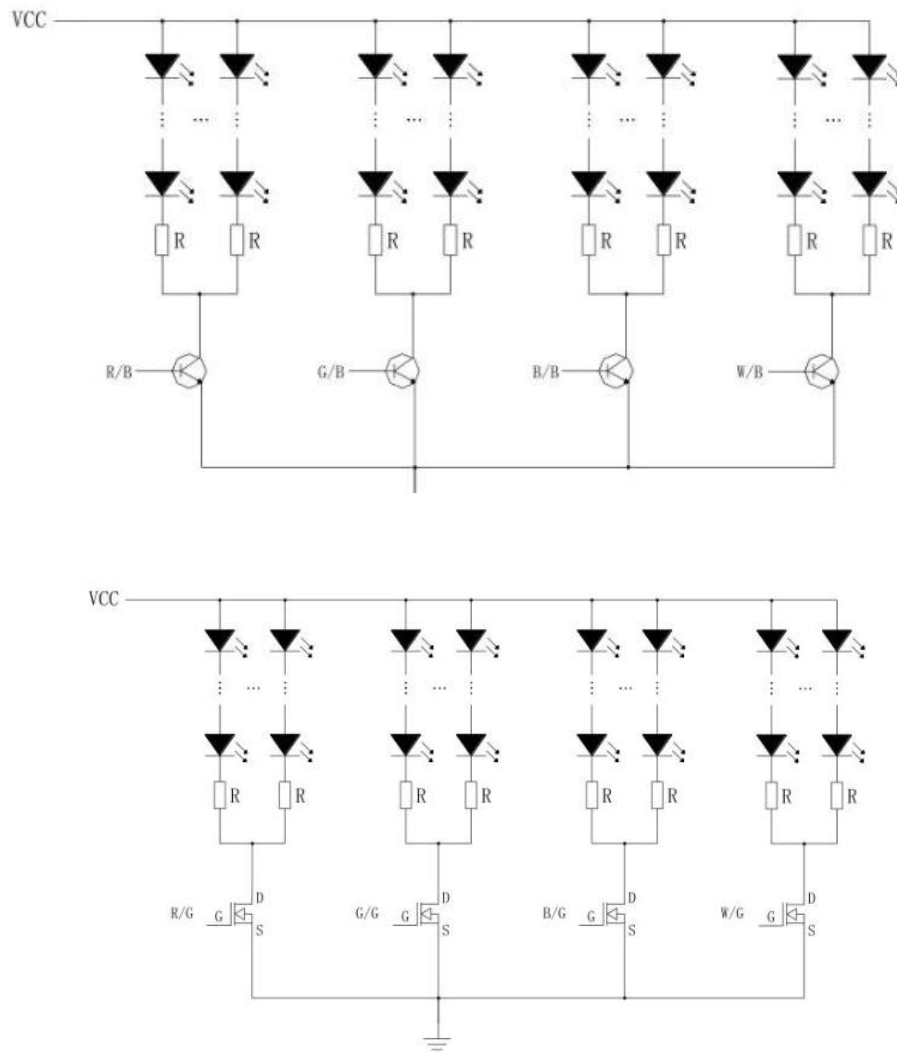


Figure 11

- Notes: 1.BJT: When the PWM pin connects to VDD, it is the output of reverse polarity, frequency reduction and constant voltage. It is suitable for external NPN triode base (B). When applied, the output pin connects pull-up resistance R1 to VDD. The pull-up resistance R1 should be selected according to the magnification of the triode and the required current. When the output current is large and the pull-up resistance needs to be less than 5K (base current is greater than 1mA), the value of the voltage-reducing resistance should be reduced accordingly and 5V regulator or other 5V regulator should be connected to the VDD.
- 2.MOS: When the PWM pin connects to VDD, it is the output of reverse polarity, frequency reduction and constant voltage. It is suitable for external MOS gate (G) or high power constant current drive. When applied, the output pin connects pull-up resistance R1 to VDD, and the pull-up resistance value is above 10K. If you want to reduce the brightness of the first gray level, the pull-up resistance R1 can be increased.
2. The above figure is the application drawing at 4-channel reverse polarity application. At other field reverse polarity application, pay attention to the selection of PORT0 and PORT1 ports.
3. IC SOP16 packaging REXT port must add grounding resistance to set output current. This port cannot be suspended. IC SSOP10 cannot apply this mode.

**6. Tables of optional values for components(NO plug-in triode application)**

VCC	24V	12V	5V
$R_Z$ ( $\Omega$ )	2K~2.4K	750~820	82
$R_I$ ( $\Omega$ )	300-500	300-500	-
$R_O$ ( $\Omega$ )	300-500	300-500	-
$R_A$ ( $\Omega$ )	1K-5K	1K-5K	1K-5K
$R_B$ ( $\Omega$ )	1K-5K	1K-5K	1K-5K

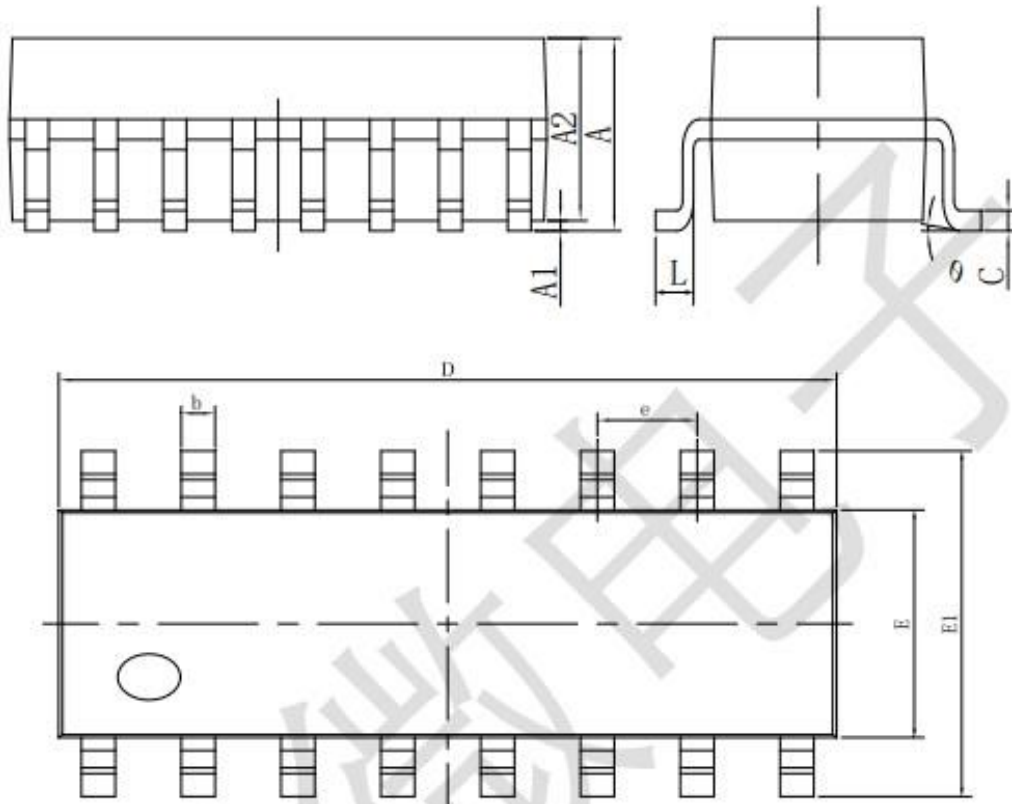
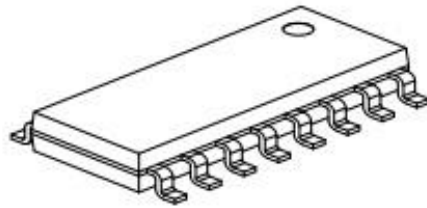
**7. Tables of optional values for components(Plug-in triode application, Single circuit current not exceeding 120 mA)**

	24V	12V
R1	2.5K	2.5K
$R_Z$ ( $\Omega$ )	1K	300
VDD Parallel Voltage Regulator	Unwanted	wanted

Value selection of light string resistor R1

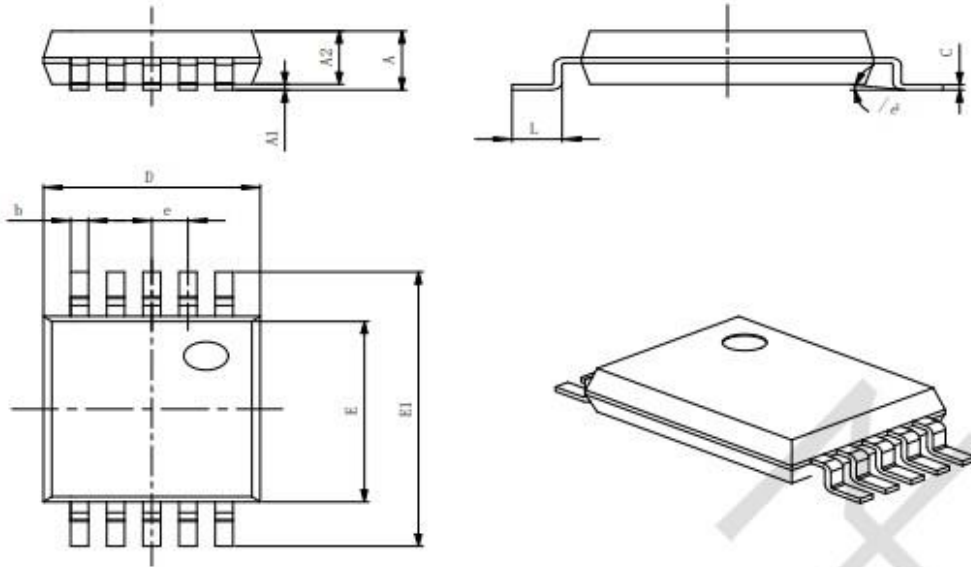
	DC24V		DC12V
	7 strings	6 strings	3 strings
Rg/Rb/Rw	0R	220R	0R
Rr	470R	560R	250R

封装示意图: SOP16



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.30	1.70	0.051	0.067
A1	0.08	0.24	0.003	0.009
b	0.4TYP		0.016TYP	
c	0.25TYP		0.010TYP	
D	8.25	8.85	0.325	0.348
E	3.75	4.15	0.148	0.163
E1	5.70	6.30	0.224	0.248
e	1.27TYP		0.050TYP	
L	0.45	0.85	0.018	0.033
$\theta$	0°	8°	0°	8°

封装示意图: SSOP10



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	-	1.75	-	0.067
A1	0.1	0.225	0.004	0.009
A2	1.30	1.50	0.051	0.059
b	0.39	0.48	0.015	0.019
c	0.21	0.26	0.008	0.01
D	4.70	5.10	0.185	0.201
E	3.70	4.10	0.146	0.161
E1	5.80	6.20	0.228	0.244
e	1.0 (BSC)		0.039 (BSC)	
L	1.05 (BSC)		0.041 (BSC)	
θ	0°	8°	0°	8°

All specs and applications shown above subject to change without prior notice.

(以上电路及规格仅供参考, 如本公司进行修正, 恕不另行通知)