

TLV760 100-mA, 30-V, Fixed-Output, Linear-Voltage Regulator

1 Features

- Wide Input Voltage Range up to 30 V
- Output Current up to 100 mA
- Available in Fixed Output Voltage 3.3-V, 5-V, 12-V and 15-V Versions
- Operating Junction Temperature -40°C to $+125^{\circ}\text{C}$
- Stable With Ceramic Capacitors Greater Than or Equal to $0.1\ \mu\text{F}$
- Active Thermal Protection and Current Limit

2 Applications

- Post Regulator for Switching DC-DC Converter
- Bias Supply for Digital and Analog Circuits
- Home Appliances
- Power Tools
- Factory and Building Automation

3 Description

The TLV760 is an integrated linear-voltage regulator featuring operation from an input as high as 30 V. The TLV760 has a maximum dropout of 1.2 V at the full 100-mA load across operating temperature. Standard packaging for the TLV760 is the 3-pin SOT-23 package.

The TLV760 is available in 3.3 V, 5 V, 12 V and 15 V. The SOT-23 packaging of the TLV760 series allows the device to be used in space-constrained applications. The TLV760 is a small size alternative to LM78Lxx series and similar devices.

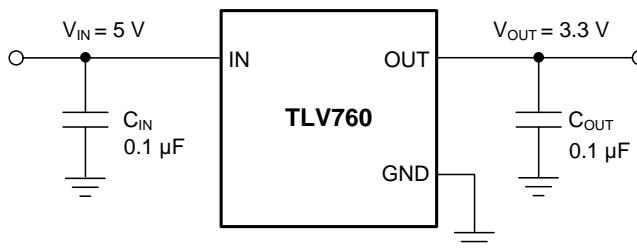
The TLV760 is designed to bias digital and analog circuits in applications that are subject to voltage transients and spikes up to 30 V — for example, appliances and automation applications. The device has robust internal thermal protection, which protects itself from potential damage caused by conditions like short to ground, increases in ambient temperature, high load, or high dropout events.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV760	SOT-23 (3)	2.92 mm x 1.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



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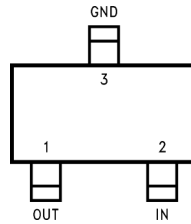
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (June 2017) to Revision A	Page
• Changed description of pin 1 to "OUT" and pin 2 to "IN" to correct error	3

5 Pin Configuration and Functions

**DBZ Package
3-Pin SOT-23
Top View**



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	OUT	O	Output voltage, a ceramic capacitor greater than or equal to 0.1 μ F is need for the stability of the device. ⁽¹⁾
2	IN	I	Input voltage supply — TI recommends a capacitor of value greater than 0.1 μ F at the input. ⁽¹⁾
3	GND	—	Common ground

(1) See [External Capacitors](#) for more details.

6 Specifications

6.1 Absolute Maximum Ratings⁽¹⁾

	MIN	MAX	UNIT
Input voltage (IN to GND)	-0.3	35	V
Output Voltage (OUT)		$V_{IN} + 0.3$	V
Output Current		Internally limited ⁽²⁾	mA
Junction temperature	-40	150	°C
Storage temperature, T_{stg}	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings*⁽¹⁾ may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) See *Recommended Operating Conditions* section for more details.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500
			V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Maximum input voltage (IN to GND)		30	V
Output current (I_{OUT})		100	mA
Input and output capacitor (C_{OUT})	0.1		µF
Junction temperature, T_J	-40	125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TLV760	UNIT
		DBZ (SOT-23)	
		3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	275.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	92.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	55.6	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Typical and other limits apply for $T_A = T_J = 25^\circ\text{C}$, $V_{\text{OUT(NOM)}} = 3.3\text{ V}, 5\text{ V}, 12\text{ V}, \text{ and } 15\text{ V}$, unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage accuracy	$V_{\text{IN}} = V_{\text{OUT(NOM)}} + 1.5\text{ V}$, $1\text{ mA} \leq I_{\text{OUT}} \leq 100\text{ mA}$		-4%		4%	V
		$V_{\text{IN}} = V_{\text{OUT(NOM)}} + 1.5\text{ V}$, $1\text{ mA} \leq I_{\text{OUT}} \leq 100\text{ mA}$, $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$		-5%		5%	
$\Delta V_{(\Delta V_{\text{IN}})}$	Line regulation	$V_{\text{OUT(NOM)}} + 1.5\text{ V} \leq V_{\text{IN}} \leq 30\text{ V}$ $I_{\text{OUT}} = 1\text{ mA}$, $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	$V_{\text{OUT(NOM)}} = 3.3\text{ V}, 5\text{ V}$		10	30	mV
			$V_{\text{OUT(NOM)}} = 12\text{ V}, 15\text{ V}$		14	45	
$\Delta V_{(\Delta I_{\text{OUT}})}$	Load regulation	$V_{\text{IN}} = V_{\text{OUT(NOM)}} + 1.5\text{ V}$, $10\text{ mA} \leq I_{\text{OUT}} \leq 100\text{ mA}$, $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	$V_{\text{OUT(NOM)}} = 3.3\text{ V}, 5\text{ V}$		20	45	mV
			$V_{\text{OUT(NOM)}} = 12\text{ V}, 15\text{ V}$		45	80	
I_{GND}	Ground pin current	$V_{\text{OUT(NOM)}} + 1.5\text{ V} \leq V_{\text{IN}} \leq 30\text{ V}$, no load, $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$			2	5	mA
V_{DO}	Dropout voltage	$I_{\text{OUT}} = 10\text{ mA}$			0.7	0.9	V
		$I_{\text{OUT}} = 10\text{ mA}$, $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$				1	
		$I_{\text{OUT}} = 100\text{ mA}$			0.9	1.1	
		$I_{\text{OUT}} = 100\text{ mA}$, $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$				1.2	
T_{SD}	Thermal shutdown temperature				150		$^\circ\text{C}$

6.6 Typical Characteristics

Unless indicated otherwise, $V_{IN} = V_{NOM} + 1.5\text{ V}$, $C_{IN} = 0.1\ \mu\text{F}$, $C_{OUT} = 0.1\ \mu\text{F}$, and $T_A = 25^\circ\text{C}$.

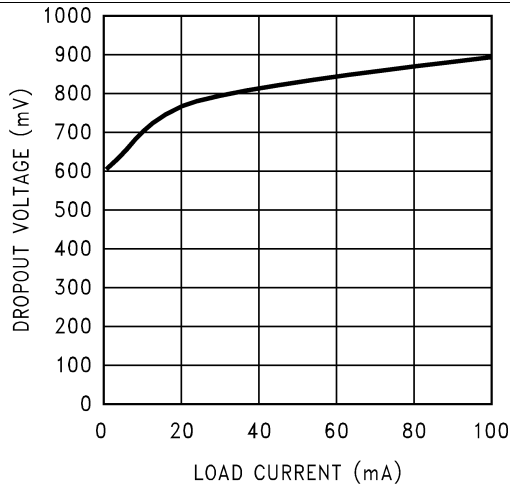


Figure 1. Dropout Voltage vs Load Current

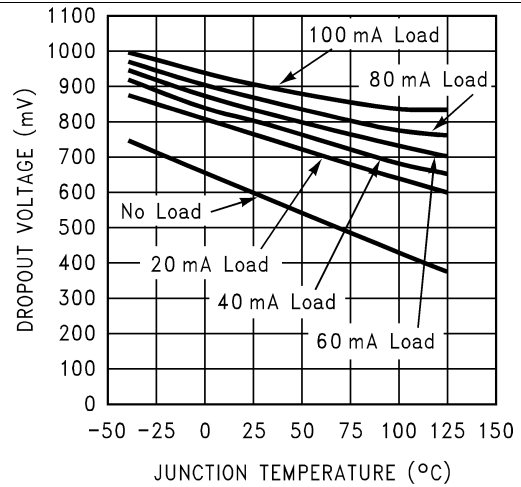


Figure 2. Dropout Voltage vs Junction Temperature

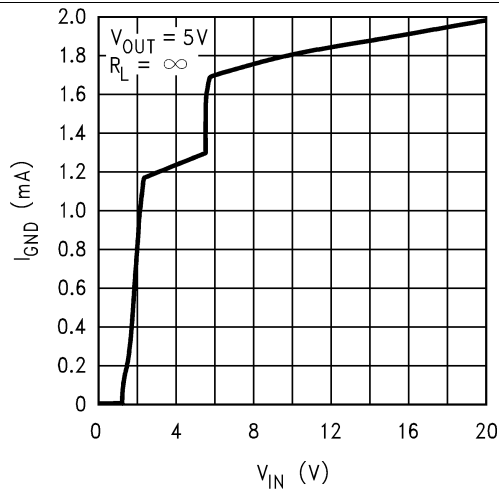


Figure 3. Ground Pin Current vs Input Voltage

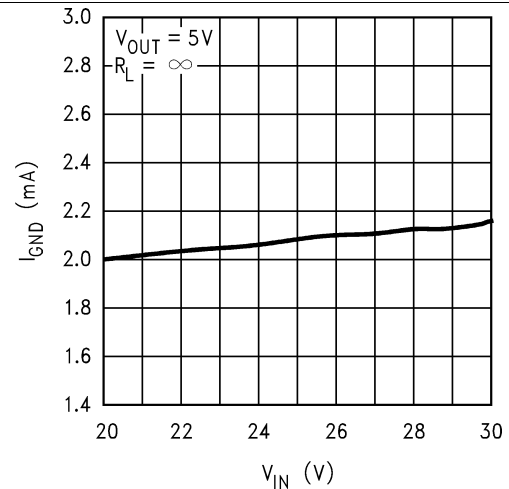


Figure 4. Ground Pin Current vs Input Voltage

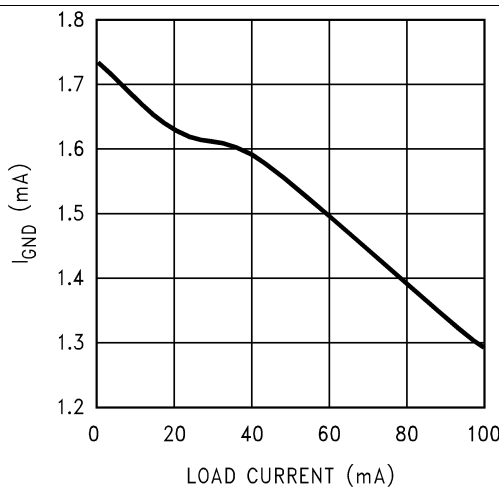


Figure 5. Ground Pin Current vs Load Current

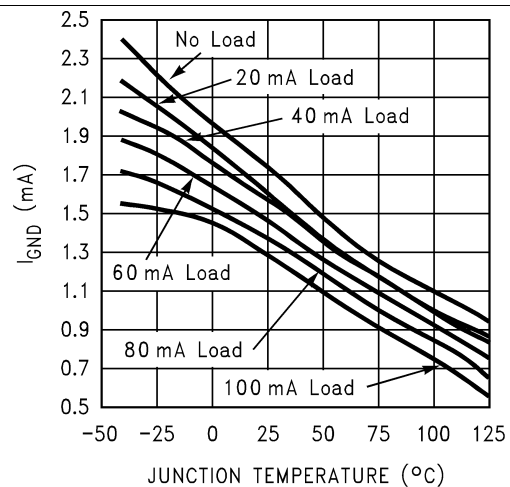


Figure 6. Ground Pin Current vs Junction Temperature

Typical Characteristics (continued)

Unless indicated otherwise, $V_{IN} = V_{NOM} + 1.5\text{ V}$, $C_{IN} = 0.1\ \mu\text{F}$, $C_{OUT} = 0.1\ \mu\text{F}$, and $T_A = 25^\circ\text{C}$.

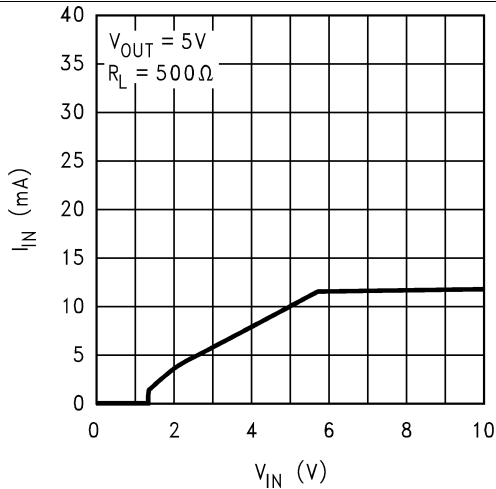


Figure 7. Input Current vs Input Voltage

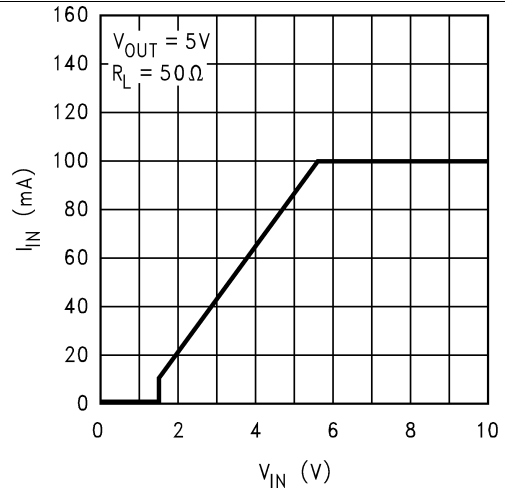


Figure 8. Input Current vs Input Voltage

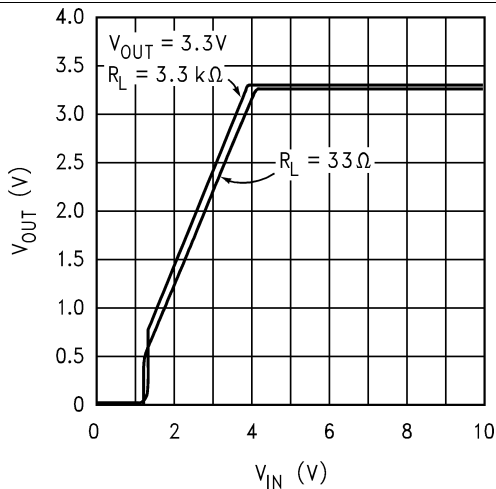


Figure 9. Output Voltage vs Input Voltage

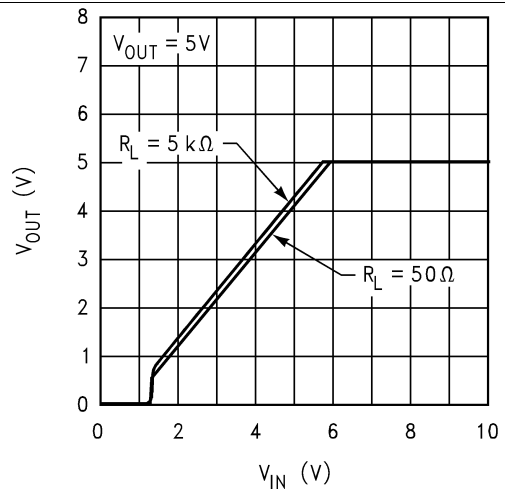


Figure 10. Output Voltage vs Input Voltage

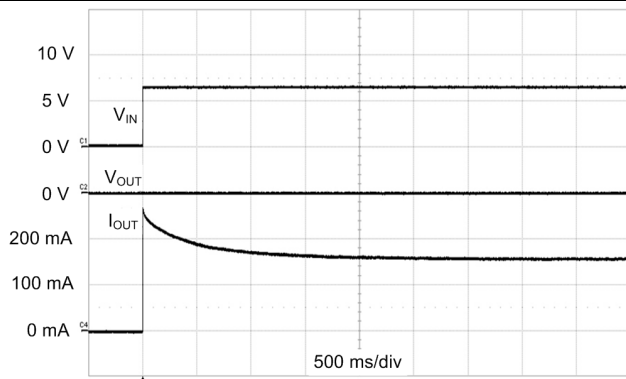


Figure 11. Output Short-Circuit Current

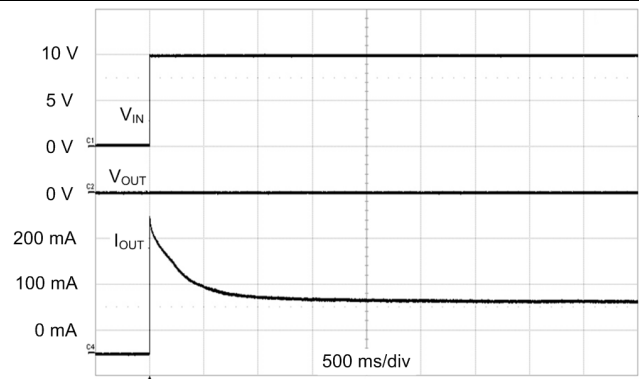


Figure 12. Output Short-Circuit Current

Typical Characteristics (continued)

Unless indicated otherwise, $V_{IN} = V_{NOM} + 1.5\text{ V}$, $C_{IN} = 0.1\ \mu\text{F}$, $C_{OUT} = 0.1\ \mu\text{F}$, and $T_A = 25^\circ\text{C}$.

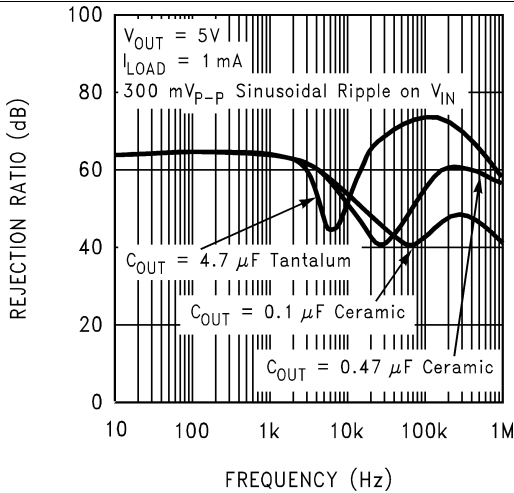


Figure 13. Power Supply Rejection Ratio

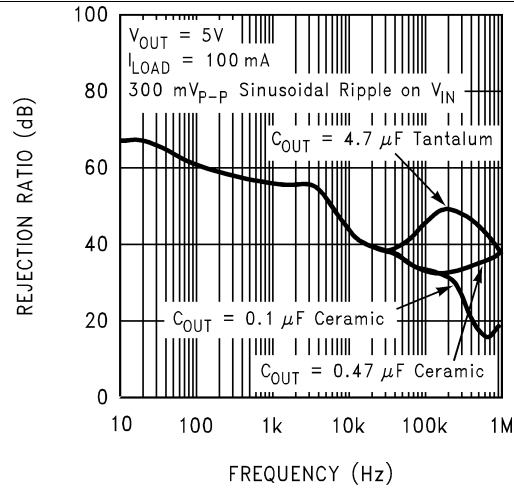


Figure 14. Power Supply Rejection Ratio

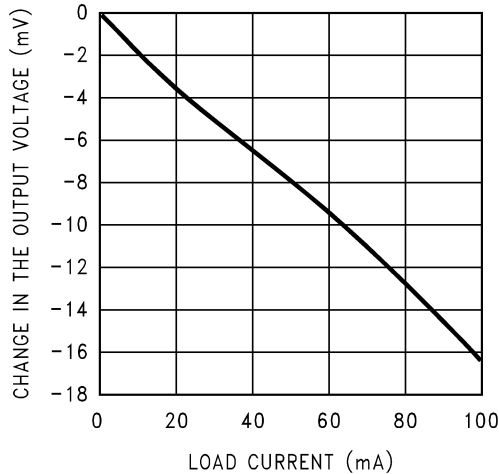


Figure 15. DC Load Regulation

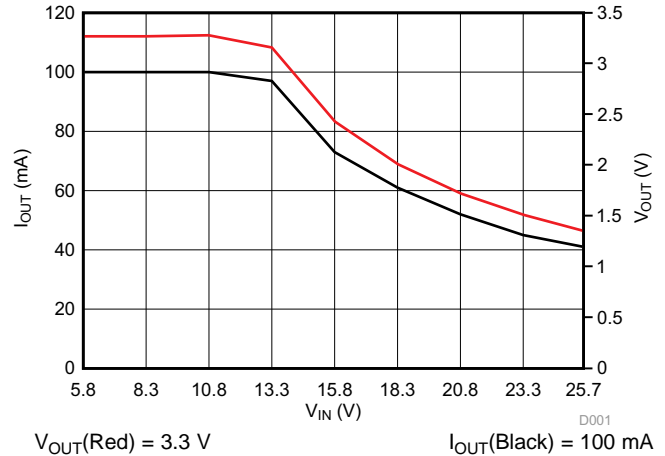


Figure 16. Output Current vs Input Voltage

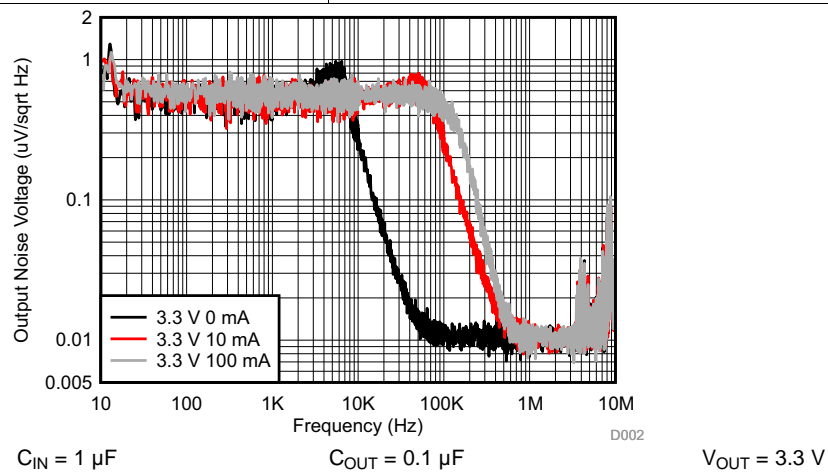


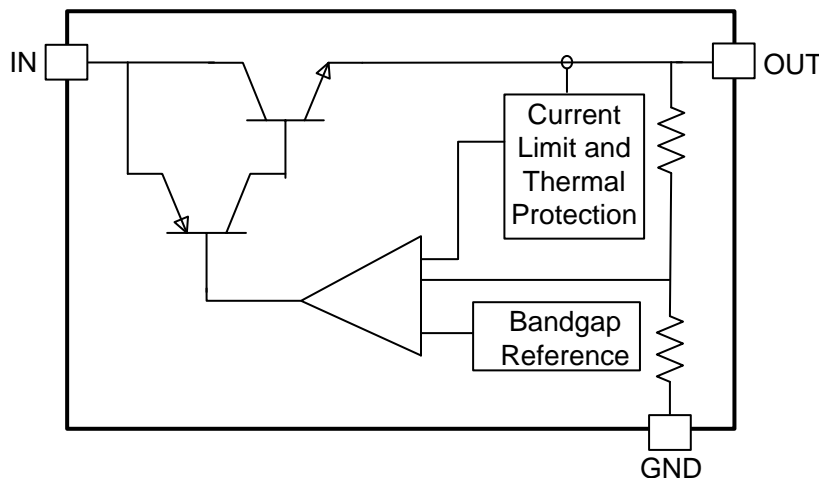
Figure 17. Output Spectral Noise Density vs Frequency

7 Detailed Description

7.1 Overview

The TLV760 is an integrated linear-voltage regulator with inputs that can be as high as 30 V. The TLV760 features [quasi LDO architecture](#), which allows the usage of low ESR capacitors at the output. A ceramic capacitor with a capacitance value greater than or equal to 0.1 μF is adequate to keep the linear regulator in stable operation. The device has a rugged active junction thermal protection mechanism.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Thermal Protection

The TLV760 contains an active thermal protection mechanism, which limits the junction temperature to 150°C. This protection comes into action when the thermal junction temperature of the device tries to exceed 150°C. The output current of the device is limited or folded back to maintain the junction temperature.

The thermal protection follows [Equation 1](#)

$$P_D = (T_J - T_A) / R_{\theta JA}$$

where

- $P_D = (V_{IN} - V_{OUT}) I_{OUT}$
 - T_J is the junction temperature
 - $R_{\theta JA}$ is the junction-to-ambient thermal resistance
- (1)

When a high drop out condition occurs resulting in higher power dissipation across the device the output current is limited to maintain a constant junction temperature of 150°C. This rugged feature protects the device from higher power dissipation applications as well as the short to ground at the output.

This internal protection circuitry of TLV760 is intended to protect the devices against thermal overload conditions. The circuitry is not intended to replace proper heat sinking. Continuously running the TLV760 into thermal protection degrades device reliability.

For reliable operation, limit junction temperature to a maximum of 125°C. To estimate the thermal margin in a given layout, increase the ambient temperature until the thermal protection is triggered using worst case load and highest input voltage conditions.

Feature Description (continued)

7.3.2 Dropout Voltage

The TLV760 is a bipolar device with [quasi LDO architecture](#). Being a bipolar device the dropout voltage of the device does not change significantly with output load current. The device has a maximum dropout across temperature of 1.2 V at 100-mA load current, which is a significant improvement over the traditional LM78Lxx devices.

7.4 Device Functional Modes

7.4.1 Normal Operation

The TLV760 operates with an input up to 30 V. Its tiny SOT-23 package and quasi-LDO architecture makes it suitable for providing a very tiny 100-mA bias supply. The device regulates to the nominal output voltage when all of the following conditions are met.

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$).
- The output current is less than or equal to 100 mA.
- The device junction temperature is less than the thermal protection temperature of 150°C.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV760 is a fixed output device which need only input and output capacitors to function. This section discusses the key aspects to implement this linear regulator in typical applications.

8.1.1 Fixed Output

TLV760 comes in fixed output voltage options, 3.3 V, 5 V, 12 V and 15 V. To ensure the proper regulated output, the input voltage should be greater than $V_{OUT(nom)} + V_{DO}$.

8.1.2 External Capacitors

8.1.2.1 Input and Output Capacitor Requirements

A minimum input and output capacitance value of 0.1 μ F is required for stability and adequate transient performance. There is no specific equivalent series resistance (ESR) limitation, although excessively high ESR compromises transient performance. There is no specific limitation on a maximum capacitance value on the input or the output. However while selecting a capacitor, derating factors on the capacitance value should be considered. Use C0G, X7R, or X5R-type ceramic capacitors because these capacitors have minimal variation in capacitance value and ESR over temperature.

8.1.2.2 Load-Step Transient Response

The load-step transient response is the output voltage response by the linear regulator to a step change in load current. The depth of charge depletion immediately after the load step is directly proportional to the amount of output capacitance. However, larger output capacitances decrease any voltage dip or peak occurring during a load step, the control-loop bandwidth is also decreased, thereby slowing the response time. TI recommends to optimally scale output capacitors for a specific application and test for the output load transients.

8.1.3 Power Dissipation

Proper consideration should be given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane to ensure the device reliability. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses. To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Power dissipation can be calculated using The thermal protection follows [Equation 1](#):

$$P_D = (T_J - T_A) / R_{\theta JA}$$

where

- $P_D = (V_{IN} - V_{OUT}) I_{OUT}$
 - T_J is the junction temperature
 - $R_{\theta JA}$ is the junction-to-ambient thermal resistance
- (2)

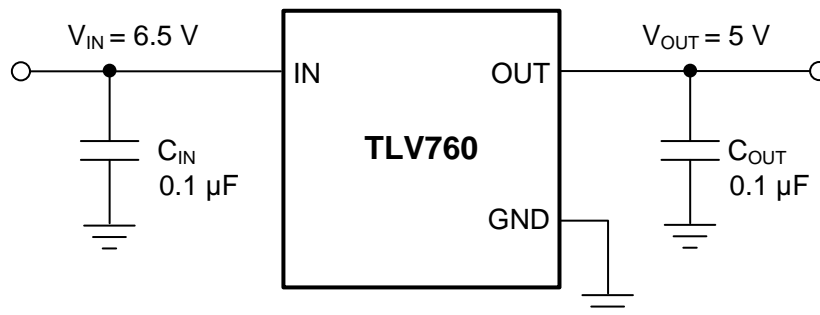
Thus, at a given load current, input and output voltage, maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device, and vice versa. Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$R_{\theta JA}$ is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in [Thermal Information](#) is determined by the JEDEC standard, PCB, and copper-spreading area and is only used as a relative measure of package thermal performance.

Application Information (continued)

TLV760 integrates a rugged protection where the T_J is limited to 150°C. The maximum power dissipation depends on the ambient temperature and can be calculated using $P_D = (T_J - T_A) / R_{\theta JA}$, for example, substituting the absolute maximum junction temperature, 150°C for T_J , 50°C for T_A , and 275.2 °C/W for $R_{\theta JA}$, the maximum power that can be dissipated is 363 mW. More power can be safely dissipated at lower ambient temperatures. Less power can be safely dissipated at higher ambient temperatures. The power dissipation can be increased by 3.6 mW for each °C below 50°C ambient. It must be derated by 3.6 mW for each °C above 50°C ambient. Proper heat sinking enables the safe dissipation of more power.

8.2 Typical Application



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Figure 18. Typical Application for the 5-V Option

8.2.1 Design Requirements

For typical TLV760 applications, use the parameters in [Table 1](#).

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	6.5 V
Output voltage	5 V
Output current	100 mA

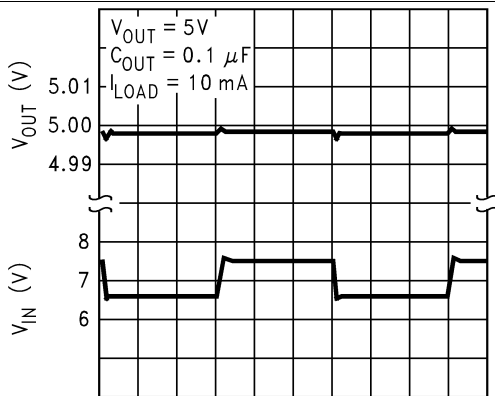
8.2.2 Detailed Design Procedure

The output for TLV76050 is internally set to 5 V. Input and output capacitors can be selected in accordance with the [External Capacitors](#). Ceramic capacitances of 0.1 µF for both input and output are selected.

See the [Layout](#) section for an example of how to PCB layout the TLV760 to achieve best performance.

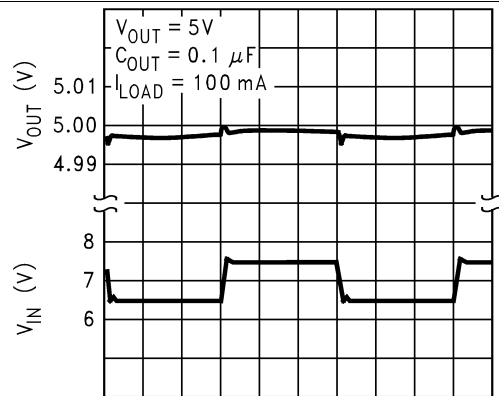
8.2.3 Application Curves

Unless indicated otherwise, $V_{IN} = 6.5\text{ V}$, $V_{OUT} = 5\text{ V}$, $C_{OUT} = 0.1\ \mu\text{F}$, and $T_A = 25^\circ\text{C}$.



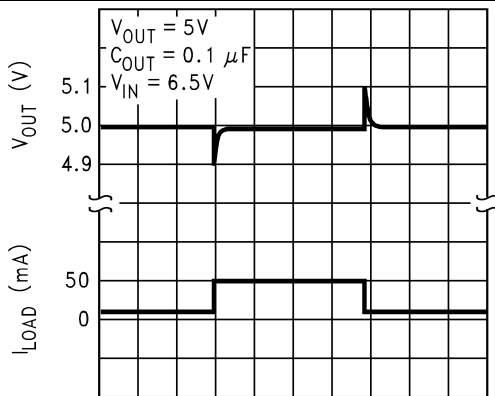
200 $\mu\text{s}/\text{Div}$

Figure 19. Line Transient Response



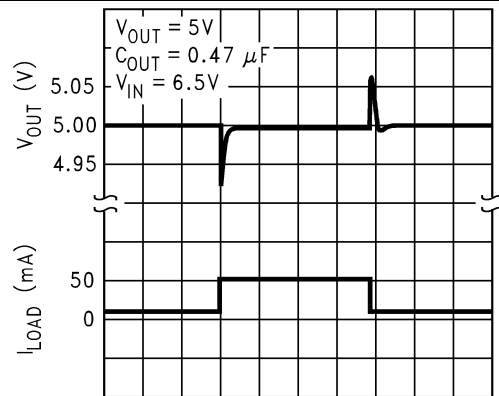
200 $\mu\text{s}/\text{Div}$

Figure 20. Line Transient Response



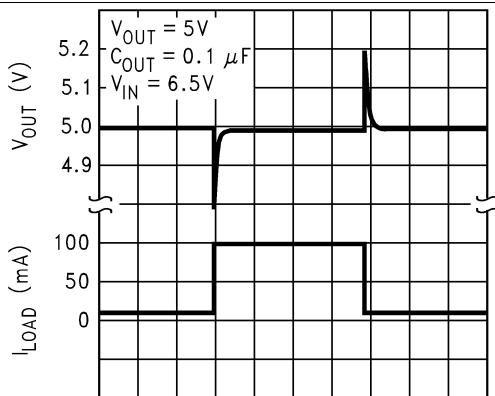
50 $\mu\text{s}/\text{Div}$

Figure 21. Load Transient Response



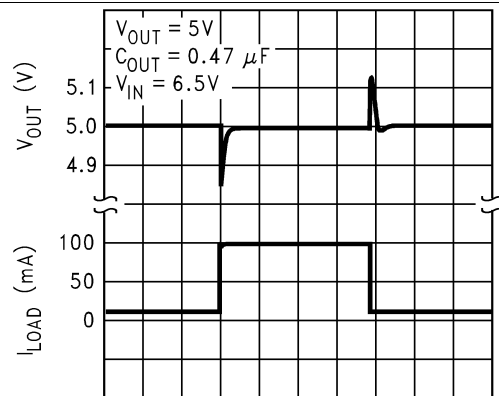
50 $\mu\text{s}/\text{Div}$

Figure 22. Load Transient Response



50 $\mu\text{s}/\text{Div}$

Figure 23. Load Transient Response



50 $\mu\text{s}/\text{Div}$

Figure 24. Load Transient Response

9 Power Supply Recommendations

The TLV760 is designed to operate from input voltage up to 30 V. If the input power supply has ripples, additional input and output capacitors with low ESR can help improve the PSRR at higher frequencies.

10 Layout

10.1 Layout Guidelines

General guidelines for linear regulator designs are to place all circuit components on the same side of the circuit board and as near as practical to the respective TLV760 pin connections. Place ground return connections to the input and output capacitors, and to the TLV760 ground pin as close as possible to each other, connected by a wide, component-side, copper surface. The use of vias and long traces to create TLV760 circuit connections is strongly discouraged and negatively affects system performance.

Use a ground reference plane, either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage and to shield noise; it behaves similarly to a thermal plane to spread heat from the linear regulator. In most applications, this ground plane is necessary to meet thermal requirements.

10.2 Layout Example

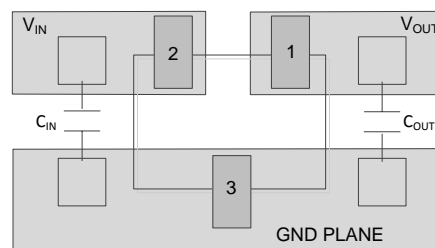


Figure 25. Layout Guideline for TLV760

11 Device and Documentation Support

11.1 Device Support

11.1.1 Related Documentation

For related documentation see the following:

[AN-1148 Linear Regulators: Theory of Operation and Compensation](#)

11.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TLV760 is available through the TLV760 product folder under simulation models.

11.1.3 Device Nomenclature

Table 2. Ordering Information⁽¹⁾

PRODUCT	DESCRIPTION
TLV760XYYYYZ	XX is the voltage designator YYY is the package designator. Z is the package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

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All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV76012DBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	18G	Samples
TLV76012DBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	18G	Samples
TLV76015DBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	18C	Samples
TLV76015DBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	18C	Samples
TLV76033DBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	18H	Samples
TLV76033DBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	18H	Samples
TLV76050DBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	18I	Samples
TLV76050DBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	18I	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV76012DBZR	SOT-23	DBZ	3	3000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
TLV76012DBZT	SOT-23	DBZ	3	250	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
TLV76015DBZR	SOT-23	DBZ	3	3000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
TLV76015DBZT	SOT-23	DBZ	3	250	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
TLV76033DBZR	SOT-23	DBZ	3	3000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
TLV76033DBZT	SOT-23	DBZ	3	250	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
TLV76050DBZR	SOT-23	DBZ	3	3000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
TLV76050DBZT	SOT-23	DBZ	3	250	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

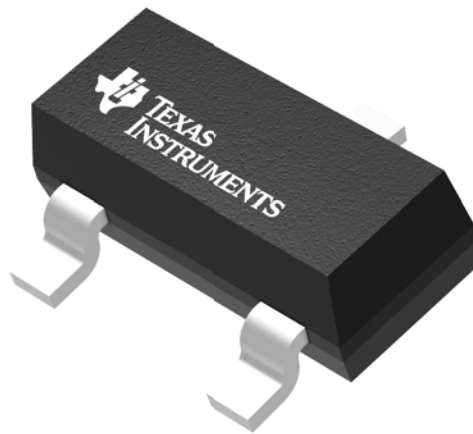
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV76012DBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0
TLV76012DBZT	SOT-23	DBZ	3	250	210.0	185.0	35.0
TLV76015DBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0
TLV76015DBZT	SOT-23	DBZ	3	250	210.0	185.0	35.0
TLV76033DBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0
TLV76033DBZT	SOT-23	DBZ	3	250	210.0	185.0	35.0
TLV76050DBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0
TLV76050DBZT	SOT-23	DBZ	3	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DBZ 3

SOT-23 - 1.12 mm max height

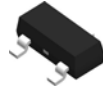
SMALL OUTLINE TRANSISTOR



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203227/C

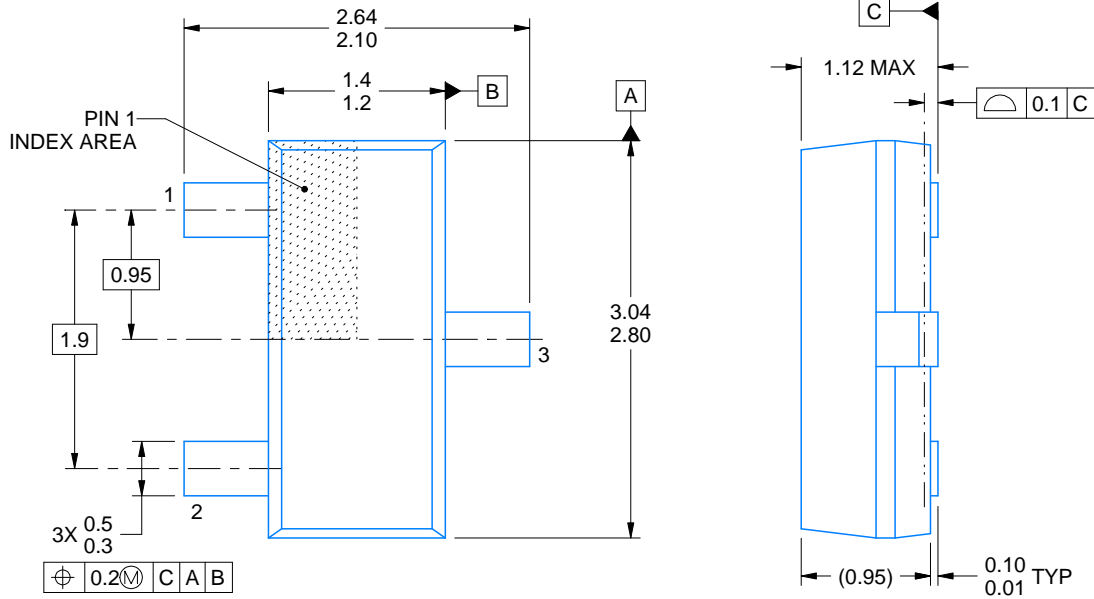
DBZ0003A



PACKAGE OUTLINE

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



4214838/C 04/2017

NOTES:

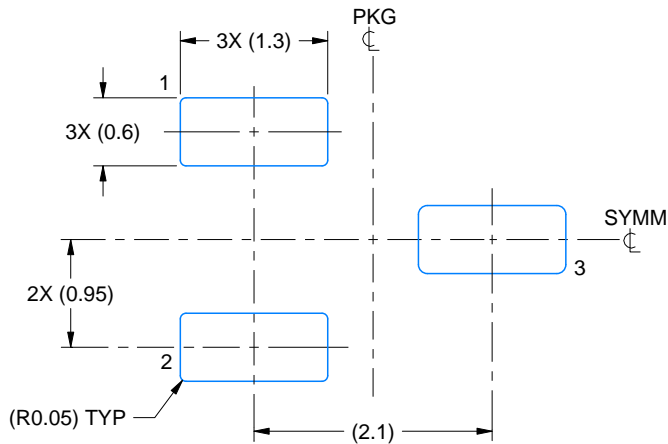
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.

EXAMPLE BOARD LAYOUT

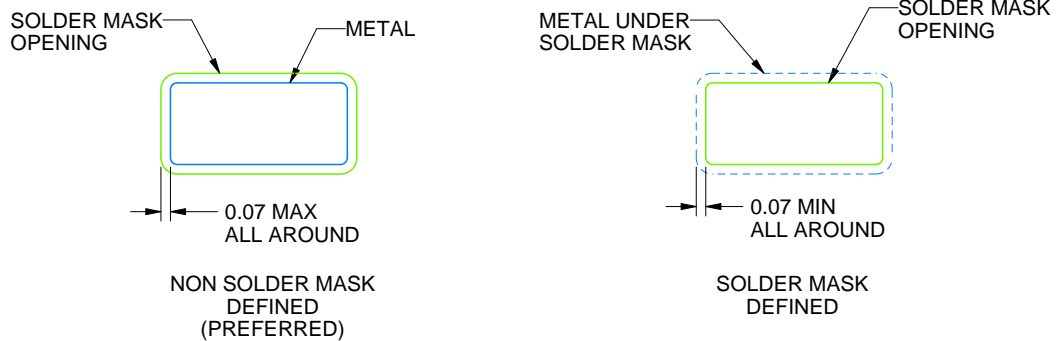
DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

4214838/C 04/2017

NOTES: (continued)

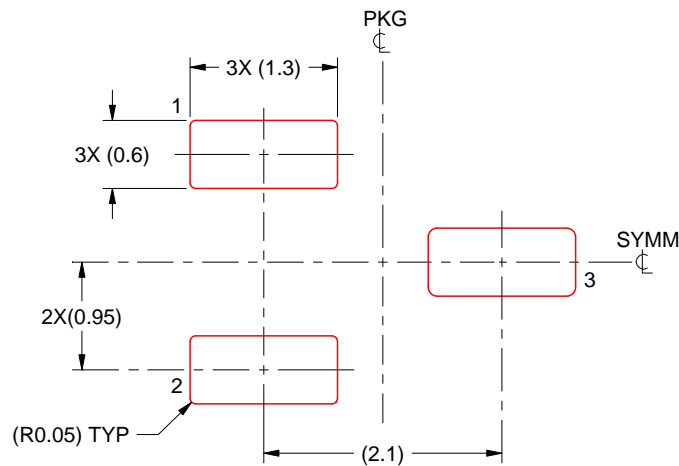
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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