4Gb DDR3L Datasheet

F60C1A0004-M7
Series

Rev 1.3

2019-12

Revision History:

Rev.	Date	Change	Remark
1.0	2019/09	Basic spec and architecture	
1.1	2019/11	Add 2133Mbps product	
1.2	2019/12	Correct some error descriptions	
1.3	2019/12	Change Figure2 & Figure3	

Contents

1. INTRODUCTION

1.1. General Description

The FORESEE DDR3L SDRAM (1.35V) is a low voltage version of the DDR3 (1.5V) SDRAM. Refer to the DDR3 (1.5V) SDRAM datasheet specifications when running in 1.5V compatible mode.

1.2. Device Features

- **Density: 4G bits**
- **Organization**
  - 8 banks x 64M words x 8 bits
  - 8 banks x 32M words x 16 bits
- **Package**
  - 78-ball FBGA
  - 96-ball FBGA
- **Lead-free(RoHS compliant) and Halogen-free**
- **Power supply**
  - VDD, VDDQ =1.35V (1.283 to 1.45V)
  - Backward compatible DDR3 (1.5V) operation
- **Data Rate: 1600Mbps/1866Mbps/2133Mbps**
- **1KB page size (x8)**
  - Row address: AX0 to AX15
  - Column address: AY0 to AY9
- **2KB page size (x16)**
  - Row address: AX0 to AX14
  - Column address: AY0 to AY9
- **Eight internal banks for concurrent operation**
- **Burst lengths(BL): 8 and 4 with Burst Chop(BC)**
- **Burst type(BT)**
  - Sequential (8, 4 with BC)
  - Interleave (8, 4 with BC)
- **CAS Latency (CL): 5, 6, 7, 8, 9, 10, 11, 12, 13, 14**
- **CAS Write Latency (CWL): 5, 6, 7, 8, 9, 10**
- **Precharge: auto precharge option for each burst access**
- **Driver strength: RZQ/7, RZQ/6 (RZQ = 240Ω)**
- **Refresh: auto-refresh, self-refresh**
- **Average refresh period**
  - 7.8us at TC ≤ +85℃
  - 3.9us at TC > +85℃
- **Operating temperature range**
  - TC = 0°C to +85°C (Commercial grade)
- **The high-speed data transfer is realized by the 8bits prefetch pipelined architecture**
- **Double data-rate architecture: two data transfers per clock cycle**
- **Bi-directional differential data strobe (DQS and DQS#) is transmitted/received with data for capturing data at the receiver**
- **DQS is edge-aligned with data for READs; center aligned with data for WRITEs**
- **Differential clock inputs (CK and CK#)**
- **DLL aligns DQ and DQS transitions with CK transitions**
- **Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS**
- **Data mask (DM) for write data**
- **Posted CAS by programmable additive latency for better command and data bus efficiency**
- **On-Die Termination (ODT) for better signal quality**
  - Synchronous ODT
  - Dynamic ODT
  - Asynchronous ODT
- **Multi Purpose Register (MPR) for pre-defined pattern read out**
- **ZQ calibration for DQ drive and ODT Access**
- **Programmable partial array self-refresh (PASR)**
- **RESET pin for Power-up sequence and reset function**
- **SRT(Self Refresh Temperature) range**
  - Normal/Extended/ASR
- **Programmable output driver impedance control**
- **JEDEC compliant DDR3**
- **RH-Free(Row Hammer Free) option is available**

[Table 1]Key Timing Parameters

Data Rate(Mbps)	CL	tRCD	tRP
2133	14	14	14
1866	13	13	13
1600	11	11	11

1.3. Product List

[Table 2] Product List

Part Number	Density	Package Type	Organization	Package Size(mm)	VCC Range	Data Rate(Mbps)
F60C1A0004-M7 9R	4Gb	FBGA 96	×16bit	7.5*13.5	1.283V ~ 1.45V	1866
F60C1A0004-M7 AR	4Gb	FBGA 96	×16bit	7.5*13.5	1.283V ~ 1.45V	2133

Marketing Part Number Chart

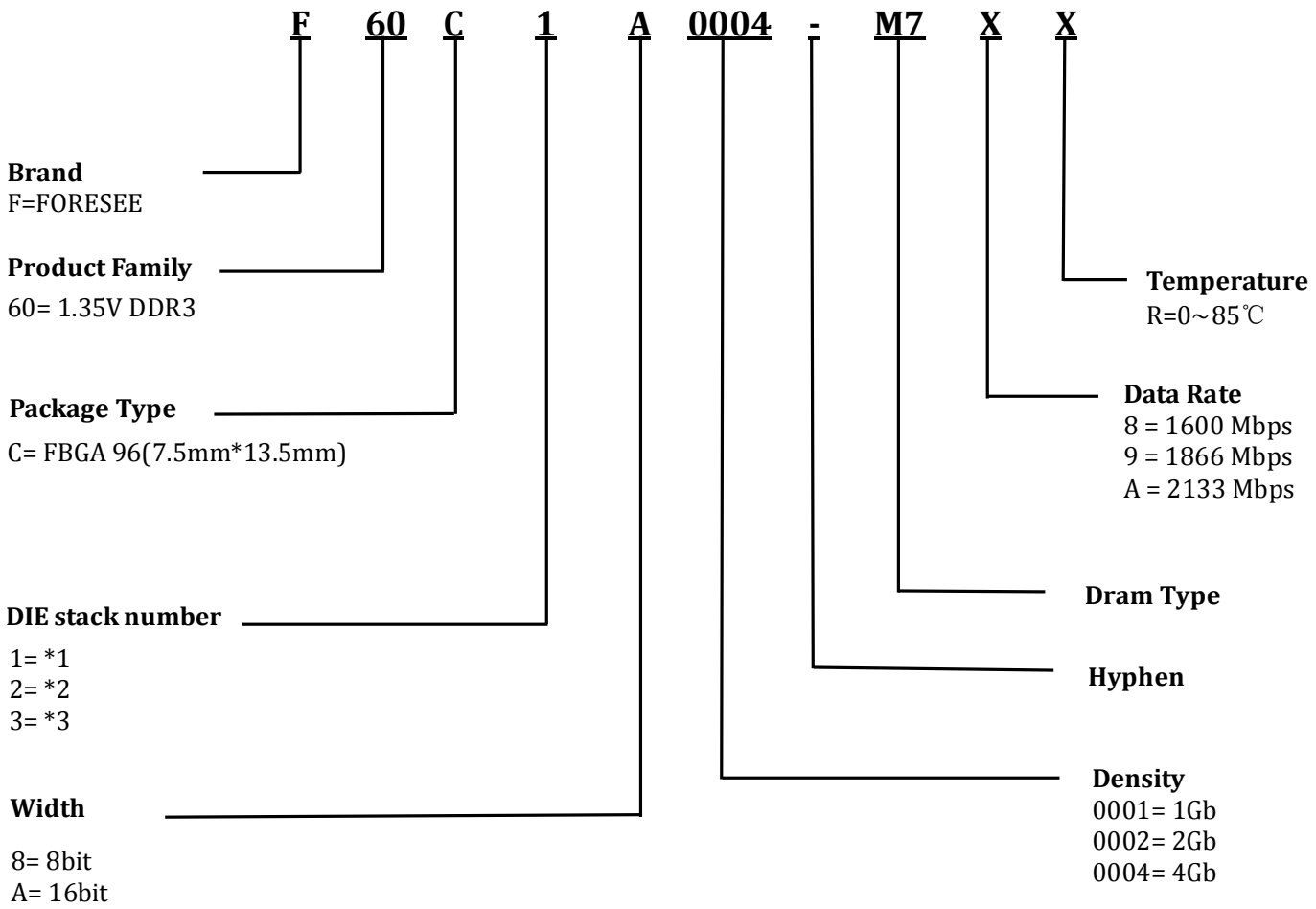


Figure 1 Part Number

1.4. Connection Diagram

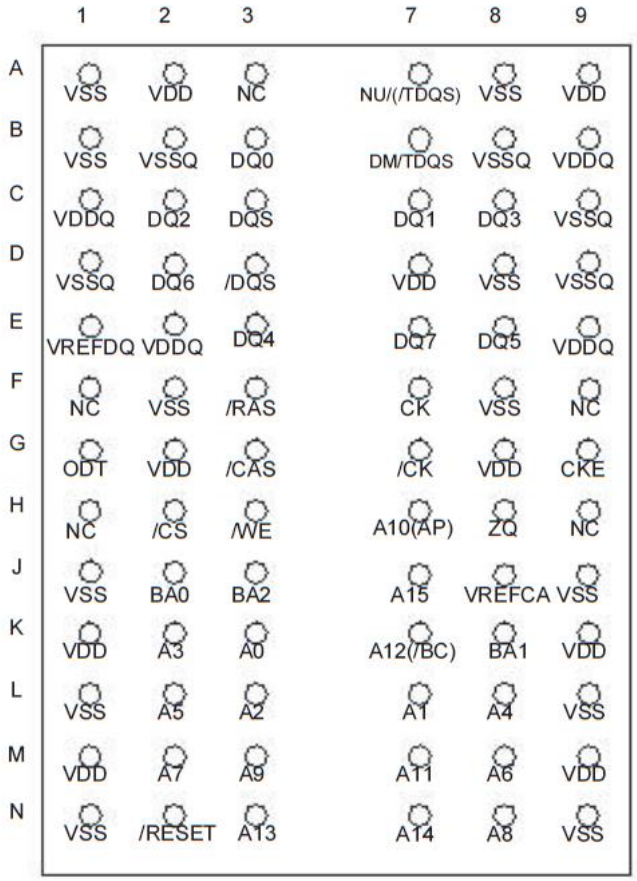


Figure 2 78ball FBGA(x8 organization) top view

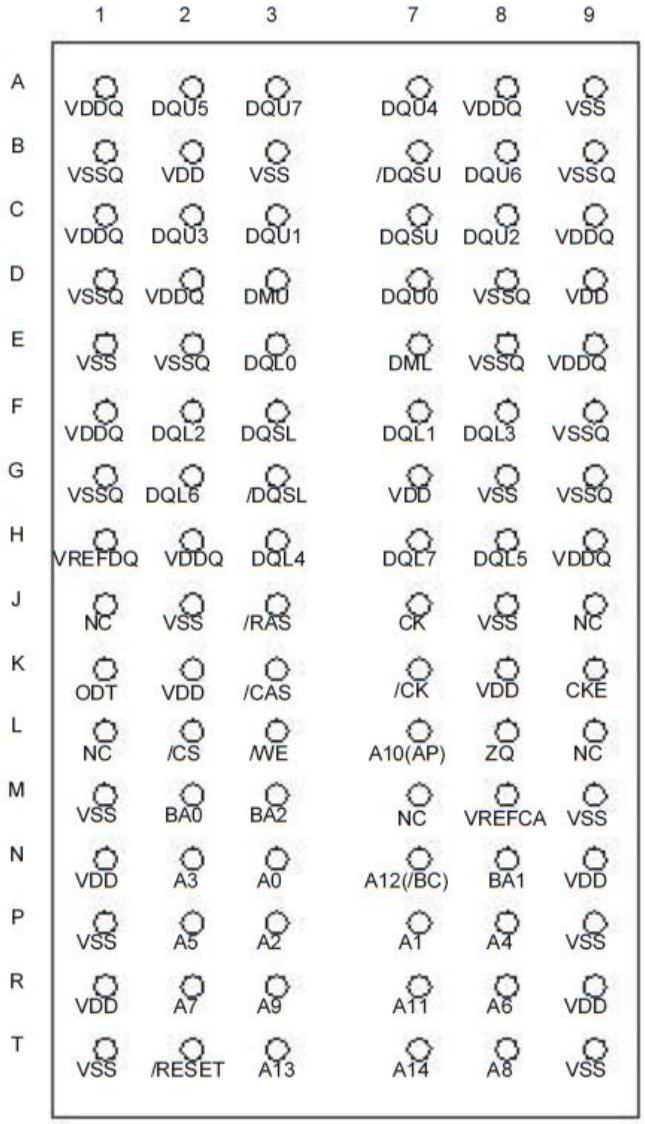


Figure 3 96ball FBGA(x16 organization) top view

1.5. Pin Description

[Table 3] 78-Ball FBGA – x8 Ball Descriptions

Symbol	Type	Description
A[15:13], A12, A11, A10/AP, A[9:0]	Input	Address inputs: Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to VREFCA. A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop, LOW = BC4).
BA[2:0]	Input	Bank address inputs: BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to VREFCA.
CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All control and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (DQS, DQS#) is referenced to the crossings of CK and CK#.
CKE	Input	Clock enable: CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/ disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during POWER-DOWN. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to VREFCA.
CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS# is considered part of the command code. CS# is referenced to VREFCA.
DM	Input	Input data mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with the input data during a write access. Although the DM ball is input-only, the DM loading is designed to match that of the DQ and DQS balls. DM is referenced to VREFDQ. DM has an optional use.
ODT	Input	On-die termination: ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls: DQ[7:0], DQS, DQS#, and DM for the x8; DQ[3:0], DQS, DQS#, and DM for the x4. The ODT input is ignored if disabled via the LOAD MODE command. ODT is referenced to VREFCA.
RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered and are referenced to VREFCA.
RESET#	Input	Reset: RESET# is an active LOW CMOS input referenced to VSS. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × VDD and DC LOW ≤ 0.2 × VDDQ. RESET# assertion and desertion are asynchronous.

[Table 4] 78-Ball FBGA –x8 Ball Descriptions (Continued)

Symbol	Type	Description
DQ[7:0]	I/O	Data input/output: Bidirectional data bus for the x8 configuration. DQ[7:0] are referenced to VREFDQ.
DQS, DQS#	I/O	Data strobe: Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data.
VDD	Supply	Power supply: 1.5V ±0.075V.
VDDQ	Supply	DQ power supply: 1.5V ±0.075V. Isolated on the device for improved noise immunity.
VREFCA	Supply	Reference voltage for control, command, and address: VREFCA must be maintained at all times(including self refresh) for proper device operation.
VREFDQ	Supply	Reference voltage for data: VREFDQ must be maintained at all times (excluding self refresh) for proper device operation.
VSS	Supply	Ground.
ZQ	Reference	External reference ball for output drive calibration: This ball is tied to an external 240Ω resistor (RZQ), which is tied to VSSQ.
NC	–	No connect: These balls should be left unconnected (the ball has no connection to the DRAM or to other balls).

[Table 5] 96-Ball FBGA – x16 Ball Descriptions

Symbol	Type	Description
A[15:13], A12, A11, A10, A[9:0]	Input	Address inputs: Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to VREFCA. A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop, LOW = BC4).
BA[2:0]	Input	Bank address inputs: BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to VREFCA.
CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All control and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (DQS, DQS#) is referenced to the crossings of CK and CK#.
CKE	Input	Clock enable: CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/ disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during POWER-DOWN. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to VREFCA.
CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CSB is considered part of the command code. CS# is referenced to VREFCA.
DML	Input	Input data mask: DML is a lower-byte, input mask signal for write data. Lower-byte input data is masked when DML is sampled HIGH along with the input data during a write access. Although the DML ball is input-only, the DML loading is designed to match that of the DQ and DQS balls. DML is referenced to VREFDQ.
ODT	Input	On-die termination: ODT enables (registered HIGH) and disables (registered LOW) Termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls: DQL/DQU[7:0], DQSL, DQSL#, DQSU,DQSU#, DML, and DMU for the x16. The ODT input is ignored if disabled via the LOAD MODE command. ODT is referenced to VREFCA.
RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WEB (along with CS#) define the command being entered and are referenced to VREFCA.
RESET#	Input	Reset: RESET# is an active LOW CMOS input referenced to VSS. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × VDD and DC LOW ≤ 0.2 × VDDQ. RESET# assertion and desertion are asynchronous.

[Table 6] 96-Ball FBGA –x16 Ball Descriptions (Continued)

Symbol	Type	Description
DMU	Input	Input data mask: DMU is an upper-byte, input mask signal for write data. Upper byte input data is masked when DMU is sampled HIGH along with that input data during a WRITE access. Although the DMU ball is input-only, the DMU loading is designed to match that of the DQ and DQS balls. DMU is referenced to VREFDQ.
DQL[7:0]	I/O	Data input/output: Bidirectional data bus for the x16 configuration. DQL[7:0] are referenced to VREFDQ.
DQU[7:0]	I/O	Data input/output: Bidirectional data bus for the x16 configuration. DQU[7:0] are referenced to VREFDQ.
DQSL, DQSL#	I/O	Data strobe: Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data.
DQSU, DQSU#	I/O	Data strobe: Output with read data. Edge-aligned with read data. Input with write data. DQS is Center-aligned to write data.
VDD	Supply	Power supply: 1.5V ±0.075V.
VDDQ	Supply	DQ power supply: 1.5V ±0.075V. Isolated on the device for improved noise immunity.
VREFCA	Supply	Reference voltage for control, command, and address: VREFCA must be maintained at all times(including self refresh) for proper device operation.
VREFDQ	Supply	Reference voltage for data: VREFDQ must be maintained at all times (excluding self refresh) for proper device operation.
VSS	Supply	Ground.
ZQ	Reference	External reference ball for output drive calibration: This ball is tied to an external 240Ω resistor (RZQ), which is tied to VSSQ.
NC	–	No connect: These balls should be left unconnected (the ball has no connection to the DRAM or to other balls).

1.6. System Block Diagram

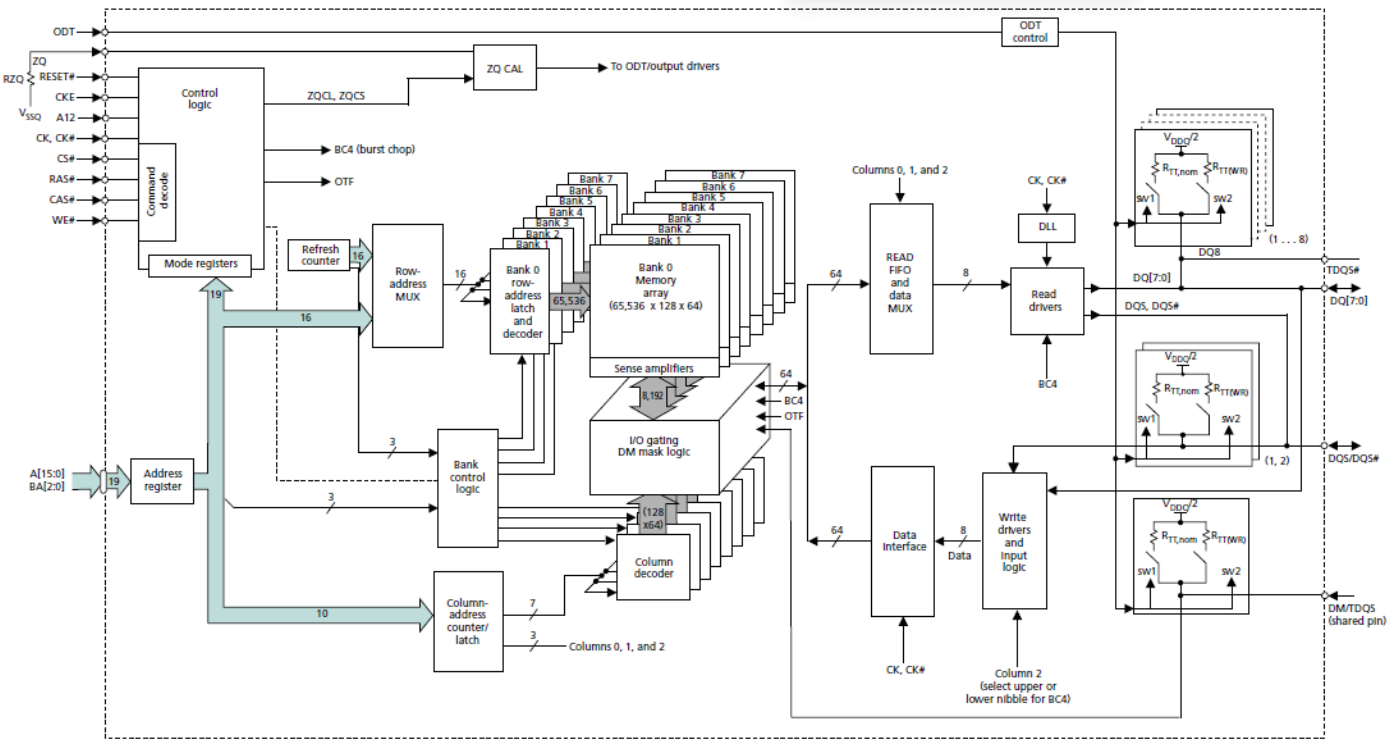


Figure 4 512M×8 Functional Block Diagram

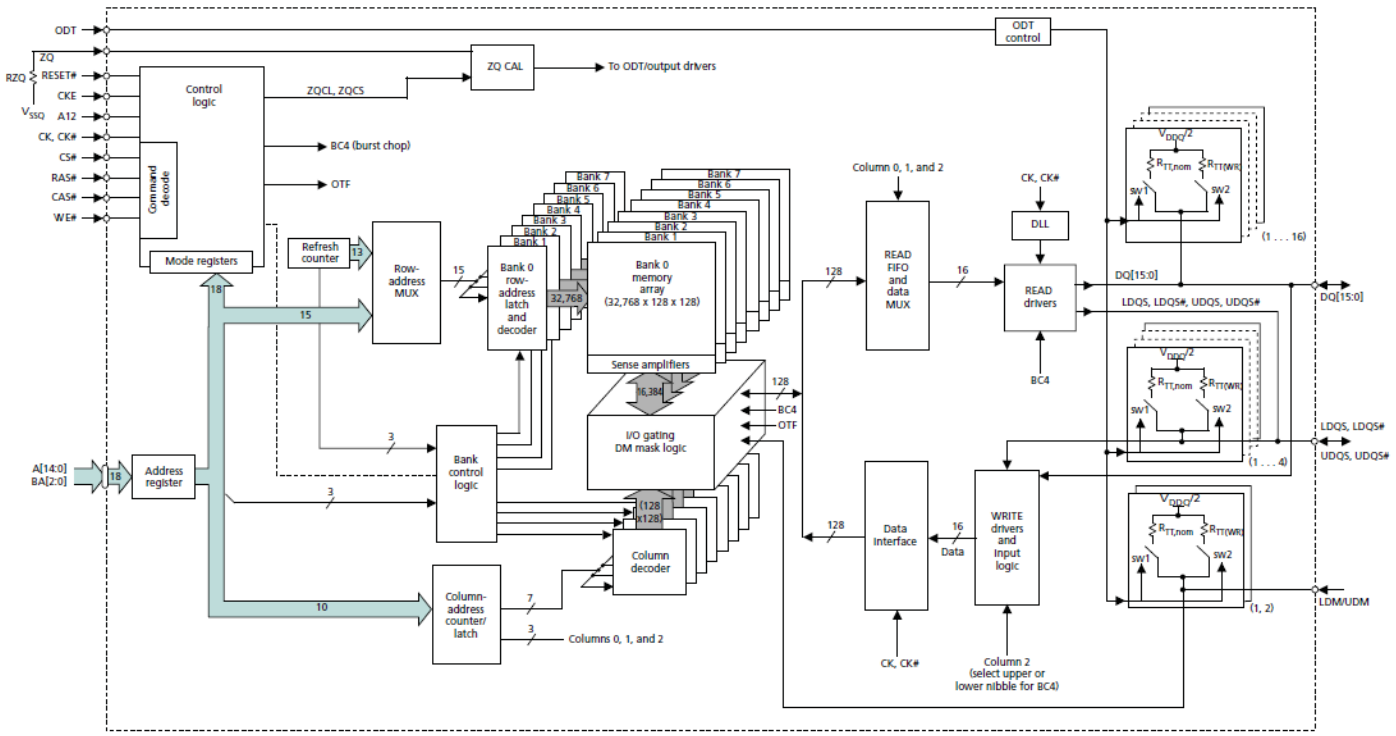


Figure 5 256M×16 Functional Block Diagram

2. COMMAND OPERATION

2.1. Command Sets

The DDR3 SDRAM recognizes the following commands specified by the CS#, RAS#, CAS#, WE# and address pins.

[Table 7] Command Truth Table

Function	Symbol	CKE		CS#	RAS#	CAS#	WE#	BA0-2	A12(/BS)	A10(AP)	A0-A15	Note
		Previous	Current									
Mode register set	MRS	H	H	L	L	L	L	BA	op-code			
Auto refresh	REF	H	H	L	L	L	H	V	V	V	V	
Self refresh entry	SELF	H	L	L	L	L	H	V	V	V	V	6,8,11
Self refresh exit	SELEX	L	H	H	X	X	X	X	X	X	X	6,8,7
		L	H	L	H	H	H	V	V	V	V	11
Single bank precharge	PRE	H	H	L	L	H	L	BA	V	L	V	
Precharge all banks	PALL	H	H	L	L	H	L	V	V	H	V	
Bank activate	ACT	H	H	L	L	H	H	BA	RA			12
Write(Fixed BL)	WRIT	H	H	L	H	L	L	BA	V	L	CA	
Write(BC4,on the fly)	WRS4	H	H	L	H	L	L	BA	L	L	CA	
Write(BL8,on the fly)	WRS8	H	H	L	H	L	L	BA	H	L	CA	
Write with auto precharge (Fixed BL)	WRITA	H	H	L	H	L	L	BA	V	H	CA	
Write with auto precharge (BC4,on the fly)	WRAS4	H	H	L	H	L	L	BA	L	H	CA	
Write with auto precharge (BL8,on the fly)	WRAS8	H	H	L	H	L	L	BA	H	H	CA	
Read(Fixed BL)	READ	H	H	L	H	L	H	BA	V	L	CA	
Read(BC4,on the fly)	RDS4	H	H	L	H	L	H	BA	L	L	CA	
Read(BL8,on the fly)	RDS8	H	H	L	H	L	H	BA	H	L	CA	
Read with auto precharge (Fixed BL)	READA	H	H	L	H	L	H	BA	V	H	CA	
Read with auto precharge (BC4,on the fly)	RDAS4	H	H	L	H	L	H	BA	L	H	CA	
Read with auto precharge (BL8,on the fly)	RDAS8	H	H	L	H	L	H	BA	H	H	CA	
No operation	NOP	H	H	L	H	H	H	V	V	V	V	9
Device deselect	DESL	H	H	H	X	X	X	X	X	X	X	10
Power down mode entry	PDEN	H	L	H	X	X	X	X	X	X	X	5,11
		H	L	L	H	H	H	V	V	V	V	
Power down mode exit	PDEX	L	H	H	X	X	X	X	X	X	X	5,11
		L	H	L	H	H	H	V	V	V	V	
ZQ calibration long	ZQCL	H	H	L	H	H	L	X	X	H	X	
ZQ calibration short	ZQCS	H	H	L	H	H	L	X	X	L	X	

Remark:
[1] H = VIH; L = VIL; V =VIH or VIL(defined logical level).
[2] X = Don't care (defined or undefined, including floating around VREF) logical level. [3] BA = Bank Address. RA = Row Address. CA = Column Address. /BC = Bust Chop.
Notes:
[1] All DDR3 commands are defined by states of CS#, RAS#, CAS#, WE# and CKE at the rising edge of the clock. The most significant bit (MSB) of BA, RA, and CA are device density and configuration dependent.
[2] RESET# is an active low asynchronous signal that must be driven high during normal operation.
[3] Bank Addresses (BA) determines which bank is to be operated upon. For MRS, BA selects a mode register.
[4] Burst READs or WRITEs cannot be terminated or interrupted and fixed/on the fly BL will be defined by MRS.
[5] The power-down mode does not perform any refresh operations.
[6] The state of ODT does not affect the states described in this table. The ODT function is not available during self-refresh.
[7] Self-refresh exit is asynchronous.
[8] VREF (both VREFDQ and VREFCA) must be maintained during self-refresh operation. VREFDQ supply may be turned off and VREFDQ may take any value between VSS and VDD during self-refresh operation, provided that VREFDQ is valid and stable prior to CKE going back high and that first write operation or first write leveling activity may not occur earlier than 512 nCK after exit from self-refresh.
[9] The No Operation command (NOP) should be used in cases when the DDR3 SDRAM is in an idle or a wait state. The purpose of the NOP command is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. A NOP command will not terminate a previous operation that is still executing, such as a burst read or write cycle.
[10] The DESL command performs the same function as a NOP command.
[11] Refer to the CKE Truth Table for more detail with CKE transition.
[12]. No more than 4 banks may be activated in a rolling tFAW window. Converting to clocks is done by dividing tFAW (ns) by tCK (ns) and rounding up to next integer value. As an example of the rolling window, if (tFAW/tCK) rounds up to 10 clocks, and an activate command is issued in clock N, no more than three further activate commands may be issued in clock N+1 through N+9.

2.2. No Operation Command [NOP]

The No Operation command (NOP) should be used in cases when the DDR3 SDRAM is in an idle or a wait state. The purpose of the NOP command is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. A NOP command will not terminate a previous operation that is still executing, such as a burst read or write cycle.
The no operation (NOP) command is used to instruct the selected DDR3 SDRAM to perform a NOP (CS# low, RAS#, CAS#, WE# high). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

2.3. Device Deselect Command [DESL]

The deselect function (CS# high) prevents new commands from being executed by the DDR3 SDRAM. The DDR3 SDRAM is effectively deselected. Operations already in progress are not affected.

2.4. Mode Register Set Command [MR0 to MR3]

The mode registers are loaded via row address inputs. See mode register descriptions in the Programming the mode register section. The mode register set command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until tMRD is met.

2.5. Bank Activate Command [ACT]

This command is used to open (or activate) a row in a particular bank for a subsequent access. The values on the BA inputs select the bank, and the address provided on row address inputs selects the row. This row remains active (or open) for accesses until a precharge command is issued to that bank. A precharge command must be issued before opening a different row in the same bank.

Note: No more than 4 banks may be activated in a rolling tFAW window. Converting to clocks is done by dividing tFAW (ns) by tCK (ns) and rounding up to next integer value. As an example of the rolling window, if (tFAW/tCK) rounds up to 10 clocks, and an activate command is issued in clock N, no more than three further activate commands may be issued in clock N+1 through N+9.

2.6. Read Command [READ, RDS4, RDS8, READA, RDAS4, RDAS8]

The read command is used to initiate a burst read access to an active row. The values on the BA inputs select the bank, and the address provided on column address inputs selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the read burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

2.7. Write Command [WRIT, WRS4, WRS8, WRITA, WRAS4, WRAS8]

The write command is used to initiate a burst write access to an active row. The values on the BA inputs select the bank, and the address provided on column address inputs selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the write burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQ is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered low, the corresponding data will be written to memory; if the DM signal is registered high, the corresponding data inputs will be ignored, and a write will not be executed to that byte/column location.

2.8. Precharge Command [PRE, PALL]

The precharge command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (tRP) after the precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA select the bank. Otherwise BA are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any read or write commands being issued to that bank. A precharge command will be treated as a NOP if there is no open row in that bank (idle state), or if the previously open row is already in the process of precharging.

2.9. Auto precharge Command [READA, WRITA]

Before a new row in an active bank can be opened, the active bank must be precharged using either the precharge command or the auto precharge function. When a read or a write command is given to the DDR3 SDRAM, the CAS# timing accepts one extra address, column

address A10, to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle. If A10 is low when the read or write command is issued, then normal read or write burst operation is executed and the bank remains active at the completion of the burst sequence. If A10 is high when the read or write command is issued, then the auto precharge function is engaged. During auto precharge, a read command will execute as normal with the exception that the active bank will begin to precharge on the rising edge which is (AL* + tRTP) cycles later from the read with auto precharge command.
Auto precharge can also be implemented during write commands. The precharge operation engaged by the Auto precharge command will not begin until the last data of the burst write sequence is properly stored in the memory array.
This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon CAS# latency) thus improving system performance for random data access. The tRAS lockout circuit internally delays the Precharge operation until the array restore operation has been completed so that the auto precharge command may be issued with any read or write command.
Note: AL (Additive Latency), refer to Posted CAS# description in the Register Definition section.

2.10. Auto-Refresh Command [REF]

Auto-refresh is used during normal operation of the DDR3 SDRAM and is analogous to CAS#-before-RAS# (CBR) refresh in FPM/EDO DRAM. This command is non persistent, so it must be issued each time a refresh is required. The addressing is generated by the internal refresh controller. This makes the address bits a "Don't Care" during an auto-refresh command.
A maximum of eight auto-refresh commands can be posted to any given DDR3, meaning that the maximum absolute interval between any auto-refresh command and the next auto-refresh command is 9 x tREFI. This maximum absolute interval is to allow DDR3 output drivers and internal terminators to automatically recalibrate compensating for voltage and temperature changes.

2.11. Self-Refresh Command [SELF]

The self-refresh command can be used to retain data in the DDR3, even if the rest of the system is powered down. When in the self-refresh mode, the DDR3 retains data without external clocking. The self-refresh command is initiated like an auto-refresh command except CKE is disabled (low).
The DLL is automatically disabled upon entering self-refresh and is automatically enabled and reset upon exiting self-refresh. The active termination is also disabled upon entering self-refresh and enabled upon exiting self-refresh. (512 clock cycles must then occur before a read command can be issued). Input signals except CKE are "Don't Care" during self-refresh. The procedure for exiting self-refresh requires a sequence of commands.
First, CK and /CK must be stable prior to CKE going back high. Once CKE is high, the DDR3 must have NOP commands issued for tXS DLL because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh, DLL requirements and out-put calibration is to apply NOPs for 512 clock cycles before applying any other command to allow the DLL to lock and the output drivers to recalibrate.

2.12. ZQ calibration Command [ZQCL, ZQCS]

ZQ calibration command (short or long) is used to calibrate DRAM RON and ODT values over PVT. ZQ Calibration Long (ZQCL) command is used to perform the initial calibration during power-up initialization sequence.
ZQ Calibration Short (ZQCS) command is used to perform periodic calibrations to account for VT variations. All banks must be precharged and tRP met before ZQCL or ZQCS commands are issued by the controller.
ZQ calibration commands can also be issued in parallel to DLL lock time when coming out of self-refresh.

2.13. CKE Truth Table

[Refer to section 4.2 in JEDEC Standard No. JESD79-3F]

3. Electrical Characteristic

All voltages are referenced to each VSS (GND).
Execute power-up and Initialization sequence before proper device operation can be achieved.

3.1. Absolute Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

[Table 8] Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
VDD	VDD supply voltage relative to VSS	–0.4	1.975	V	1
VDDQ	VDD supply voltage relative to VSSQ	–0.4	1.975	V	
VIN, VOUT	Voltage on any pin relative to VSS	–0.4	1.975	V	
TC	Operating case temperature – Commercial	0	95	°C	2, 3
	Operating case temperature – Industrial	–40	95	°C	2, 3
TSTG	Storage temperature	–55	150	°C	

Notes:
[1] VDD and VDDQ must be within 300mV of each other at all times, and VREF must not be greater than 0.6 × VDDQ. When VDD and VDDQ are <500mV, VREF can be ≤300mV.
[2] MAX operating case temperature. TC is measured in the center of the package.
[3] Device functionality is not guaranteed if the DRAM device exceeds the maximum TC during operation.

3.2. Operating Temperature Condition

[Table 9] Operating Temperature Condition

Product grades	Parameter	Symbol	Rating	Unit	Note
Commercial	Operating case temperature	TC	0 to +85	℃	1,2,3,4

Notes:
[1] MAX operating case temperature TC is measured in the center of the package, as shown below.
[2] A thermal solution must be designed to ensure that the device does not exceed the maximum TC during operation.
[3] Device functionality is not guaranteed if the device exceeds maximum TC during operation.
[4] If TC exceeds 85℃, the DRAM must be refreshed externally at 2x refresh, which is a 3.9μs interval refresh rate. The use of self refresh temperature (SRT) or automatic self refresh (ASR), must be enabled.

3.3. Recommended DC Operating Conditions

[Table 10] Recommended DC operating Conditions for DDR3L (1.35V)

Parameter	Symbol	min.	typ.	max.	Unit	Note
Supply voltage	VDD	1.283	1.35	1.45	V	1,2
Supply voltage for DQ	VDDQ	1.283	1.35	1.45	V	1,2

Notes:
[1] Maximum DC value may not be greater than 1.425V. The DC value is the linear average of VDD/VDDQ(t) over a very long period of time (e.g. 1sec.).
[2] If maximum limit is exceeded, input levels shall be governed by DDR3 specifications.
[3] Under these supply voltages, the device operates to this DDR3L specification.
[4] Once initialized for DDRD3L operation, DDR3 operation may only be used if the device is in reset while.
[5] VDD and VDDQ are changed for DDR3 operation shown as following timing waveform.

[Table 11] Recommended DC operating Conditions for DDR3L (1.5V)

Parameter	Symbol	min.	typ.	max.	Unit	Note
Supply voltage	VDD	1.425	1.5	1.575	V	1,2
Supply voltage for DQ	VDDQ	1.425	1.5	1.575	V	1,2

Notes:
[1] If minimum limit is exceeded, input levels shall be governed by DDR3L specifications.
[2] Under 1.5V operation, the DDR3L device operates to the DDR3 specification under the same speed timings as defined for this device.
[3] Once initialized for DDR3 operation, DDR3L operation may only be used if the device in reset while VDD and VDDQ are changed for DDR3L operation shown as next page.

3.4. 1.35V DDR3L AC and DC Logic Input Levels for Single-Ended Signals

[Refer to section 3 in JEDEC Standard No. JESD79- 3- 1A.01]

3.5. 1.35V DDR3L Electrical Characteristics and AC Timing

[Refer to section 4 in JEDEC Standard No. JESD79- 3- 1A.01]

3.6. Address / Command Setup, Hold and Derating

[Refer to section 4.1 in JEDEC Standard No. JESD79- 3- 1A.01]

3.7. Data Setup, Hold and Slew Rate Derating

[Refer to section 4.2 in JEDEC Standard No. JESD79- 3- 1A.01]

3.8. Overshoot and Undershoot Specifications

[Refer to section 9.6 in JEDEC Standard No. JESD79-3F]

3.9. 1.35V DDR3L Output Driver DC Electrical Characteristics

[Refer to section 6 in JEDEC Standard No. JESD79- 3- 1A.01]

3.10. 1.35V DDR3L On-Die Termination (ODT) Levels and I-V Characteristics

[Refer to section 7 in JEDEC Standard No. JESD79- 3- 1A.01]

3.11. 1.35V DDR3L Single Ended Output Slew Rate

[Refer to section 8 in JEDEC Standard No. JESD79- 3- 1A.01]

3.12. 1.35V Differential Output Slew Rate

[Refer to section 9 in JEDEC Standard No. JESD79- 3- 1A.01]

3.13. 1.35V DDR3L AC and DC Logic Input Levels for Differential Signals

[Refer to section 10 in JEDEC Standard No. JESD79- 3- 1A.01]

3.14. Differential Input Cross point voltage

[Refer to section 11 in JEDEC Standard No. JESD79- 3- 1A.01]

3.15. DQS Output Cross point voltage

[Refer to section 12 in JEDEC Standard No. JESD79- 3- 1A.01]

3.16. DC Characteristics

[Table 12] DDR3L 1.35V Operating IDD Characteristics

Speed			DDR3/3L -1600	DDR3/3L -1866	DDR3/3L -2133	Units	Notes
Parameter	Symbol	Width					
Operating current 0: One bank ACTIVATE-to- PRECHARGE	IDD0	X8	47	49	51	mA	1, 2
		X16	57	59	61	mA	1, 2
Operating current 1: One bank ACTIVATE-to-READ-to- PRECHARGE	IDD1	X8	61	64	67	mA	1, 2
		X16	81	84	87	mA	1, 2
Precharge power-down current: Slow exit	IDD2P0	All	8	8	8	mA	1, 2
Precharge power-down current: Fast exit	IDD2P1	All	14	16	18	mA	1, 2
Precharge quiet standby current	IDD2Q	All	24	26	28	mA	1, 2
Precharge standby current	IDD2N	All	24	26	28	mA	1, 2
Precharge standby ODT current	IDD2NT	X8	28	30	32	mA	1, 2
		X16	31	33	35	mA	1, 2
Active power-down current	IDD3P	All	26	28	30	mA	1, 2
Active standby current	IDD3N	X8	30	32	34	mA	1, 2
		X16	38	40	42	mA	1, 2
Burst read operating current	IDD4R	X8	95	105	115	mA	1, 2
		X16	155	165	175	mA	1, 2
Burst write operating current	IDD4W	X8	95	105	115	mA	1, 2
		X16	155	165	175	mA	1, 2
Burst refresh current	IDD5B	All	235	242	185	mA	1, 2
Room temperature self refresh	IDD6	All	12	12	12	mA	1, 2, 3
Extended temperature self refresh	IDD6ET	All	16	16	16	mA	2, 4
All banks interleaved read current	IDD7	X8	130	140	150	mA	1, 2
		X16	190	200	210	mA	1, 2
Reset current	IDD8	All	IDD2P + 2mA	IDD2P + 2mA	IDD2P + 2mA	mA	1, 2

Notes:
[1] TC = 85°C; SRT and ASR are disabled.
[2] Enabling ASR could increase IDDx by up to an additional 2mA.
[3] Restricted to TC (MAX) = 85°C.
[4] TC = 85°C; ASR and ODT are disabled; SRT is enabled.
[5] The IDD values must be derated (increased) on IT-option devices when operated outside of the range 0°C ≤ TC ≤ +85°C:
5a. When TC < 0°C: IDD2P0, IDD2P1 and IDD3P must be derated by 4%; IDD4R and IDD4W must be derated by 2%; and IDD6, IDD6ET and IDD7 must be derated by 7%.
5b. When TC > 85°C: IDD0, IDD1, IDD2N, IDD2NT, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, and IDD5B must be derated by 2%; IDD2Px must be derated by 30%.

3.17. Pin Capacitance(TC = 25°C, VDD, VDDQ = 1.35V)

[Table 13] Pin Capacitance

Capacitance Parameters	Symbol	DDR3L -1600		DDR3L -1866		DDR3L -2133		Unit	Notes
		Min	Max	Min	Max	Min	Max		
CK and CKB	CCK	0.8	1.4	0.8	1.3	0.8	1.3	pF	
ΔC: CK to CKB	CDCK	0.0	0.15	0.0	0.15	0.0	0.15	pF	
Single-end I/O: DQ, DM	CIO	1.4	2.2	1.4	2.1	1.4	2.1	pF	2
Differential I/O: DQS, DQSB	CIO	1.4	2.2	1.4	2.1	1.4	2.1	pF	3
ΔC: DQS to DQSB	CDDQS	0.0	0.15	0.0	0.15	0.0	0.15	pF	3
ΔC: DQ to DQS	CDIO	−0.5	0.3	−0.5	0.3	−0.5	0.3	pF	4
Inputs (CTRL, CMD, ADDR)	CI	0.75	1.2	0.75	1.2	0.75	1.2	pF	5
ΔC: CTRL to CK	CDI_CTRL	−0.4	0.2	−0.4	0.2	−0.4	0.2	pF	6
ΔC: CMD_ADDR to CK	CDI_CMD _ADDR	−0.4	0.4	−0.4	0.4	−0.4	0.4	pF	7
ZQ pin capacitance	CZQ	–	3.0	–	3.0	–	3.0	pF	
Reset pin capacitance	CRE	–	3.0	–	3.0	–	3.0	pF	

Notes:
[1] VDD = 1.35V (1.283–1.45V), VDDQ = VDD, VREF = VSS, f = 100 MHz, TC = 25°C. VOUT(DC) = 0.5× VDDQ, VOUT = 0.1V (peak-to-peak).
[2] DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
[3] Includes .CDDQS is for DQS vs. DQS# separately.
[4] CDIO = CIO(DQ) - 0.5 × (CIO(DQS) + CIO(DQS#)).
[5] Excludes CK, CKB; CTRL = ODT, CSB, and CKE; CMD = RASB, CASB, and WEB; ADDR= A[n:0], BA[2:0].
[6] CDI_CTRL = CI(CTRL) - 0.5 × (CCK(CK) + CCK(CKB)).
[7] CDI_CMD_ADDR = CI(CMD_ADDR) - 0.5 × (CCK(CK) + CCK(CKB)).

3.18. Standard Speed Bins

Refer to section 12.3 in JEDEC Standard No. JESD79-3F.

[Table 14] DDR3L-1600 Speed Bins

DDR3L-1600 Speed Bin			800MHz		Unit	Notes
CL-tRCD-tRP			11-11-11			
Parameter		Symbol	Min	Max		
Internal READ command to first data		tAA	13.75	–	ns	
ACTIVATE to internal READ or WRITE delay time		tRCD	13.75	–	ns	
PRECHARGE command period		tRP	13.75	–	ns	
ACTIVATE-to-ACTIVATE or REFRESH command period		tRC	48.75	–	ns	
ACTIVATE-to-PRECHARGE command period		tRAS	35	9 x tREFI	ns	2
CL = 5	CWL = 5	tCK (AVG)	3.0	3.3	ns	3
	CWL = 6, 7, 8	tCK (AVG)	Reserved		ns	4
CL = 6	CWL = 5	tCK (AVG)	2.5	3.3	ns	3
	CWL = 6	tCK (AVG)	Reserved		ns	4
	CWL = 7, 8	tCK (AVG)	Reserved		ns	4
CL = 7	CWL = 5	tCK (AVG)	Reserved		ns	4
	CWL = 6	tCK (AVG)	1.875	<2.5	ns	3
	CWL = 7	tCK (AVG)	Reserved		ns	4
	CWL = 8	tCK (AVG)	Reserved		ns	4
CL = 8	CWL = 5	tCK (AVG)	Reserved		ns	4
	CWL = 6	tCK (AVG)	1.875	<2.5	ns	3
	CWL = 7	tCK (AVG)	Reserved		ns	4
	CWL = 8	tCK (AVG)	Reserved		ns	4
CL = 9	CWL = 5, 6	tCK (AVG)	Reserved		ns	4
	CWL = 7	tCK (AVG)	1.5	<1.875	ns	3
	CWL = 8	tCK (AVG)	Reserved		ns	4
CL = 10	CWL = 5, 6	tCK (AVG)	Reserved		ns	4
	CWL = 7	tCK (AVG)	1.5	<1.875	ns	3
	CWL = 8	tCK (AVG)	Reserved		ns	4
CL = 11	CWL = 5, 6, 7	tCK (AVG)	Reserved		ns	4
	CWL = 8	tCK (AVG)	1.25	<1.5	ns	3
Supported CL settings			5, 6, 7, 8, 9, 10, 11		CK	
Supported CWL settings			5, 6, 7, 8		CK	

[Table 15] DDR3L-1866 Speed Bins

DDR3L-1866 Speed Bin			933MHz		Unit	Notes
CL-tRCD-tRP			13-13-13			
Parameter		Symbol	Min	Max		
Internal READ command to first data		tAA	13.91	20		
ACTIVATE to internal READ or WRITE delay time		tRCD	13.91	–	ns	
PRECHARGE command period		tRP	13.91	–	ns	
ACTIVATE-to-ACTIVATE or REFRESH command period		tRC	47.91	–	ns	
ACTIVATE-to-PRECHARGE command period		tRAS	34	9 x tREFI	ns	2
CL = 5	CWL = 5	tCK (AVG)	3.0	3.3	ns	3
	CWL = 6, 7, 8, 9	tCK (AVG)	Reserved		ns	4
CL = 6	CWL = 5	tCK (AVG)	2.5	3.3	ns	3
	CWL = 6, 7, 8, 9	tCK (AVG)	Reserved		ns	4
CL = 7	CWL = 5, 7, 8, 9	tCK (AVG)	Reserved		ns	4
	CWL = 6	tCK (AVG)	1.875	<2.5	ns	3
CL = 8	CWL = 5, 8, 9	tCK (AVG)	Reserved		ns	4
	CWL = 6	tCK (AVG)	1.875	<2.5	ns	3
	CWL = 7	tCK (AVG)	Reserved		ns	4
CL = 9	CWL = 5, 6, 8, 9	tCK (AVG)	Reserved		ns	4
	CWL = 7	tCK (AVG)	1.5	<1.875	ns	3
CL = 10	CWL = 5, 6, 9	tCK (AVG)	Reserved		ns	4
	CWL = 7	tCK (AVG)	1.5	<1.875	ns	3
	CWL = 8	tCK (AVG)	Reserved		ns	4
CL = 11	CWL = 5, 6, 7	tCK (AVG)	Reserved		ns	4
	CWL = 8	tCK (AVG)	1.25	<1.5	ns	3
	CWL = 9	tCK (AVG)	Reserved		ns	4
CL = 12	CWL = 5, 6, 7, 8	tCK (AVG)	Reserved		ns	4
	CWL = 9	tCK (AVG)	Reserved		ns	4
CL = 13	CWL = 5, 6, 7, 8	tCK (AVG)	Reserved		ns	4
	CWL = 9	tCK (AVG)	1.07	<1.25	ns	3
Supported CL settings			5, 6, 7, 8, 9, 10, 11, 13		CK	
Supported CWL settings			5, 6, 7, 8, 9		CK	

[Table 16] DDR3L-2133 Speed Bins

DDR3L-2133 Speed Bin			1066MHz		Unit	Notes
CL-tRCD-tRP			14-14-14			
Parameter		Symbol	Min	Max		
Internal READ command to first data		tAA	13.09	20		
ACTIVATE to internal READ or WRITE delay time		tRCD	13.09	–	ns	
PRECHARGE command period		tRP	13.09	–	ns	
ACTIVATE-to-ACTIVATE or REFRESH command period		tRC	46.09	–	ns	
ACTIVATE-to-PRECHARGE command period		tRAS	33	9 x tREFI	ns	2
CL = 5	CWL = 5	tCK (AVG)	3.0	3.3	ns	3
	CWL = 6, 7, 8, 9	tCK (AVG)	Reserved		ns	4
CL = 6	CWL = 5	tCK (AVG)	2.5	3.3	ns	3
	CWL = 6, 7, 8, 9	tCK (AVG)	Reserved		ns	4
CL = 7	CWL = 5, 7, 8, 9	tCK (AVG)	Reserved		ns	4
	CWL = 6	tCK (AVG)	1.875	<2.5	ns	3
CL = 8	CWL = 5, 8, 9	tCK (AVG)	Reserved		ns	4
	CWL = 6	tCK (AVG)	1.875	<2.5	ns	3
	CWL = 7	tCK (AVG)	Reserved		ns	4
CL = 9	CWL = 5, 6, 8, 9	tCK (AVG)	Reserved		ns	4
	CWL = 7	tCK (AVG)	1.5	<1.875	ns	3
CL = 10	CWL = 5, 6, 9	tCK (AVG)	Reserved		ns	4
	CWL = 7	tCK (AVG)	1.5	<1.875	ns	3
	CWL = 8	tCK (AVG)	Reserved		ns	4
CL = 11	CWL = 5, 6, 7	tCK (AVG)	Reserved		ns	4
	CWL = 8	tCK (AVG)	1.25	<1.5	ns	3
	CWL = 9	tCK (AVG)	Reserved		ns	4
CL = 12	CWL = 5, 6, 7, 8	tCK (AVG)	Reserved		ns	4
	CWL = 9	tCK (AVG)	Reserved		ns	4
CL = 13	CWL = 5, 6, 7, 8	tCK (AVG)	Reserved		ns	4
	CWL = 9	tCK (AVG)	1.07	<1.25	ns	3
CL = 14	CWL = 5, 6, 7, 8, 9	tCK (AVG)	Reserved	Reserved	ns	4
	CWL = 10	tCK (AVG)	0.938	<1.07	ns	3
Supported CL settings			5, 6, 7, 8, 9, 10, 11, 13, 14		CK	
Supported CWL settings			5, 6, 7, 8, 9		CK	

Notes:
[1] The 2133 speed grade is backward compatible with 1866, CL = 13, 1600, CL = 11, 1333, CL = 9 and 1066, CL = 7.
[2] tREFI depends on TOPER.
[3] The CL and CWL settings result in tCK requirements. When making a selection of tCK, both CL and CWL requirement settings need to be fulfilled.
[4] Reserved settings are not allowed.

3.19. AC Timing Characteristics

Refer to section 13 in JEDEC Standard No. JESD79-3F.

[Table 17] DDR3L-1600 AC Timing Characteristics 1

Parameter		Symbol	DDR3L-1600		Unit	Notes
			Min	Max		
Clock Timing						
Clock period average: DLL disable mode	TC ≤ 85°C	tCK (DLL_DIS)	8	7800	ns	9, 42
	TC = >85°C to 95°C		8	3900	ns	42
Clock period average: DLL enable mode		tCK (AVG)	–	–	ns	10, 11
High pulse width average		tCH (AVG)	0.47	0.53	CK	12
Low pulse width average		tCL (AVG)	0.47	0.53	CK	12
Clock period jitter	DLL locked	tJITper	–70	70	ps	13
	DLL locking	tJITper,lck	–60	60	ps	13
Clock absolute period		tCK (ABS)	MIN = tCK (AVG) MIN + tJITper MIN; MAX = tCK (AVG) MAX +tJITper		ps	
Clock absolute high pulse width		tCH (ABS)	0.43	–	tCK (AVG)	14
Clock absolute low pulse width		tCL (ABS)	0.43	–	tCK (AVG)	15
Cycle-to-cycle jitter	DLL locked	tJITcc	140		ps	16
	DLL locking	tJITcc,lck	120		ps	16
Cumulative error across	2 cycles	tERR2per	–103	103	ps	17
	3 cycles	tERR3per	–122	122	ps	17
	4 cycles	tERR4per	–136	136	ps	17
	5 cycles	tERR5per	–147	147	ps	17
	6 cycles	tERR6per	–155	155	ps	17
	7 cycles	tERR7per	–163	163	ps	17
	8 cycles	tERR8per	–169	169	ps	17
	9 cycles	tERR9per	–175	175	ps	17
	10 cycles	tERR10per	–180	180	ps	17
	11 cycles	tERR11per	–184	184	ps	17
	12 cycles	tERR12per	–188	188	ps	17
	n = 13, 14 . . . 49, 50 cycles	tERRnper	tERRnper MIN = (1 + 0.68ln[n]) × tJITper MIN tERRnper MAX = (1 + 0.68ln[n]) × tJITper MAX		ps	17

[Table 18] DDR3L-1600 **AC Timing Characteristics 2**

Parameter		Symbol	DDR3L-1600		Unit	Notes
			Min	Max		
DQ Input Timing						
Data setup time to DQS, DQS#	Base (specification)	tDS (AC160)	–	–	ps	18, 19, 44
	VREF @ 1 V/ns		–	–	ps	19, 20
Data setup time to DQS, DQS#	Base (specification)	tDS (AC135)	25	–	ps	18, 19, 44
	VREF @ 1 V/ns		160	–	ps	19, 20
Data hold time from DQS, DQS#	Base (specification)	tDH (DC90)	55	–	ps	18, 19
	VREF @ 1 V/ns		145	–	ps	19, 20
Minimum data pulse width		tDIPW	360	–	ps	41
DQ Output Timing						
DQS, DQS# to DQ skew, per access		tDQSQ	–	100	ps	
DQ output hold time from DQS, DQS#		tQH	0.38	–	tCK (AVG)	21
DQ Low-Z time from CK, CKB		tLZDQ	–450	225	ps	22, 23
DQ High-Z time from CK, CKB		tHZDQ	–	225	ps	22, 23
DQ Strobe Input Timing						
DQS, DQS# rising to CK, CKB rising		tDQSS	–0.27	0.27	CK	25
DQS, DQS# differential input low pulse width		tDQSL	0.45	0.55	CK	
DQS, DQS# differential input high pulse width		tDQSH	0.45	0.55	CK	
DQS, DQS# falling setup to CK, CKB rising		tDSS	0.18	–	CK	25
DQS, DQS# falling hold from CK, CKB rising		tDSH	0.18	–	CK	25
DQS, DQS# differential WRITE preamble		tWPRE	0.9	–	CK	
DQS, DQS# differential WRITE postamble		tWPST	0.3	–	CK	
DQ Strobe Output Timing						
DQS, DQS# rising to/from rising CK, CKB		tDQSCK	–225	225	ps	23
DQS, DQS# rising to/from rising CK, CKB when DLL is disabled		tDQSCK (DLL_DIS)	1	10	ns	26
DQS, DQS# differential output high time		tQSH	0.40	–	CK	21
DQS, DQS# differential output low time		tQSL	0.40	–	CK	21
DQS, DQS# Low-Z time (RL - 1)		tLZDQS	–450	225	ps	22, 23
DQS, DQS# High-Z time (RL + BL/2)		tHZDQS	–	225	ps	22, 23
DQS, DQS# differential READ preamble		tRPRE	0.9	Note 24	CK	23, 24
DQS, DQS# differential READ postamble		tRPST	0.3	Note 27	CK	23, 27

[Table 19] DDR3L-1600 **AC Timing Characteristics 3**

Parameter		Symbol	DDR3L-1600		Unit	Notes
			Min	Max		
Command and Address Timing						
DLL locking time		tDLLK	512	–	CK	28
CTRL, CMD, ADDR setup to CK,CKB	Base (specification)	tIS (AC160)	60	–	ps	29, 30, 44
	VREF @ 1 V/ns		220	–	ps	20, 30
CTRL, CMD, ADDR setup to CK,CKB	Base (specification)	tIS (AC135)	185	–	ps	29, 30, 44
	VREF @ 1 V/ns		320	–	ps	20, 30
CTRL, CMD, ADDR setup to CK,CKB	Base (specification)	tIH (DC90	130	–	ps	29, 30, 44
	VREF @ 1 V/ns		220	–	ps	20, 30
Minimum CTRL, CMD, ADDR pulse width		tIPW	560	–	ps	41
ACTIVATE to internal READ or WRITE delay		tRCD	See Speed Bin Tables for tRCD		ns	31
PRECHARGE command period		tRP	See Speed Bin Tables for tRP		ns	31
ACTIVATE-to-PRECHARGE command period		tRAS	See Speed Bin Tables for tRAS		ns	31, 32
ACTIVATE-to-ACTIVATE command period		tRC	See Speed Bin Tables for tRC		ns	31, 43
ACTIVATE-to-ACTIVATE minimum command period	X8 (1KB page size)	tRRD	MIN = greater of 4CK or 6ns		CK	31
	X16 (2KB page size)		MIN = greater of 4CK or 7.5ns		CK	31
Four ACTIVATE windows	X8 (1KB page size)	tFAW	30	–	ns	31
	X16 (2KB page size)		40		ns	31
Write recovery time		tWR	MIN = 15ns; MAX = N/A		ns	31, 32, 33,34
Delay from start of internal WRITE transaction to internal READ command		tWTR	MIN = greater of 4CK or 7.5ns; MAX = N/A		CK	31, 34
READ-to-PRECHARGE time		tRTP	MIN = greater of 4CK or 7.5ns; MAX = N/A		CK	31, 32
CASB-to-CASB command delay		tCCD	MIN = 4CK; MAX = N/A		CK	
Auto precharge write recovery + precharge time		tDAL	MIN = WR + tRP/tCK (AVG); MAX = N/A		CK	
MODE REGISTER SET command cycle time		tMRD	MIN = 4CK; MAX = N/A		CK	
MODE REGISTER SET command update delay		tMOD	MIN = greater of 12CK or 15ns; MAX = N/A		CK	
MULTIPURPOSE REGISTER READ burst end to mode register set for multipurpose register exit		tMPRR	MIN = 1CK; MAX = N/A		CK	
Calibration Timing						
ZQCL command: Long calibration time	POWER-UP and RESET operation	tZQinit	512	_	CK	
	Normal operation	tZQoper	256	_	CK	
ZQCS command: Short calibration time		tZQCS	64	_	CK	
Initialization and Reset Timing						
Exit reset from CKE HIGH to a valid command		tXPR	MIN = greater of 5CK or tRFC + 10ns; MAX = N/A		CK	
Begin power supply ramp to power supplies stable		tVDDPR	MIN = N/A; MAX = 200		ms	
RESET# LOW to power supplies stable		tRPS	MIN = 0; MAX = 200		ms	
RESET# LOW to I/O and RTT High-Z		tIOZ	MIN = N/A; MAX = 20		ns	35

[Table 20] DDR3L-1600 **AC Timing Characteristics 4**

Parameter		Symbol	DDR3L-1600		Unit	Notes
			Min	Max		
Refresh Timing						
REFRESH-to-ACTIVATE or REFRESH command period		tRFC – 1Gb	MIN = 110; MAX = 70,200		ns	
		tRFC – 2Gb	MIN = 160; MAX = 70,200		ns	
		tRFC – 4Gb	MIN = 260; MAX = 70,200		ns	
		tRFC – 8Gb	MIN = 350; MAX = 70,200		ns	
Maximum refresh period	TC ≤ 85°C	–	64 (1X)		ms	36
	TC > 85°C		32 (2X)		ms	36
Maximum average periodic refresh	TC ≤ 85°C	tREFI	7.8 (64ms/8192)		µs	36
	TC > 85°C		3.9 (32ms/8192)		µs	36
Self Refresh Timing						
Exit self refresh to commands not requiring a locked DLL		tXS	MIN = greater of 5CK or tRFC + 10ns; MAX = N/A		CK	
Exit self refresh to commands requiring a locked DLL		tXSDLL	MIN = tDLLK (MIN); MAX = N/A		CK	28
Minimum CKE low pulse width for self refresh entry to self refresh exit timing		tCKESR	MIN = tCKE (MIN) + CK; MAX = N/A		CK	
Valid clocks after self refresh entry or power-down entry		tCKSRE	MIN = greater of 5CK or 10ns; MAX = N/A		CK	
Valid clocks before self refresh exit, power-down exit, or reset exit		tCKSRX	MIN = greater of 5CK or 10ns; MAX = N/A		CK	
Power-Down Timing						
CKE MIN pulse width		tCKE (MIN)	Greater of 3CK or 5ns		CK	
Command pass disable delay		tCPDED	MIN = 1; MAX = N/A		CK	
Power-down entry to power-down exit timing		tPD	MIN = tCKE (MIN); MAX = 9 * tREFI		CK	
Begin power-down period prior to CKE registered HIGH		tANPD	WL - 1CK		CK	
Power-down entry period: ODT either synchronous or asynchronous		PDE	Greater of tANPD or tRFC - REFRESH command to CKE LOW time		CK	
Power-down exit period: ODT either synchronous or asynchronous		PDX	tANPD + tXPDLL		CK	
Power-Down Entry Minimum Timing						
ACTIVATE command to power-down entry		tACTPDEN	MIN = 1		CK	
PRECHARGE/PRECHARGE ALL command to power-down entry		tPRPDEN	MIN = 1		CK	
REFRESH command to power-down entry		tREFPDEN	MIN = 1		CK	37
MRS command to power-down entry		tMRSPDEN	MIN = tMOD (MIN)		CK	
READ/READ with auto precharge command to power-down entry		tRDPDEN	MIN = RL + 4 + 1		CK	
WRITE command to power-down entry	BL8 (OTF, MRS) BC4OTF	tWRPDEN	MIN = WL + 4 + tWR/tCK (AVG)		CK	
	BC4MRS	tWRPDEN	MIN = WL + 2 + tWR/tCK (AVG)		CK	
	BL8 (OTF, MRS) BC4OTF	tWRAPDEN	MIN = WL + 4 + WR + 1		CK	
	BC4MRS	tWRAPDEN	MIN = WL + 2 + WR + 1		CK	

[Table 21] DDR3L-1600 **AC Timing Characteristics 5**

Parameter	Symbol	DDR3L-1600		Unit	Notes
		Min	Max		
Power-Down Exit Timing					
DLL on, any valid command, or DLL off to commands not requiring locked DLL	tXP	MIN = greater of 3CK or 6ns; MAX = N/A		CK	
Precharge power-down with DLL off to commands requiring a locked DLL	tXPDLL	MIN = greater of 10CK or 24ns; MAX = N/A		CK	28
ODT Timing					
RTT synchronous turn-on delay	ODTLon	CWL + AL - 2CK		CK	38
RTT synchronous turn-off delay	ODTLoff	CWL + AL - 2CK		CK	40
RTT turn-on from ODTL on reference	tAON	–225	225	ps	23, 38
RTT turn-off from ODTL off reference	tAOF	0.3	0.7	CK	39, 40
Asynchronous RTT turn-on delay (power-down with DLL off)	tAONPD	MIN = 2; MAX = 8.5		ns	38
Asynchronous RTT turn-off delay (power-down with DLL off)	tAOFPD	MIN = 2; MAX = 8.5		ns	40
ODT HIGH time with WRITE command and BL8	ODTH8	MIN = 6; MAX = N/A		CK	
ODT HIGH time without WRITE command or with WRITE command and BC4	ODTH4	MIN = 4; MAX = N/A		CK	
Dynamic ODT Timing					
RTT,nom-to-RTT(WR) change skew	ODTLcnw	WL - 2CK		CK	
RTT(WR)-to-RTT,nom change skew - BC4	ODTLcwn4	4CK + ODTLoff		CK	
RTT(WR)-to-RTT,nom change skew - BL8	ODTLcwn8	6CK + ODTLoff		CK	
RTT dynamic change skew	tADC	0.3	0.7	CK	39
Write Leveling Timing					
First DQS, DQS# rising edge	tWLMRD	40	–	CK	
DQS, DQS# delay	tWLDQSEN	25	–	CK	
Write leveling setup from rising CK, CKB crossing to rising DQS, DQS# crossing	tWLS	165	–	ps	
Write leveling hold from rising DQS, DQS# crossing to rising CK, CKB crossing	tWLH	165	–	ps	
Write leveling output delay	tWLO	0	7.5	ns	
Write leveling output error	tWLOE	0	2	ns	

Notes:

[1] AC timing parameters are valid from specified T_C MIN to T_C MAX values.

[2] All voltages are referenced to V_{SS}.

[3] Output timings are only valid for R_{ON34} output buffer selection.

[4] The unit ^tCK (AVG) represents the actual ^tCK (AVG) of the input clock under operation. The unit CK represents one clock cycle of the input clock, counting the actual clock edges.

[5] AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 900mV in the test environment, but input timing is still referenced to V_{REF} (except ^tIS, ^tIH, ^tDS, and ^tDH use the AC/DC trip points and CK, CKB and DQS, DQS# use their crossing points). The minimum slew rate for the input signals used to test the device is 1 V/ns for single-ended inputs and 2 V/ns for differential inputs in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$.

[6] All timings that use time-based values (ns, µs, ms) should use ^tCK (AVG) to determine the correct number of clocks uses CK or ^tCK [AVG] interchangeably). In the case of noninteger results, all minimum limits are to be rounded up to the nearest whole integer, and all maximum limits are to be rounded down to the nearest whole integer.

[7] Strobe or DQS_{diff} refers to the DQS and DQS# differential crossing point when DQS is the rising edge. Clock or CK refers to the CK and CKB differential crossing point when CK is the rising edge.

[8] This output load is used for all AC timing (except ODT reference timing) and slew rates. The actual test load may be different. The output signal voltage reference point is $V_{DDQ}/2$ for single-ended signals and the crossing point for differential signals.

[9] When operating in DLL disable mode, PTC does not warrant compliance with normal mode timings or functionality.

[10] The clock's ^tCK (AVG) is the average clock over any 200 consecutive clocks and ^tCK(AVG) MIN is the smallest clock rate allowed, with the exception of a deviation due to clock jitter. Input clock jitter is allowed provided it does not exceed values specified and must be of a random Gaussian distribution in nature.

[11] Spread spectrum is not included in the jitter specification values. However, the input clock can accommodate spread-spectrum at a sweep rate in the range of 20–60 kHz with an additional 1% of ^{t}CK (AVG) as a long-term jitter component; however, the spread spectrum may not use a clock rate below ^{t}CK (AVG) MIN.

[12] The clock's ^{t}CH (AVG) and ^{t}CL (AVG) are the average half clock period over any 200 consecutive clocks and is the smallest clock half period allowed, with the exception of a deviation due to clock jitter. Input clock jitter is allowed provided it does not exceed values specified and must be of a random Gaussian distribution in nature.

[13] The period jitter (^{t}JITper) is the maximum deviation in the clock period from the average or nominal clock. It is allowed in either the positive or negative direction.

[14] ^{t}CH (ABS) is the absolute instantaneous clock high pulse width as measured from one rising edge to the following falling edge.

[15] ^{t}CL (ABS) is the absolute instantaneous clock low pulse width as measured from one falling edge to the following rising edge.

[16] The cycle-to-cycle jitter ^{t}JITcc is the amount the clock period can deviate from one cycle to the next. It is important to keep cycle-to-cycle jitter at a minimum during the DLL locking time.

[17] The cumulative jitter error ^{t}ERRnper, where *n* is the number of clocks between 2 and 50, is the amount of clock time allowed to accumulate consecutively away from the average clock over *n* number of clock cycles.

[18] ^{t}DS (base) and ^{t}DH (base) values are for a single-ended 1 V/ns slew rate DQs and 2 V/ns slew rate differential DQS, DQS#; when DQ single-ended slew rate is 2V/ns, the DQS differential slew rate is 4V/ns.

[19] These parameters are measured from a data signal (DM, DQ0, DQ1, and so forth) transition edge to its respective data strobe signal (DQS, DQS#) crossing.

[20] The setup and hold times are listed converting the base specification values (to which derating tables apply) to V_{REF} when the slew rate is 1 V/ns. These values, with a slew rate of 1 V/ns, are for reference only.

[21] When the device is operated with input clock jitter, this parameter needs to be derated by the actual ^{t}JITper (larger of ^{t}JITper (MIN) or ^{t}JITper (MAX) of the input clock (output deratings are relative to the SDRAM input clock).

[22] Single-ended signal parameter.

[23] The DRAM output timing is aligned to the nominal or average clock. Most output parameters must be derated by the actual jitter error when input clock jitter is present, even when within specification. This results in each parameter becoming larger. The following parameters are required to be derated by subtracting ^{t}ERR10per (MAX): ^{t}DQSCK (MIN), ^{t}LZDQS (MIN), ^{t}LZDQ (MIN), and ^{t}AON (MIN). The following parameters are required to be derated by subtracting ^{t}ERR10per (MIN): ^{t}DQSCK (MAX), ^{t}HZ (MAX), ^{t}LZDQS (MAX), ^{t}LZDQ MAX, and ^{t}AON (MAX). The parameter ^{t}RPRE (MIN) is derated by subtracting ^{t}JITper (MAX), while ^{t}RPRE (MAX) is derated by subtracting ^{t}JITper (MIN).

[24] The maximum preamble is bound by ^{t}LZDQS (MAX).

[25] These parameters are measured from a data strobe signal (DQS, DQS#) crossing to its respective clock signal (CK, CKB) crossing. The specification values are not affected by the amount of clock jitter applied, as these are relative to the clock signal crossing. These parameters should be met whether clock jitter is present.

[26] The ^{t}DQSCK (DLL_DIS) parameter begins CL + AL - 1 cycles after the READ command.

[27] The maximum postamble is bound by ^{t}HZDQS(MAX).

[28] Commands requiring a locked DLL are: READ (and RDAP) and synchronous ODT commands. In addition, after any change of latency ^{t}XPDLL, timing must be met.

[29] ^{t}IS (base) and ^{t}IH (base) values are for a single-ended 1 V/ns control/command/address slew rate and 2 V/ns CK, CKB differential slew rate.

[30] These parameters are measured from a command/address signal transition edge to its respective clock (CK, CKB) signal crossing. The specification values are not affected by the amount of clock jitter applied as the setup and hold times are relative to the clock signal crossing that latches the command/address. These parameters should be met whether clock jitter is present.

[31] For these parameters, the DDR3L SDRAM device supports ^{t}*n*PARAM (*n*CK) = RU(^{t}PARAM [ns]/^{t}CK[AVG] [ns]), assuming all input clock jitter specifications are satisfied. For example, the device will support ^{t}*n*RP (*n*CK) = RU(^{t}RP/^{t}CK[AVG]) if all input clock jitter specifications are met. This means that for DDR3-800 6-6-6, of which ^{t}RP = 5ns, the device will support ^{t}*n*RP = RU(^{t}RP/^{t}CK[AVG]) = 6 as long as the input clock jitter specifications are met. That is, the PRECHARGE command at T0 and the ACTIVATE command at T0 + 6 are valid even if six clocks are less than 15ns due to input clock jitter.

[32] During READs and WRITEs with auto precharge, the DDR3 SDRAM will hold off the internal PRECHARGE command until ^{t}RAS (MIN) has been satisfied.

[33] When operating in DLL disable mode, the greater of 4CK or 15ns is satisfied for ^{t}WR.

[34] The start of the write recovery time is defined as follows:

a) For BL8 (fixed by MRS or OTF): Rising clock edge four clock cycles after WL

b) For BC4 (OTF): Rising clock edge four clock cycles after WL

c) For BC4 (fixed by MRS): Rising clock edge two clock cycles after WL

[35] RESET# should be LOW as soon as power starts to ramp to ensure the outputs are in High-Z. Until RESET# is LOW, the outputs are at risk of driving and could result in excessive current, depending on bus activity.

[36] The refresh period is 64ms when T_C is less than or equal to 85°C. This equates to an average refresh rate of 7.8125µs. However, nine REFRESH commands should be asserted at least once every 70.3µs. When T_C is greater than 85°C, the refresh period is 32ms.

[37] Although CKE is allowed to be registered LOW after a REFRESH command when ^{t}REFPDEN (MIN) is satisfied, there are cases where additional time such as ^{t}XPDLL (MIN) is required.

[38] ODT turn-on time MIN is when the device leaves High-Z and ODT resistance begins to turn on. ODT turn-on time maximum is when the ODT resistance is fully on. The ODT reference load is shown. This output load is used for ODT timings. Designs that were created prior to JEDEC tightening the maxi- mum limit from 9ns to 8.5ns will be allowed to have a 9ns maximum.

[39] Half-clock output parameters must be derated by the actual ^{t}ERR10per and ^{t}JITdty when input clock jitter is present. This results in each parameter becoming larger. The parameters ^{t}ADC (MIN) and ^{t}AOF (MIN) are each required to be derated by subtracting both ^{t}ERR10per (MAX) and ^{t}JITdty (MAX). The parameters ^{t}ADC (MAX) and ^{t}AOF (MAX) are required to be derated by subtracting both ^{t}ERR10per (MAX) and ^{t}JITdty(MAX).

[40] ODT turn-off time minimum is when the device starts to turn off ODT resistance. ODT turn- off time maximum is when the DRAM buffer is in High-Z. The ODT reference load is shown. This output load is used for ODT timings.

[41] Pulse width of a input signal is defined as the width between the first crossing of $V_{REF(DC)}$ and the consecutive crossing of $V_{REF(DC)}$.

[42] Should the clock rate be larger than ^{t}RFC (MIN), an AUTO REFRESH command should have at least one NOP command between it and another AUTO REFRESH command. Additionally, if the clock rate is slower than 40ns (25 MHz), all REFRESH commands should be followed by a PRECHARGE ALL command.

[43] DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to a particular row address may result in a reduction of REFRESH characteristics or product lifetime.

[44] When two $V_{IH(AC)}$ values (and two corresponding $V_{IL(AC)}$ values) are listed for a specific speed bin, the user may choose either value for the input AC level. Whichever value is used, the associated setup time for that AC level must also be used. Additionally, one $V_{IH(AC)}$ value may be used for address/command inputs and the other $V_{IH(AC)}$ value may be used for data inputs.

For example, for DDR3-800, two input AC levels are defined: $V_{IH(AC175),min}$ and $V_{IH(AC150),min}$ (corresponding $V_{IL(AC175),min}$ and $V_{IL(AC150),min}$). For DDR3-800, the address/ command inputs must use either $V_{IH(AC175),min}$ with ^{t}IS(AC175) of 200ps or $V_{IH(AC150),min}$ with ^{t}IS(AC150) of 350ps; independently, the data inputs must use either $V_{IH(AC175),min}$ with ^{t}DS(AC175) of 75ps or $V_{IH(AC150),min}$ with ^{t}DS(AC150) of 125ps.

[Table 22] DDR3L-1866/2133 AC Timing Characteristics 1

Parameter		Symbol	DDR3L-1866		DDR3L-2133		Unit	Notes
			Min	Max	Min	Max		
Clock Timing								
Clock period average: DLL disable mode	TC = 0°C to 85°C	tCK (DLL_DIS)	8	7800	8	7800	ns	9, 42
	TC = >85°C to 95°C		8	3900	8	3900	ns	42
Clock period average: DLL enable mode		tCK (AVG)	See Speed Bin Tables for tCK range allowed ns					10, 11
High pulse width average		tCH (AVG)	0.47	0.53	0.47	0.53	CK	12
Low pulse width average		tCL (AVG)	0.47	0.53	0.47	0.53	CK	12
Clock period jitter	DLL locked	tJITper	–60	60	–50	50	ps	13
	DLL locking	tJITper,lck	–50	50	–40	40	ps	13
Clock absolute period		tCK (ABS)	MIN = tCK (AVG) MIN + tJITper MIN; MAX = tCK (AVG) MAX +tJITper MAX				ps	
Clock absolute high pulse width		tCH (ABS)	0.43	–	0.43	–	tCK (AVG)	14
Clock absolute low pulse width		tCL (ABS)	0.43	–	0.43	–	tCK (AVG)	15
Cycle-to-cycle jitter	DLL locked	tJITcc	120		120		ps	16
	DLL locking	tJITcc,lck	100		100		ps	16
Cumulative error across	2 cycles	tERR2per	–88	88	–74	74	ps	17
	3 cycles	tERR3per	–105	105	–87	87	ps	17
	4 cycles	tERR4per	–117	117	–97	97	ps	17
	5 cycles	tERR5per	–126	126	–105	105	ps	17
	6 cycles	tERR6per	–133	133	–111	111	ps	17
	7 cycles	tERR7per	–139	139	–116	116	ps	17
	8 cycles	tERR8per	–145	145	–121	121	ps	17
	9 cycles	tERR9per	–150	150	–125	125	ps	17
	10 cycles	tERR10per	–154	154	–128	128	ps	17
	11 cycles	tERR11per	–158	158	–132	132	ps	17
	12 cycles	tERR12per	–161	161	–134	134	ps	17
	n = 13, 14 . . . 49, 50 cycles	tERRnper	tERRnper MIN = (1 + 0.68ln[n]) × tJITper MIN tERRnper MAX = (1 + 0.68ln[n]) × tJITper MAX				ps	17

[Table 23] DDR3L-1866/2133 AC Timing Characteristics 2

Parameter		Symbol	DDR3L-1866		DDR3L-2133		Unit	Notes
			Min	Max	Min	Max		
DQ Input Timing								
Data setup time to DQS, DQS#	Base (specification) @ 2 V/ns	tDS (AC130)	70	–	55	–	ps	18, 19
	VREF @ 2 V/ns		135	–	120.5	–	ps	19, 20
Data hold time from DQS, DQS#	Base (specification) @ 2 V/ns	tDH (DC90)	75	–	60	–	ps	18, 19
	VREF @ 2 V/ns		110	–	105	–	ps	19, 20
Minimum data pulse width		tDIPW	320	–	280	–	ps	41
DQ Output Timing								
DQS, DQS# to DQ skew, per access		tDQSQ	–	85	–	75	ps	
DQ output hold time from DQS, DQS#		tQH	0.38	–	0.38	–	tCK (AVG)	21
DQ Low-Z time from CK, CK#		tLZDQ	–390	195	–360	180	ps	22, 23
DQ High-Z time from CK, CK#		tHZDQ	–	195	–	180	ps	22, 23
DQ Strobe Input Timing								
DQS, DQS# rising to CK, CK# rising		tDQSS	–0.27	0.27	–0.27	0.27	CK	25
DQS, DQS# differential input low pulse width		tDQSL	0.45	0.55	0.45	0.55	CK	
DQS, DQS# differential input high pulse width		tDQSH	0.45	0.55	0.45	0.55	CK	
DQS, DQS# falling setup to CK, CK# rising		tDSS	0.18	–	0.18	–	CK	25
DQS, DQS# falling hold from CK, CK# rising		tDSH	0.18	–	0.18	–	CK	25
DQS, DQS# differential WRITE preamble		tWPRE	0.9	–	0.9	–	CK	
DQS, DQS# differential WRITE postamble		tWPST	0.3	–	0.3	–	CK	
DQ Strobe Output Timing								
DQS, DQS# rising to/from rising CK, CK#		tDQSCK	–195	195	–180	180	ps	23
DQS, DQS# rising to/from rising CK, CK# when DLL is disabled		tDQSCK (DLL_DIS)	1	10	1	10	ns	26
DQS, DQS# differential output high time		tQSH	0.40	–	0.40	–	CK	21
DQS, DQS# differential output low time		tQSL	0.40	–	0.40	–	CK	21
DQS, DQS# Low-Z time (RL - 1)		tLZDQS	–390	195	–360	180	ps	22, 23
DQS, DQS# High-Z time (RL + BL/2)		tHZDQS	–	195	–	180	ps	22, 23
DQS, DQS# differential READ preamble		tRPRE	0.9	Note 24	0.9	Note 24	CK	23, 24
DQS, DQS# differential READ postamble		tRPST	0.3	Note 27	0.3	Note 27	CK	23, 27

[Table 24] DDR3L-1866/2133 AC Timing Characteristics 3

Parameter		Symbol	DDR3L-1866		DDR3L-2133		Unit	Notes
			Min	Max	Min	Max		
Command and Address Timing								
DLL locking time		tDLLK	512	–	512	–	CK	28
CTRL, CMD, ADDR setup to CK,CK#	Base (specification)	tIS (AC135)	65	–	60	–	ps	29, 30, 44
	VREF @ 1 V/ns		200	–	195	–	ps	20, 30
CTRL, CMD, ADDR setup to CK,CK#	Base (specification)	tIS (AC125)	150	–	135	–	ps	29, 30, 44
	VREF @ 1 V/ns		275	–	260	–	ps	20, 30
CTRL, CMD, ADDR hold from CK,CK#	Base (specification)	tIH (DC90)	110	–	95	–	ps	29, 30
	VREF @ 1 V/ns		200	–	195	–	ps	20, 30
Minimum CTRL, CMD, ADDR pulse width		tIPW	535	–	470	–	ps	41
ACTIVATE to internal READ or WRITE delay		tRCD	See Speed Bin Tables for tRCD				ns	31
PRECHARGE command period		tRP	See Speed Bin Tables for tRP				ns	31
ACTIVATE-to-PRECHARGE command period		tRAS	See Speed Bin Tables for tRAS				ns	31, 32
ACTIVATE-to-ACTIVATE command period		tRC	See Speed Bin Tables for tRC				ns	31, 43
ACTIVATE-to-ACTIVATE minimum command period	1KB page size	tRRD	MIN = greater of 4CK or 5ns				CK	31
	2KB page size		MIN = greater of 4CK or 6ns				CK	31
Four ACTIVATE windows	1KB page size	tFAW	27	–	25	–	ns	31
	2KB page size		35	–	35	–	ns	31
Write recovery time		tWR	MIN = 15ns; MAX = N/A				ns	31, 32, 33
Delay from start of internal WRITE transaction to internal READ command		tWTR	MIN = greater of 4CK or 7.5ns; MAX = N/A				CK	31, 34
READ-to-PRECHARGE time		tRTP	MIN = greater of 4CK or 7.5ns; MAX = N/A				CK	31, 32
CAS#-to-CAS# command delay		tCCD	MIN = 4CK; MAX = N/A				CK	
Auto precharge write recovery + precharge time		tDAL	MIN = WR + tRP/tCK (AVG); MAX = N/A				CK	
MODE REGISTER SET command cycle time		tMRD	MIN = 4CK; MAX = N/A				CK	
MODE REGISTER SET command update delay		tMOD	MIN = greater of 12CK or 15ns; MAX = N/A				CK	
MULTIPURPOSE REGISTER READ burst end to mode register set for multipurpose register exit		tMPRR	MIN = 1CK; MAX = N/A				CK	
Calibration Timing								
ZQCL command: Long calibration time	POWER-UP and RESET operation	tZQinit	MIN = N/A MAX = MAX(512nCK, 640ns)				CK	
	Normal operation	tZQoper	MIN = N/A MAX = max(256nCK, 320ns)				CK	
ZQCS command: Short calibration time			MIN = N/A MAX = max(64nCK, 80ns) tZQCS				CK	
Initialization and Reset Timing								
Exit reset from CKE HIGH to a valid command		tXPR	MIN = greater of 5CK or tRFC + 10ns; MAX = N/A				CK	
Begin power supply ramp to power supplies stable		tVDDPR	MIN = N/A; MAX = 200				ms	
RESET# LOW to power supplies stable		tRPS	MIN = 0; MAX = 200				ms	
RESET# LOW to I/O and RTT High-Z		tIOZ	MIN = N/A; MAX = 20				ns	35

[Table 25] DDR3L-1866/2133 AC Timing Characteristics 4

Parameter		Symbol	DDR3L-1866		DDR3L-2133		Unit	Notes
			Min	Max	Min	Max		
Refresh Timing								
REFRESH-to-ACTIVATE or REFRESH command period		tRFC – 1Gb	MIN = 110; MAX = 70,200				ns	
		tRFC – 2Gb	MIN = 160; MAX = 70,200				ns	
		tRFC – 4Gb	MIN = 260; MAX = 70,200				ns	
		tRFC – 8Gb	MIN = 350; MAX = 70,200				ns	
Maximum refresh period	TC ≤ 85°C	–	64 (1X)				ms	36
	TC > 85°C		32 (2X)				ms	36
Maximum average periodic refresh	TC ≤ 85°C	tREFI	7.8 (64ms/8192)				µs	36
	TC > 85°C		3.9 (32ms/8192)				µs	36
Self Refresh Timing								
Exit self refresh to commands not requiring a locked DLL		tXS	MIN = greater of 5CK or tRFC + 10ns; MAX = N/A				CK	
Exit self refresh to commands requiring a locked DLL		tXSDLL	MIN = tDLLK (MIN); MAX = N/A				CK	28
Minimum CKE low pulse width for self refresh entry to self refresh exit timing		tCKESR	MIN = tCKE (MIN) + CK; MAX = N/A				CK	
Valid clocks after self refresh entry or power-down entry		tCKSRE	MIN = greater of 5CK or 10ns; MAX = N/A				CK	
Valid clocks before self refresh exit, power-down exit, or reset exit		tCKSRX	MIN = greater of 5CK or 10ns; MAX = N/A				CK	
Power-Down Timing								
CKE MIN pulse width		tCKE (MIN)	Greater of 3CK or 5ns				CK	
Command pass disable delay		tCPDED	MIN = 2; MAX = N/A				CK	
Power-down entry to power-down exit timing		tPD	MIN = tCKE (MIN); MAX = 9 * tREFI				CK	
Begin power-down period prior to CKE registered HIGH		tANPD	WL - 1CK				CK	
Power-down entry period: ODT either synchronous or asynchronous		PDE	Greater of tANPD or tRFC - REFRESH command to CKE LOW time				CK	
Power-down exit period: ODT either synchronous or asynchronous		PDX	tANPD + tXPDLL				CK	
Power-Down Entry Minimum Timing								
ACTIVATE command to power-down entry		tACTPDEN	MIN = 2				CK	
PRECHARGE/PRECHARGE ALL command to power-down entry		tPRPDEN	MIN = 2				CK	
REFRESH command to power-down entry		tREFPDEN	MIN = 2				CK	37
MRS command to power-down entry		tMRSPDEN	MIN = tMOD (MIN)				CK	
READ/READ with auto precharge command to power-down entry		tRDPDEN	MIN = RL + 4 + 1				CK	
WRITE command to power-down entry	BL8 (OTF, MRS) BC4OTF	tWRPDEN	MIN = WL + 4 + tWR/tCK (AVG)				CK	
	BC4MRS	tWRPDEN	MIN = WL + 2 + tWR/tCK (AVG)				CK	
WRITE with auto pre-charge command to power-down entry	BL8 (OTF, MRS) BC4OTF	tWRAPDEN	MIN = WL + 4 + WR + 1				CK	
	BC4MRS	tWRAPDEN	MIN = WL + 2 + WR + 1				CK	

[Table 26] DDR3L-1866/2133 AC Timing Characteristics 5

Parameter	Symbol	DDR3L-1866		DDR3L-2133		Unit	Notes
		Min	Max	Min	Max		
Power-Down Exit Timing							
DLL on, any valid command, or DLL off to commands not requiring locked DLL	tXP	MIN = greater of 3CK or 6ns; MAX = N/A				CK	
Precharge power-down with DLL off to commands requiring a locked DLL	tXPDLL	MIN = greater of 10CK or 24ns; MAX = N/A				CK	28
ODT Timing							
RTT synchronous turn-on delay	ODTL on	CWL + AL - 2CK				CK	38
RTT synchronous turn-off delay	ODTL off	CWL + AL - 2CK				CK	40
RTT turn-on from ODTL on reference	tAON	–195	195	–180	180	ps	23, 38
RTT turn-off from ODTL off reference	tAOF	0.3	0.7	0.3	0.7	CK	39, 40
Asynchronous RTT turn-on delay (power-down with DLL off)	tAONPD	MIN = 2; MAX = 8.5				ns	38
Asynchronous RTT turn-off delay (power-down with DLL off)	tAOFPD	MIN = 2; MAX = 8.5				ns	40
ODT HIGH time with WRITE command and BL8	ODTH8	MIN = 6; MAX = N/A				CK	
ODT HIGH time without WRITE command or with WRITE command and BC4	ODTH4	MIN = 4; MAX = N/A				CK	
Dynamic ODT Timing							
RTT,nom-to-RTT(WR) change skew	ODTLcnw	WL - 2CK				CK	
RTT(WR)-to-RTT,nom change skew - BC4	ODTLcwn4	4CK + ODTLoff				CK	
RTT(WR)-to-RTT,nom change skew - BL8	ODTLcwn8	6CK + ODTLoff				CK	
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	CK	39
Write Leveling Timing							
First DQS, DQS# rising edge	tWLMRD	40	–	40	–	CK	
DQS, DQS# delay	tWLDQSEN	25	–	25	–	CK	
Write leveling setup from rising CK, CK# crossing to rising DQS, DQS# crossing	tWLS	140	–	125	–	ps	
Write leveling hold from rising DQS, DQS# crossing to rising CK, CK# crossing	tWLH	140	–	125	–	ps	
Write leveling output delay	tWLO	0	7.5	0	7	ns	
Write leveling output error	tWLOE	0	2	0	2	ns	

Notes:

[1] AC timing parameters are valid from specified T_C MIN to T_C MAX values.

[2] All voltages are referenced to V_{SS}.

[3] Output timings are only valid for R_{ON34} output buffer selection.

[4] The unit ^tCK (AVG) represents the actual ^tCK (AVG) of the input clock under operation. The unit CK represents one clock cycle of the input clock, counting the actual clock edges.

[5] AC timing and IDD tests may use a VIL-to-VIH swing of up to 900mV in the test environment, but input timing is still referenced to V_{REF} (except ^tIS, ^tIH, ^tDS, and ^tDH use the AC/DC trip points and CK, CKB and DQS, DQS# use their crossing points). The minimum slew rate for the input signals used to test the device is 1 V/ns for single-ended inputs (DQs are at 2V/ns for DDR3-1866 and DDR3-2133) and 2 V/ns for differential inputs in the range between VIL(AC) and VIH(AC).

[6] All timings that use time-based values (ns, µs, ms) should use ^tCK (AVG) to determine the correct number of clocks uses CK or ^tCK [AVG] interchangeably). In the case of noninteger results, all minimum limits are to be rounded up to the nearest whole integer, and all maximum limits are to be rounded down to the nearest whole integer.

[7] Strobe or DQS diff refers to the DQS and DQS# differential crossing point when DQS is the rising edge. Clock or CK refers to the CK and CKB differential crossing point when CK is the rising edge.

[8] This output load is used for all AC timing (except ODT reference timing) and slew rates. The actual test load may be different. The output signal voltage reference point is $V_{DDQ}/2$ for single-ended signal sand the crossing point for differential signals.

[9] When operating in DLL disable mode, PTC does not warrant compliance with normal mode timings or functionality.

[10] The clock's ^{t}CK (AVG) is the average clock over any 200 consecutive clocks and ^{t}CK(AVG) MIN is the smallest clock rate allowed, with the exception of a deviation due to clock jitter. Input clock jitter is allowed provided it does not exceed values specified and must be of a random Gaussian distribution in nature.

[11] Spread spectrum is not included in the jitter specification values. However, the input clock can accommodate spread-spectrum at a sweep rate in the range of 20–60 kHz with an additional 1% of ^{t}CK (AVG) as a long-term jitter component; however, the spread spectrum may not use a clock rate below ^{t}CK (AVG) MIN.

[12] The clock's ^{t}CH (AVG) and ^{t}CL (AVG) are the average half clock period over any 200 consecutive clocks and is the smallest clock half period allowed, with the exception of a deviation due to clock jitter. Input clock jitter is allowed provided it does not exceed values specified and must be of a random Gaussian distribution in nature.

[13] The period jitter (^{t}JITper) is the maximum deviation in the clock period from the average or nominal clock. It is allowed in either the positive or negative direction.

[14] ^{t}CH (ABS) is the absolute instantaneous clock high pulse width as measured from one rising edge to the following falling edge.

[15] ^{t}CL (ABS) is the absolute instantaneous clock low pulse width as measured from one falling edge to the following rising edge.

[16] The cycle-to-cycle jitter ^{t}JITcc is the amount the clock period can deviate from one cycle to the next. It is important to keep cycle-to-cycle jitter at a minimum during the DLL locking time.

[17] The cumulative jitter error ^{t}ERRnper, where *n* is the number of clocks between 2 and 50, is the amount of clock time allowed to accumulate consecutively away from the average clock over *n* number of clock cycles.

[18] ^{t}DS (base) and ^{t}DH (base) values are for a single-ended 1 V/ns slew rate DQs (DQs are at 2V/ns for DDR3-1866 and DDR3-2133) and 2 V/ns slew rate differential DQS, DQS#; when DQ single-ended slew rate is 2V/ns, the DQS differential slew rate is 4V/ns.

[19] These parameters are measured from a data signal (DM, DQ0, DQ1, and so forth) transition edge to its respective data strobe signal (DQS, DQS#) crossing.

[20] The setup and hold times are listed converting the base specification values (to which derating tables apply) to VREF when the slew rate is 1 V/ns (DQs are at 2V/ns for
   i. DDR3-1866 and DDR3-2133). These values, with a slew rate of 1 V/ns
   ii. (DQs are at 2V/ns for DDR3-1866 and DDR3-2133), are for reference only.

[21] When the device is operated with input clock jitter, this parameter needs to be derated by the actual ^{t}JITper (larger of ^{t}JITper (MIN) or ^{t}JITper (MAX) of the input clock (output deratings are relative to the SDRAM input clock).

[22] Single-ended signal parameter.

[23] The DRAM output timing is aligned to the nominal or average clock. Most output parameters must be derated by the actual jitter error when input clock jitter is present, even when within specification. This results in each parameter becoming larger. The following parameters are required to be derated by subtracting ^{t}ERR10per (MAX): ^{t}DQSCK (MIN), ^{t}LZDQS (MIN), ^{t}LZDQ (MIN), and ^{t}AON (MIN). The following parameters are required to be derated by subtracting ^{t}ERR10per (MIN): ^{t}DQSCK (MAX), ^{t}HZ (MAX), ^{t}LZDQS (MAX), ^{t}LZDQ (MAX), and ^{t}AON (MAX). The parameter ^{t}RPRE (MIN) is derated by subtracting ^{t}JITper (MAX), while ^{t}RPRE (MAX) is derated by subtracting ^{t}JITper (MIN).

[24] The maximum preamble is bound by ^{t}LZDQS (MAX).

[25] These parameters are measured from a data strobe signal (DQS, DQS#) crossing to its respective clock signal (CK, CKB) crossing. The specification values are not affected by the amount of clock jitter applied, as these are relative to the clock signal crossing. These parameters should be met whether clock jitter is present.

[26] The ^{t}DQSCK (DLL_DIS) parameter begins CL + AL - 1 cycles after the READ command.

[27] The maximum postamble is bound by ^{t}HZDQS(MAX).

[28] Commands requiring a locked DLL are: READ (and RDAP) and synchronous ODT commands. In addition, after any change of latency tXPDLL, timing must be met.

[29] tIS (base) and tIH (base) values are for a single-ended 1 V/ns control/command/address slew rate and 2 V/ns CK, CKB differential slew rate.

[30] These parameters are measured from a command/address signal transition edge to its respective clock (CK, CKB) signal crossing. The specification values are not affected by the amount of clock jitter applied as the setup and hold times are relative to the clock signal crossing that latches the command/address. These parameters should be met whether clock jitter is present.

[31] For these parameters, the DDR3L SDRAM device supports tnPARAM (nCK) = RU(tPARAM [ns]/tCK[AVG] [ns]), assuming all input clock jitter specifications are satisfied. For example, the device will support ^{t}*n*RP (*n*CK) = RU(^{t}RP/^{t}CK[AVG]) if all input clock jitter specifications are met. This means that for DDR3-800 6-6-6, of which ^{t}RP = 5ns, the device will support ^{t}*n*RP = RU(^{t}RP/^{t}CK[AVG]) = 6 as long as the input clock jitter specifications are met. That is, the PRECHARGE command at T0 and the ACTIVATE command at T0 + 6 are valid even if six clocks are less than 15ns due to input clock jitter.

[32] During READs and WRITEs with auto precharge, the DDR3 SDRAM will hold off the internal PRECHARGE command until ^{t}RAS (MIN) has been satisfied.

[33] When operating in DLL disable mode, the greater of 5CK or 15ns is satisfied for ^{t}WR.

[34] The start of the write recovery time is defined as follows:

   a) For BL8 (fixed by MRS or OTF): Rising clock edge four clock cycles after WL
   b) For BC4 (OTF): Rising clock edge four clock cycles after WL
   c) For BC4 (fixed by MRS): Rising clock edge two clock cycles after WL

[35] RESET# should be LOW as soon as power starts to ramp to ensure the outputs are in High-Z. Until RESET# is LOW, the outputs are at risk of driving and could result in excessive current, depending on bus activity.

[36] The refresh period is 64ms when T_C is less than or equal to 85°C. This equates to an average refresh rate of 7.8125µs. However, nine REFRESH commands should be asserted at least once every 70.3µs. When T_C is greater than 85°C, the refresh period is 32ms.

[37] Although CKE is allowed to be registered LOW after a REFRESH command when ^{t}REFPDEN (MIN) is satisfied, there are cases where additional time such as ^{t}XPDLL (MIN) is required.

[38] ODT turn-on time MIN is when the device leaves High-Z and ODT resistance begins to turn on. ODT turn-on time maximum is when the ODT resistance is fully on. The ODT reference load is shown. This output load is used for ODT timings. Designs that were created prior to JEDEC tightening the maxi- mum limit from 9ns to 8.5ns will be allowed to have a 9ns maximum.

[39] Half-clock output parameters must be derated by the actual ^{t}ERR10per and ^{t}JITdty when input clock jitter is present. This results in each parameter becoming larger. The parameters ^{t}ADC (MIN) and ^{t}AOF (MIN) are each required to be derated by subtracting both ^{t}ERR10per (MAX) and ^{t}JITdty (MAX). The parameters ^{t}ADC (MAX) and ^{t}AOF (MAX) are required to be derated by subtracting both ^{t}ERR10per (MAX) and ^{t}JITdty(MAX).

[40] ODT turn-off time minimum is when the device starts to turn off ODT resistance. ODT turn- off time maximum is when the DRAM buffer is in High-Z. The ODT reference load is shown. This output load is used for ODT timings.

[41] Pulse width of a input signal is defined as the width between the first crossing of $V_{REF(DC)}$ and the consecutive crossing of $V_{REF(DC)}$.

[42] Should the clock rate be larger than ^{t}RFC (MIN), an AUTO REFRESH command should have at least one NOP command between it and another AUTO REFRESH command. Additionally, if the clock rate is slower than 40ns (25 MHz), all REFRESH commands should be followed by a PRECHARGE ALL command.

[43] DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to a particular row address may result in a reduction of REFRESH characteristics or product lifetime.

[44] When two $V_{IH(AC)}$ values (and two corresponding $V_{IL(AC)}$ values) are listed for a specific speed bin, the user may choose either value for the input AC level. Whichever value is used, the associated setup time for that AC level must also be used. Additionally, one $V_{IH(AC)}$ value may be used for address/command inputs and the other $V_{IH(AC)}$ value may be used for data inputs.

For example, for DDR3-800, two input AC levels are defined: $V_{IH(AC175),min}$ and $V_{IH(AC150),min}$ (corresponding $V_{IL(AC175),min}$ and $V_{IL(AC150),min}$). For DDR3-800, the address/ command inputs must use either $V_{IH(AC175),min}$ with ^{t}IS(AC175) of 200ps or $V_{IH(AC150),min}$ with ^{t}IS(AC150) of 350ps; independently, the data inputs must use either $V_{IH(AC175),min}$ with ^{t}DS(AC175) of 75ps or $V_{IH(AC150),min}$ with ^{t}DS(AC150) of 125ps.

4. Functional Description and Timing

4.1. Simplified State Diagram

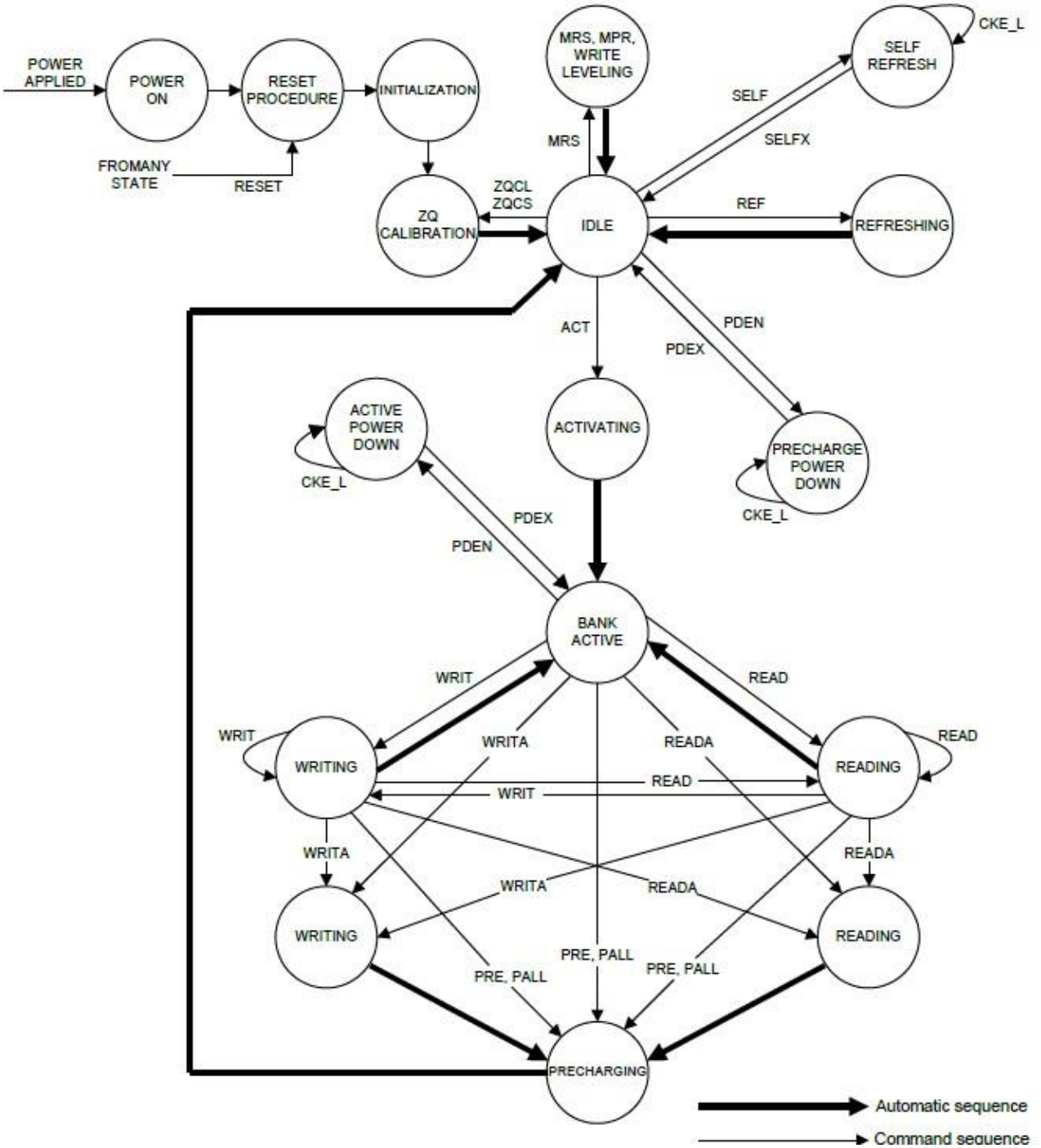


Figure 6 State Diagram

4.2. RESET and Initialization Procedure

Power-Up and Initialization Sequence

[1] Apply power

- RESET# is recommended to be maintained below 0.2 x VDD, all other inputs may be undefined.
- RESET# needs to be maintained for minimum 200us with stable power. CKE is pulled low anytime before RESET# being de-asserted (min. time 10ns). The power voltage ramp time between 300mV to VDD (min.) must be no greater than 200ms; and during the ramp, VDD > VDDQ and (VDD - VDDQ) < 0.3V.
- VDD and VDDQ are driven from a single power converter output.

  AND
- The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.95V max once power ramp is finished.,

  AND
- VREF tracks VDDQ/2.

  OR
- Apply VDD without any slope reversal before or at the same time as VDDQ.
- Apply VDDQ without any slope reversal before or at the same time as VTT and VREF.
- The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.

[2] After RESET# is de-asserted, wait for another 500us until CKE become active. During this time, the DRAM will start internal state initialization; this will be done independently of external clocks.

[3] Clocks (CK, /CK) need to be started and stabilized for at least 10ns or 5tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding set up time to clock (tIS) must be met. Also a NOP or DESL command must be registered (with tIS set up time to clock) before CKE goes active. Once the CKE registered "high" after Reset, CKE needs to be continuously registered high until the initialization sequence is finished, including expiration of tDLLK and tZQinit.

[4] The DDR3 SDRAM will keep its on-die termination in high-impedance state during RESET# being asserted at least until CKE being registered high. Therefore, the ODT signal may be in undefined state until tIS before CKE being registered high. After that, the ODT signal must be kept inactive (low) until the power-up and initialization sequence is finished, including expiration of tDLLK and tZQinit.

[5] After CKE being registered high, wait minimum of tXPR, before issuing the first MRS command to load mode register. (tXPR = max. (tXS ; 5 x tCK))

[6] Issue MRS command to load MR2 with all application settings. (To issue MRS command for MR2, provide low to BA0 and BA2, high to BA1.)

[7] Issue MRS command to load MR3 with all application settings. (To issue MRS command for MR3, provide low to BA2, high to BA0 and BA1.)

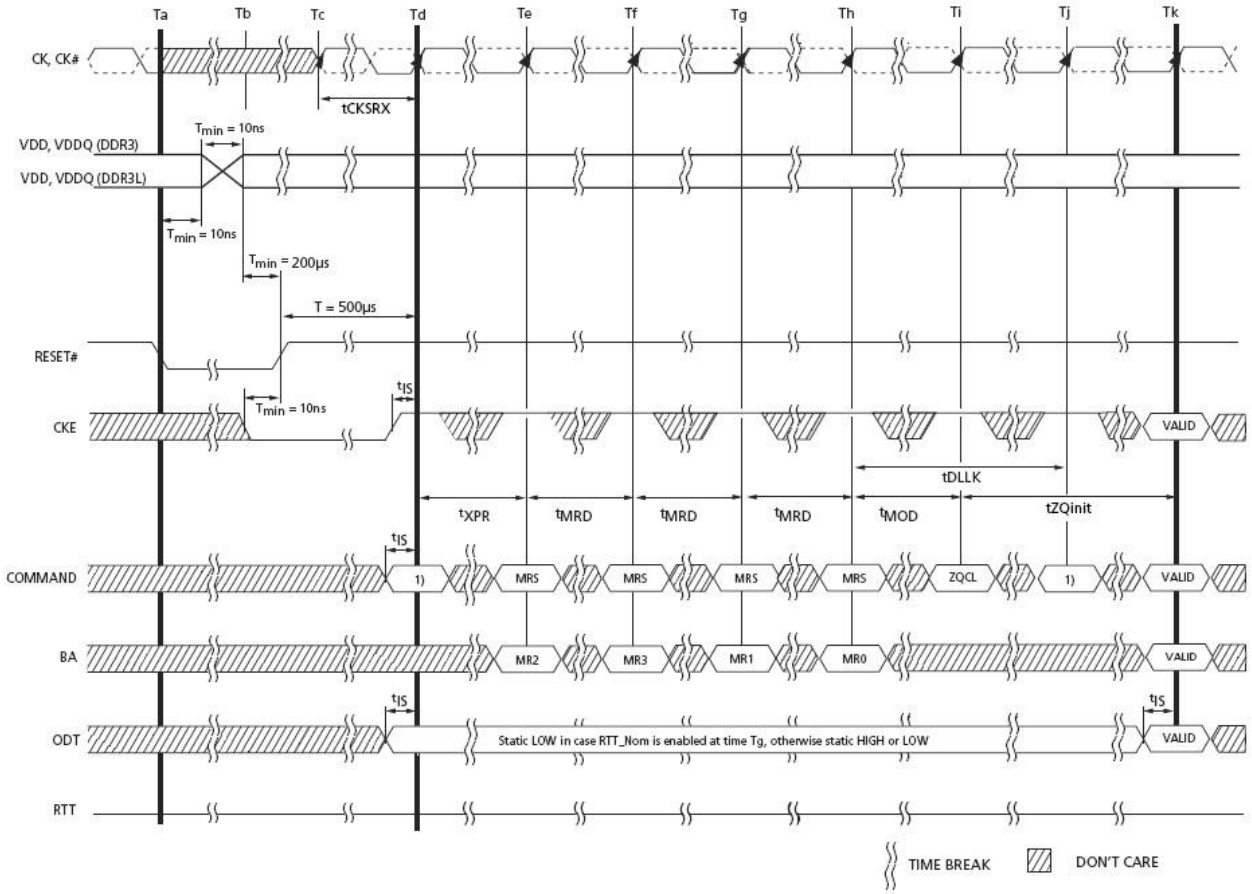
[8] Issue MRS command to load MR1 with all application settings and DLL enabled. (To issue DLL Enable command, provide low to A0, high to BA0 and low to BA1 and BA2.)

[9] Issue MRS command to load MR0 with all application settings and DLL reset. (To issue DLL reset command, provide high to A8 and low to BA0 to BA2.)

[10] Issue ZQCL command to start ZQ calibration.

[11] Wait for both tDLLK and tZQinit completed.

[12] The DDR3 SDRAM is now ready for normal operation.



Note: From time point Td until Tk, NOP or DES commands must be applied between MRS and ZQCL commands.

Figure 7 Reset Procedure at Power Stable Condition

4.3. Programming the Mode Register

For application flexibility, various functions, features and modes are programmable in four mode registers, provided by the DDR3 SDRAM, as user defined variables, and they must be programmed via a Mode Register Set (MRS) command. As the default values of the Mode Registers (MR#) are not defined, content of mode registers must be fully initialized and/or reinitialized, i.e. written, after Power-up and/or reset for proper operation. Also the contents of the mode registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset does not affect array contents, which means these commands can be executed any time after power-up without affecting the array contents.
The mode register set command cycle time, tMRD is required to complete the write operation to the mode register and is the minimum time required between two MRS commands. The MRS command to non-MRS command delay, tMOD, is required for the DRAM to update the features except DLL reset and is the minimum time required from an MRS command to a non-MRS command excluding NOP and DESL. The mode register contents can be changed using the same command and timing requirements during normal operation as long as the DRAM is in idle state, i.e. all banks are in the precharged state with tRP satisfied, all data bursts are completed and CKE is already high prior to writing into the mode register. The mode registers are divided into various fields depending on the functionality and/or modes.

Mode Register Set Command Cycle Time (tMRD)

tMRD is the minimum time required from an MRS command to the next MRS command. As DLL enable and DLL reset are both MRS commands, tMRD is applicable between MRS to MR1 for DLL enable and MRS to MR0 for DLL reset, and not tMOD.

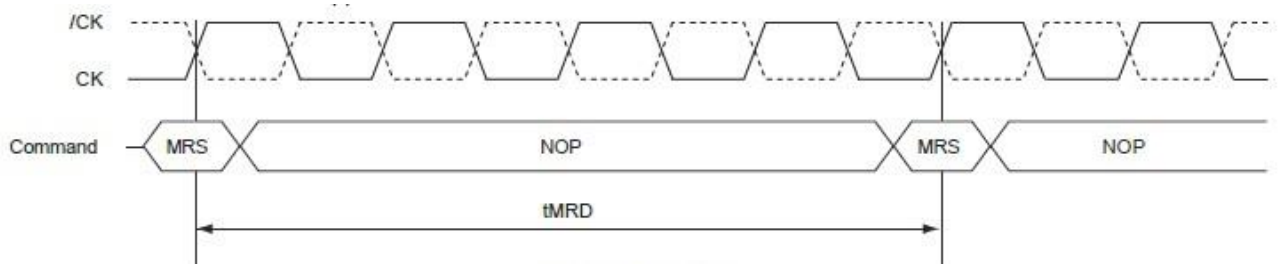


Figure 8 tMRD Timing

MRS Command to Non-MRS Command Delay (tMOD)

tMOD is the minimum time required from an MRS command to a non-MRS command excluding NOP and DESL. Note that additional restrictions may apply, for example, MRS to MR0 for DLL reset followed by read.

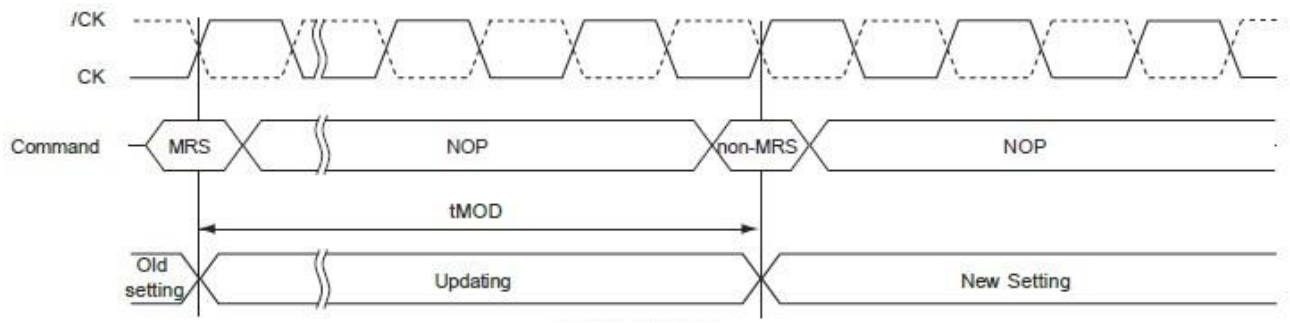


Figure 9 tMOD Timing

4.4. DDR3 SDRAM Mode Register 0 [MR0]

The Mode Register MR0 stores the data for controlling various operating modes of DDR3 SDRAM. It controls burst length, read burst type, CAS# latency, test mode, DLL reset, WR and DLL control for precharge power-down, which include various vendor specific options to make DDR3 SDRAM useful for various applications. The mode register is written by asserting low on CS#, RAS#, CAS#, WE#, BA0, BA1 and BA2, while controlling the states of address pins according to the table below.

BA2	BA1	BA0	A14~A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Field
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
0*1	0	0	0*1	PPD	WR			DLL	TM	CAS Latency			RBT	CL	BL		Mode Register 0

A8	DLL Reset
0	No
1	Yes

A7	Mode
0	Normal
1	Test

A3	Read Burst Type
0	Nibble Sequential
1	Interleave

Burst Length		
A1	A0	BL
0	0	8(Fixed)
0	1	4or 8(on the fly)
1	0	4(Fixed)
1	1	Reserved

A12	DLL Control for Precharge PD
0	Slow exit(DLL off)
1	Fast exit(DLL on)

BA1	BA0	MR Select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

Write recovery for autoprecharge			
A11	A10	A9	WR(cycle)
0	0	0	Reserved
0	0	1	5*2
0	1	0	6*2
0	1	1	7*2
1	0	0	8*2
1	0	1	10*2
1	1	0	12*2
1	1	1	14*2

CAS Latency				
A6	A5	A4	A2	Latency
0	0	0	0	Reserved
0	0	1	0	5
0	1	0	0	6
0	1	1	0	7
1	0	0	0	8
1	0	1	0	9
1	1	0	0	10
1	1	1	0	11
0	0	0	1	12
0	0	1	1	13
0	1	0	1	14

Figure 10 MR0 Programming

Notes:
[1] BA2 and A13 ~ A14 are reserved for future use and must be programmed to 0 during MRS.
[2] WR (Write Recovery for auto precharge) min in clock cycle is calculated by dividing tWR (in ns) by tCK (in ns) and rounding up to the next integer:
[3] WR min [cycles] = roundup (tWR [ns] / tCK [ns]).
[4] The WR value in the mode register must be programmed to be equal or larger than WR min. The programmed WR value is used with tRP to determine tDAL.

4.5. DDR3 SDRAM Mode Register 1 [MR1]

The Mode Register MR1 stores the data for enabling or disabling the DLL, output driver strength, RTT_Nom impedance, additive latency, write leveling enable and Qoff. The Mode Register 1 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA0 and low on BA1, while controlling the states of address pins according to the table below.

BA2	BA1	BA0	A14~A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Field
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
0*1	0	1	0*1	Qoff	TDQS	0*1	Rtt_Nom	0*1	Level	Rtt_Nom	D.I.C	AL		Rtt_Nom	D.I.C	DLL	Mode Register 1

A11	DLL enable
0	Disabled
1	Enabled

A7	Write leveling enable
0	Disabled
1	Enabled

A4	A3	Additive Latency
0	0	0(AL disabled)
0	1	CL-1
1	0	CL-2
1	1	Reserved

A12	Qoff*2
0	Output buffer enabled
1	Output buffer disabled*2

BA1	BA0	MR Select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A9	A6	A2	Rtt Nom*5
0	0	0	Rtt_Nom disabled
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/12*4
1	0	1	RZQ/8*4
1	1	0	Reserved
1	1	1	Reserved

A0	DLL Enable
0	Enable
1	Disable

A5	A1	Output Driver Impedance Control
0	0	RZQ/6
0	1	RZQ/7
1	0	Reserved
1	1	Reserved

Figure 11 MR1 Programming

Notes:
[1] BA2, A8, A10, A11 and A13 ~ A14 are reserved for future use (RFU) and must be programmed to 0 during MRS.
[2] Outputs disabled - DQ, DQS, /DQS.
[3] RZQ = 240 Ohm.
[4] If RTT_Nom is used during writes, only the values RZQ/2, RZQ/4 and RZQ/6 are allowed. [5] In write leveling mode (MR1[bit7] = 1) with MR1[bit12] = 1, all RTT_Nom settings are allowed; in write leveling mode (MR1[bit7] = 1) with MR1[bit12] = 0, only RTT_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed.

4.6. DDR3 SDRAM Mode Register 2 [MR2]

The Mode Register MR2 stores the data for controlling refresh related features, RTT_WR impedance and CAS# write latency (CWL). The Mode Register 2 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA1 and low on BA0, while controlling the states of address pins according to the table below.

BA2	BA1	BA0	A14~A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Field
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
0*1	1	0	0*1			Rtt_WR*2		0*1	SRT	ASR	CWL			PASR*3			Mode Register 2

A7	Self-Refresh Temperature (SRT)range
0	Normal temperature range
1	Extended temperature range

A6	Auto Self-Refresh(ASR)
0	Manual SR Refresh(SRT)
1	ASR enable(optional)

A10	A9	Rtt_WR
0	0	Dynamic ODT Off(write does not affect Rtt value)
0	1	RZQ/4
1	0	RZQ/2
1	1	Reserved

BA1	BA0	MR Select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A2	A1	A0	Partial Array Self-Refresh	
0	0	0	Full	——
0	0	1	Half :Bank0~3	(BA[2:0]=000,001,010,011)
0	1	0	Quarter :Bank0~1	(BA[2:0]=000,001)
0	1	1	1/8 :Bank0	(BA[2:0]=000)
1	0	0	3/4 :Bank2~7	(BA[2:0]=010,011,100,101,110,111)
1	0	1	Half :Bank4~7	(BA[2:0]=100,101,110,111)
1	1	0	Quarter :Bank6~7	(BA[2:0]=110,111)
1	1	1	1/8 :Bank7	(BA[2:0]=111)

A5	A4	A3	CAS write Latency(CWL)
0	0	0	5(tCK≥2.5ns)
0	0	1	6(2.5ns>tCK≥1.875ns)
0	1	0	7(1.875ns>tCK≥1.5ns)
0	1	1	8(1.5ns>tCK≥1.25ns)
1	0	0	9(1.25ns>tCK≥1.07ns)
1	0	1	10(1.07ns>tCK≥0.935ns)
1	1	0	11(0.935ns>tCK≥0.833ns)
1	1	1	12(0.833ns>tCK≥0.75ns)

Figure 12 MR2 Programming

Notes:
[1] BA2, A8 and A11 to A14 are RFU and must be programmed to 0 during MRS.
[2] The Rtt_WR value can be applied during writes even when Rtt_Nom is desabled. During write leveling, Dynamic ODT is not available.
[3] Optional in DDR3 SDRAM: If PASR (Partial Array Self-Refresh) is enabled, data located in areas of the array beyond the specified address range will be lost if self-refresh is entered. Data integrity will be maintained if tREF conditions are met and no self-refresh command is issued.

4.7. DDR3 SDRAM Mode Register 3 [MR3]

The Mode Register MR3 controls Multi Purpose Registers (MPR). The Mode Register 3 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA1 and BA0, while controlling the states of address pins according to the table below.

BA2	BA1	BA0	A14~A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Field
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
0*1	1	1	0*1											MPR	MPR Loc		Mode Register 3

MPR Operation

A2	MPR
0	Normal operation*3
1	Dataflow from MPR

MPR Address

A1	A0	MPR location
0	0	Predefined pattern *2
0	1	RFU
1	0	RFU
1	1	RFU

BA1	BA0	MR Select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

Figure 13 MR3 Programming

Notes:
[1] BA2, A3 to A14 are reserved for future use (RFU) and must be programmed to 0 during MRS.
[2] The predefined pattern will be used for read synchronization.
[3] When MPR control is set for normal operation, MR3 A[2]=0, MR3 A[1:0] will be ignored.

4.8. Extended Temperature Usage

[Table 27] Mode Register Description

Field	Bits	Description
ASR	MR2(A6)	Auto Self-Refresh (ASR) when enabled, DDR3 SDRAM automatically provides Self-Refresh power management functions for all supported operating temperature values. If not enabled, the SRT bit must be programmed to indicate TC during subsequent Self-Refresh operation 0=Manual SR Reference(SRT) 1=ASR enable
SRT	MR2(A7)	Self-Refresh Temperature (SRT) Range If ASR =0, the SRT bit must be programmed to indicate TC during subsequent Self-Refresh operation If ASR=1. SRT bit must be set to Ob 0=Normal operating temperature range 1=Extended(optional) operating temperature range

Partial Array Self-Refresh (PASR)

Optional in DDR3 SDRAM: Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material. If PASR (Partial Array Self-Refresh) is enabled, data located in areas of the array beyond the specified address range shown in figure of MR2 programming will be lost if Self-Refresh is entered. Data integrity will be maintained if tREFI conditions are met and no Self-Refresh command is issued.

Auto Self-Refresh Mode - ASR Mode

DDR3 SDRAM provides an Auto Self-Refresh mode (ASR) for application ease. ASR mode is enabled by setting MR2 bit A6 = 1 and MR2 bit A7 = 0. The DRAM will manage self-refresh entry in either the Normal or Extended (optional) Temperature Ranges. In this mode, the DRAM will also manage self-refresh power consumption when the DRAM operating temperature changes, lower at low temperatures and higher

at high temperatures.
If the ASR option is not supported by the DRAM, MR2 bit A6 must be set to 0.
If the ASR mode is not enabled (MR2 bit A6 = 0), the SRT bit (MR2 A7) must be manually programmed with the operating temperature range required during self-refresh operation. Support of the ASR option does not automatically imply support of the Extended Temperature Range.

Self- Refresh Temperature Range - SRT

If ASR = 0, the Self-Refresh Temperature (SRT) Range bit must be programmed to guarantee proper self-refresh operation.
If SRT = 0, then the DRAM will set an appropriate refresh rate for self-refresh operation in the Normal Temperature Range.
If SRT = 1 then the DRAM will set an appropriate, potentially different, refresh rate to allow self-refresh operation in either the Normal or Extended Temperature Ranges. The value of the SRT bit can effect self-refresh power consumption, please refer to the IDD table for details.
For parts that do not support the Extended Temperature Range, MR2 bit A7 must be set to 0 and the DRAM should not be operated outside the Normal Temperature Range.

[Table 28] Self-Refresh Mode Summary

MR2 A[6]	MR2 A[7]	Self-Refresh operation	Allowed Operating Temperature Range for Self-Refresh Mode
0	0	Self-refresh rate appropriate for the Normal Temperature Range	Normal (0-85℃)
0	1	Self-refresh rate appropriate for either the Normal or Extended Temperature Ranges. The DRAM must support Extended Temperature Range. The value of the SRT bit can effect self-refresh power consumption, please refer to the IDD table for details.	Normal and Extended (0-95℃)
1	0	ASR enabled. Self-Refresh power consumption is temperature dependent	Normal(0-85℃)
1	0	ASR enabled. Self-Refresh power consumption is temperature dependent	Normal and Extended(0-95℃)
1	1	Illegal	

4.9. Refresh Command

The refresh command (REF) is used during normal operation of the DDR3 SDRAMs. This command is non- persistent, so it must be issued each time a refresh is required. The DDR3 SDRAM requires refresh cycles at an average periodic interval of tREFI. When CS#, RAS# and CAS# are held low and WE# high at the rising edge of the clock, the chip enters a refresh cycle. All banks of the SDRAM must be precharged and idle for a minimum of the precharge time tRP(min) before the refresh command can be applied. The refresh addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during a refresh command. An internal address counter supplies the addresses during the refresh cycle. No control of the external address bus is required once this cycle has started. When the refresh cycle has completed, all banks of the SDRAM will be in the precharged (idle) state. A delay between the refresh command and the next valid command, except NOP or DESL, must be greater than or equal to the minimum refresh cycle time tRFC(min) as shown in the following figure. Note that the tRFC timing parameter depends on memory density.
In general, a refresh command needs to be issued to the DDR3 SDRAM regularly every tREFI interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of 8 refresh commands can be postponed during operation of the DDR3 SDRAM, meaning that at no point in time more than a total of 8 refresh commands are allowed to be postponed. In case that 8 refresh commands are postponed in a row, the resulting maximum interval between the surrounding refresh commands is limited to 9 × tREFI. A maximum of 8 additional refresh commands can be issued in advance ("pulled in"), with each one reducing the number of regular refresh commands required later by one. Note that pulling in more than 8 refresh commands in advance does not further reduce the number of regular refresh commands required later, so that the resulting maximum interval between two surrounding refresh commands is limited to 9 × tREFI. At any given time, a maximum of 16 REF commands can be issued within 2 × tREFI.
Self-refresh mode may be entered with a maximum of eight refresh commands being postponed. After exiting self-refresh mode with one or more refresh commands postponed, additional refresh commands may be postponed to the extent that the total number of postponed refresh commands (before and after the self-refresh) will never exceed eight. During self-refresh mode, the number of postponed or pulled-in REF commands does not change.

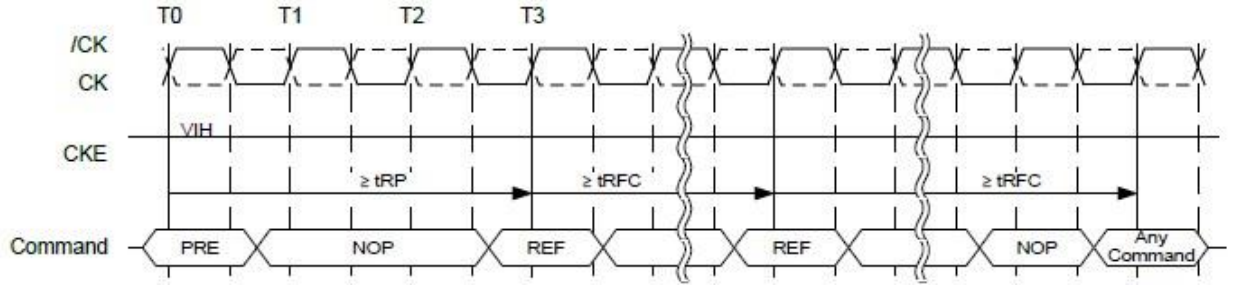


Figure 14 Refresh Command Timing

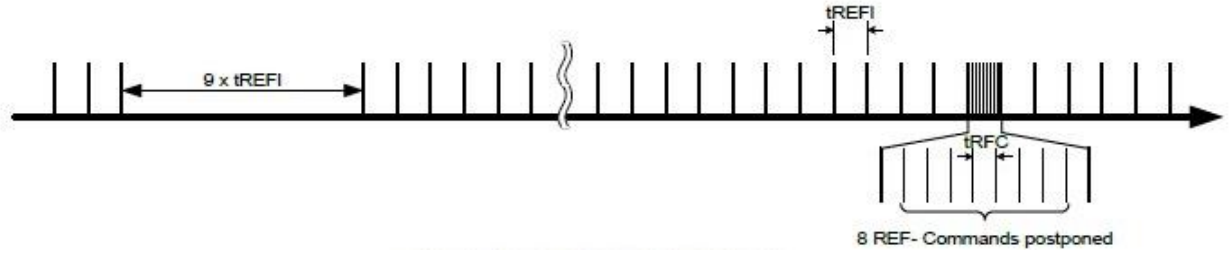


Figure 15 Postponing Refresh Commands

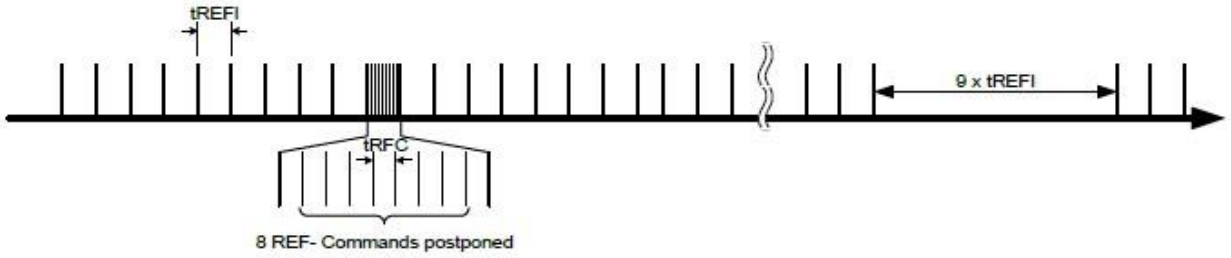


Figure 16 Pulling-in Refresh Commands

4.10. Self-Refresh Operation

The self-refresh command can be used to retain data in the DDR3 SDRAM, even if the rest of the system is powered down. When in the self-refresh mode, the DDR3 SDRAM retains data without external clocking. The DDR3 SDRAM device has a built-in timer to accommodate self-refresh operation. The self-refresh entry (SELF) command is defined by having CS#, RAS#, CAS# and CKE held low with WE# high at the rising edge of the clock.

Before issuing the self-refresh entry command, the DDR3 SDRAM must be idle with all bank precharge state with tRP satisfied. 'Idle state' is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.) Also, on-die termination must be turned off before issuing self-refresh entry command, by either registering ODT pin low "ODTL + 0.5tCK" prior to the self-refresh entry command or using MRS to MR1 command. Once the self-refresh entry command is registered, CKE must be held low to keep the device in self-refresh mode. During normal operation (DLL on), MR1 (A0 = 0), the DLL is automatically disabled upon entering self-refresh and is automatically enabled (including a DLL-Reset) upon exiting self-refresh.

When the DDR3 SDRAM has entered self-refresh mode all of the external control signals, except CKE and RESET#, are "don't care". For proper self-refresh operation, all power supply and reference pins (VDD, VDDQ, VSS, VSSQ, VREFCA and VREFDQ) must be at valid levels. VREFDQ supply may be turned OFF and VREFDQ may take any value between VSS and VDD during self-refresh operation, provided that VREFDQ is valid and stable prior to CKE going back high and that first write operation or first write leveling activity may not occur earlier than 512 nCK after exit from self-refresh.

The DRAM initiates a minimum of one refresh command internally within tCKESR period once it enters self-refresh mode.

The clock is internally disabled during self-refresh operation to save power. The minimum time that the DDR3 SDRAM must remain in self-refresh mode is tCKESR. The user may change the external clock frequency or halt the external clock tCKSRE cycles after self-refresh entry is registered, however, the clock must be restarted and stable tCKSRX clock cycles before the device can exit self-refresh operation. To protect DRAM internal delay on CKE line to block the input signals, one NOP (or DESL) command is needed after self-refresh entry.

The procedure for exiting self-refresh requires a sequence of events. First, the clock must be stable prior to CKE going back high. Once a self-refresh exit command (SREX, combination of CKE going high and either NOP or DESL on command bus) is registered, a delay of at least tXS must be satisfied before a valid command not requiring a locked DLL can be issued to the device to allow for any internal refresh in progress.

Before a command that requires a locked DLL can be applied, a delay of at least tXSDLL must be satisfied.

Depending on the system environment and the amount of time spent in self-refresh, ZQ calibration commands may be required to compensate for the voltage and temperature drift as described in ZQ Calibration section. To issue ZQ calibration commands, applicable timing requirements must be satisfied (See Figure ZQ Calibration).

CKE must remain high for the entire self-refresh exit period tXSDLL for proper operation except for self-refresh re-entry. Upon exit from self-refresh, the DDR3 SDRAM can be put back into self-refresh mode after waiting at least tXS period and issuing one refresh command (refresh period of tRFC). NOP or DESL commands must be registered on each positive clock edge during the self-refresh exit interval tXS. ODT must be turned off during tXSDLL.

The use of self-refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from self-refresh mode. Upon exit from self-refresh, the DDR3 SDRAM requires a minimum of one extra refresh command before it is put back into self-refresh mode.

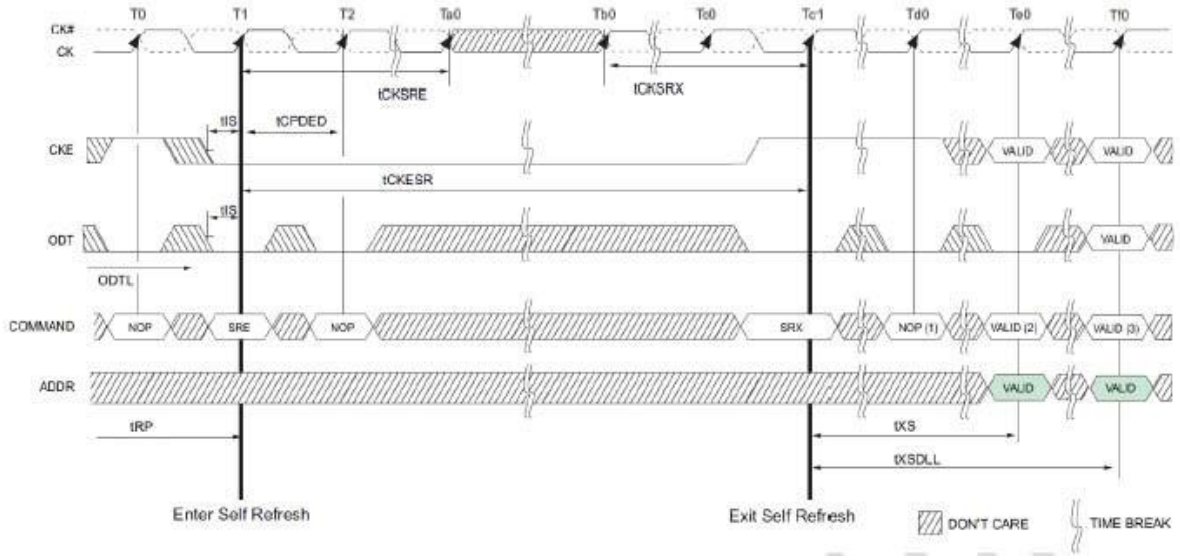


Figure 17 Self-Refresh Entry and Exit Timing

Notes:
[1] Only NOP or DESL commands.
[2] Valid commands not requiring a locked DLL.
[3] Valid commands requiring a locked DLL.
[4] One NOP or DESL commands.

4.11. DLL-off Mode

[Refer to section 4.5 in JEDEC Standard No. JESD79-3F]

4.12. DLL on/off switching procedure

[Refer to section 4.6 in JEDEC Standard No. JESD79-3F]

4.13. Input clock frequency change

[Refer to section 4.7 in JEDEC Standard No. JESD79-3F]

4.14. Write Leveling

[Refer to section 4.8 in JEDEC Standard No. JESD79-3F]

4.15. Multi Purpose Register

[Refer to section 4.10 in JEDEC Standard No. JESD79-3F]

4.16. Read Operation

[Refer to section 4.13 in JEDEC Standard No. JESD79-3F]

4.17. Write Operation

[Refer to section 4.14 in JEDEC Standard No. JESD79-3F]

4.18. Power-Down Modes

[Refer to section 4.17 in JEDEC Standard No. JESD79-3F]

4.19. On-Die Termination (ODT)

[Refer to section 5 in JEDEC Standard No. JESD79-3F]

4.20. ZQ Calibration

[Refer to section 5.5 in JEDEC Standard No. JESD79-3F]

5. Physical Diagram

5.1. FBGA 78-ball ×8bit

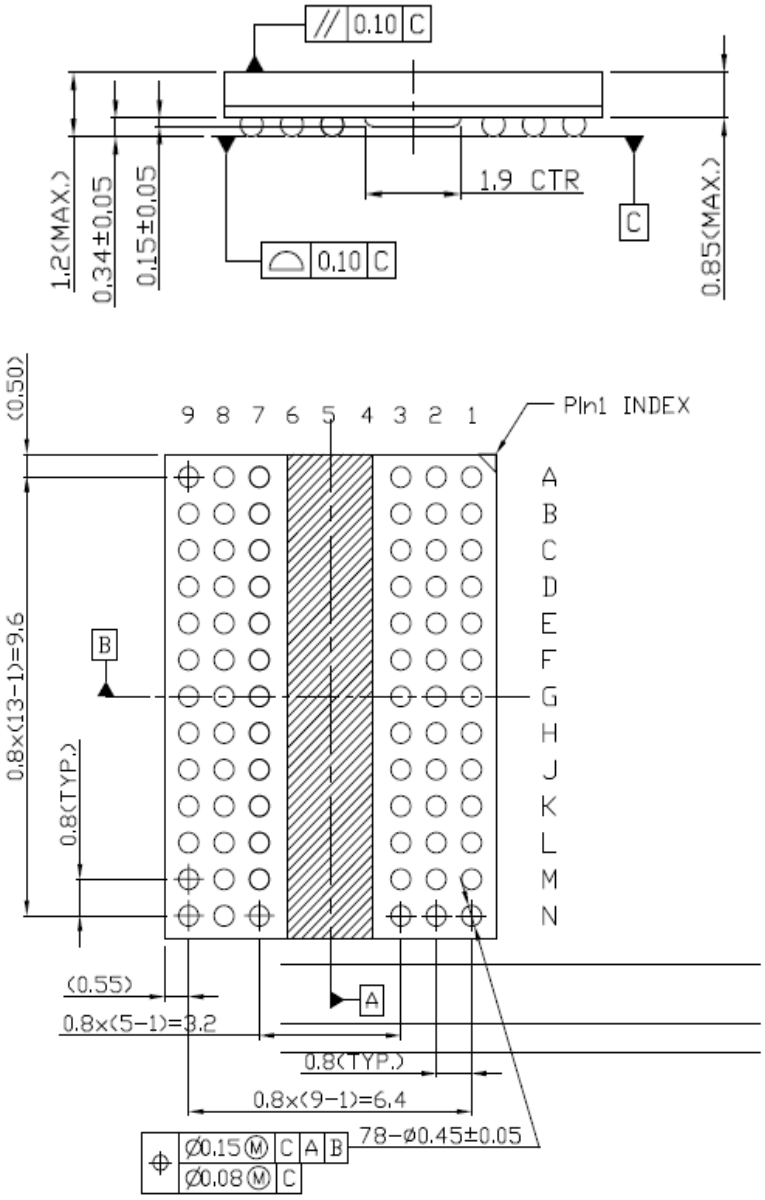


Figure 18 FBGA 78-ball package outline drawing（unit:mm）

5.2. FBGA 96-ball ×16bit

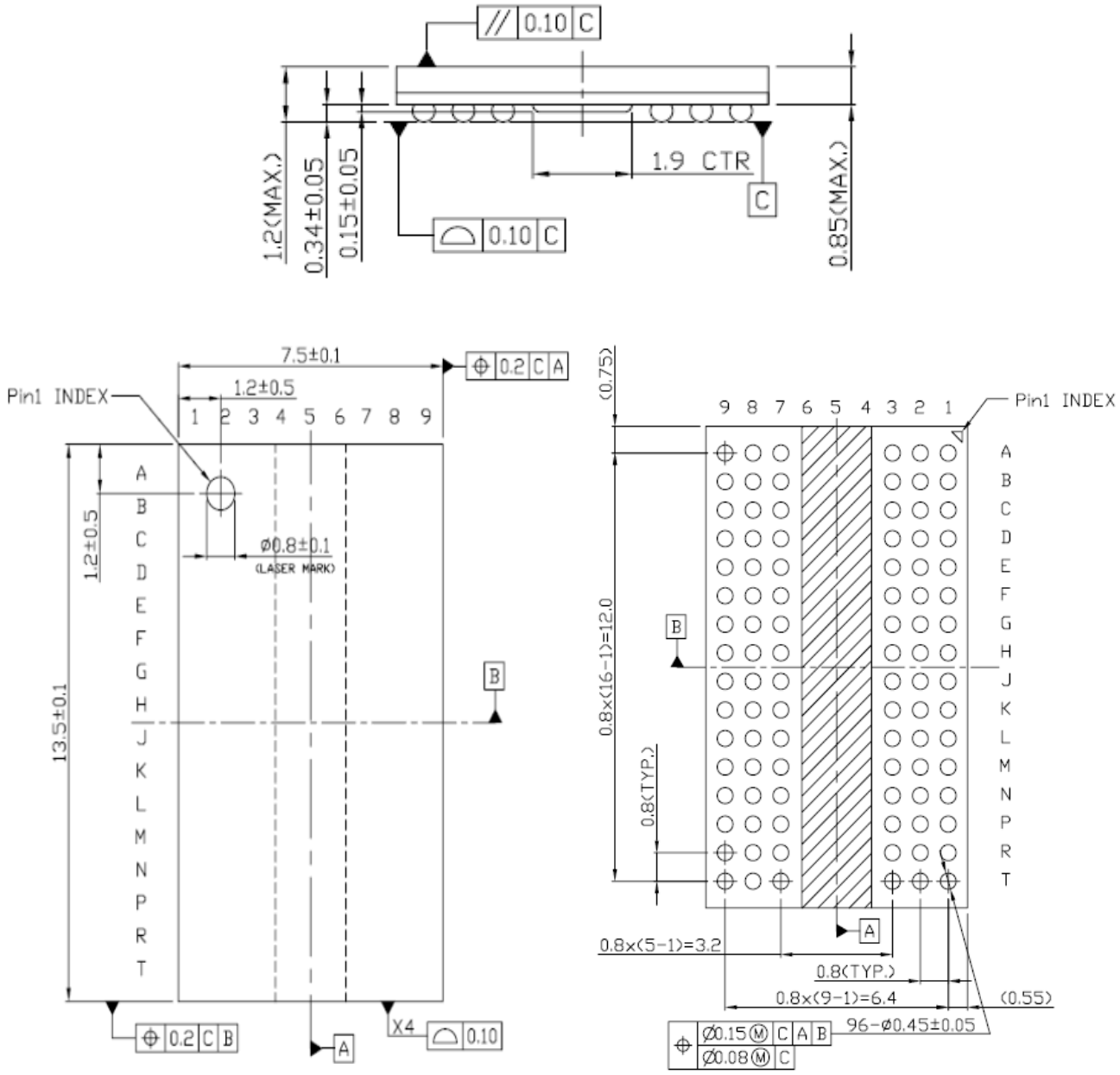


Figure 19 FBGA 96-ball package outline drawing（unit:mm）