FUDAN MICROELECTRONICS

FM17XX Serial Contactless Readers ICS

Datasheet

May. 2008

Content

1. Product Overview

1.1. Introduction

The FM17XX family is common serial reader ICs for contactless communications based on ISO14443. It takes 0.6μm CMOS EEPROM processing technology.

The FM17XX family supports all layers of ISO14443 typeA/typeB and ISO15693 on 13.56MHz. M1 and SH security arithmetic are both supported. The FM17XX family internal highly integrated analog circuitry for modulating/demodulating and thus they can work with the least peripheral circuitry. They support six types of μ-Processor interface. The digital part has two kinds of voltage operation modes: TTL and CMOS mode. The FM17XX family is compatible with RC500、RC530、RC531 and RC632 of Philips. The FM17XX serial reader ICs are optimized for use in public transport、variously charging payment card and comparable applications using contactless communication.

An outstanding feature of the FM17XXL chipset is the lowest operation voltage of all three supplies of theirs can up to 2.9V; this is lays over anything else of the kind.

1.2. Features

- **Highly integrated analog circuitry for modulate/demodulate, only require the least peripheral circuitry**
- **Proximity operating distance (up to 100 mm, depend on the antenna)**
- **Supports ISO14443 typeA & typeB protocol**
- **Supports ISO15693 protocol**
- **512 byte EEPROM**
- **Support M1and SH security arithmetic**
- **Support six types of μ-Processor interface**
- **64 byte FIFO**
- **two voltage operation modes of digital module: TTL/CMOS**
- **Support Standby/Soft Power down mode**
- **Programmable timer**
- **Interrupt controller with smartly interrupt handing**
- **Unique serial number**
- **Serial input/output interface**
- **User programmable start-up configuration**
- **Bit- and byte-oriented framing**
- **Independent power supply pins for digital, analog and transmitter part**
- **All of the FM17XXL's three power supply can operate on low voltage, the lowest operation voltage can reach 2.9V**

1.3. Family

TYPE	PROTOCOL SUPPORTED	SECURITY ARITHMETIC SUPPORTED	COMPATIBLE PHILIPS READERS
FM1702/FM1702L	typeA	M1	RC500、RC530
FM1715/FM1715L	typeA 、typeB	M1、SH	—
FM1725/FM1725L	typeA 、typeB、15693	M1、SH	RC632

Table 1-1 FM17 Family

1.4. Block Diagram

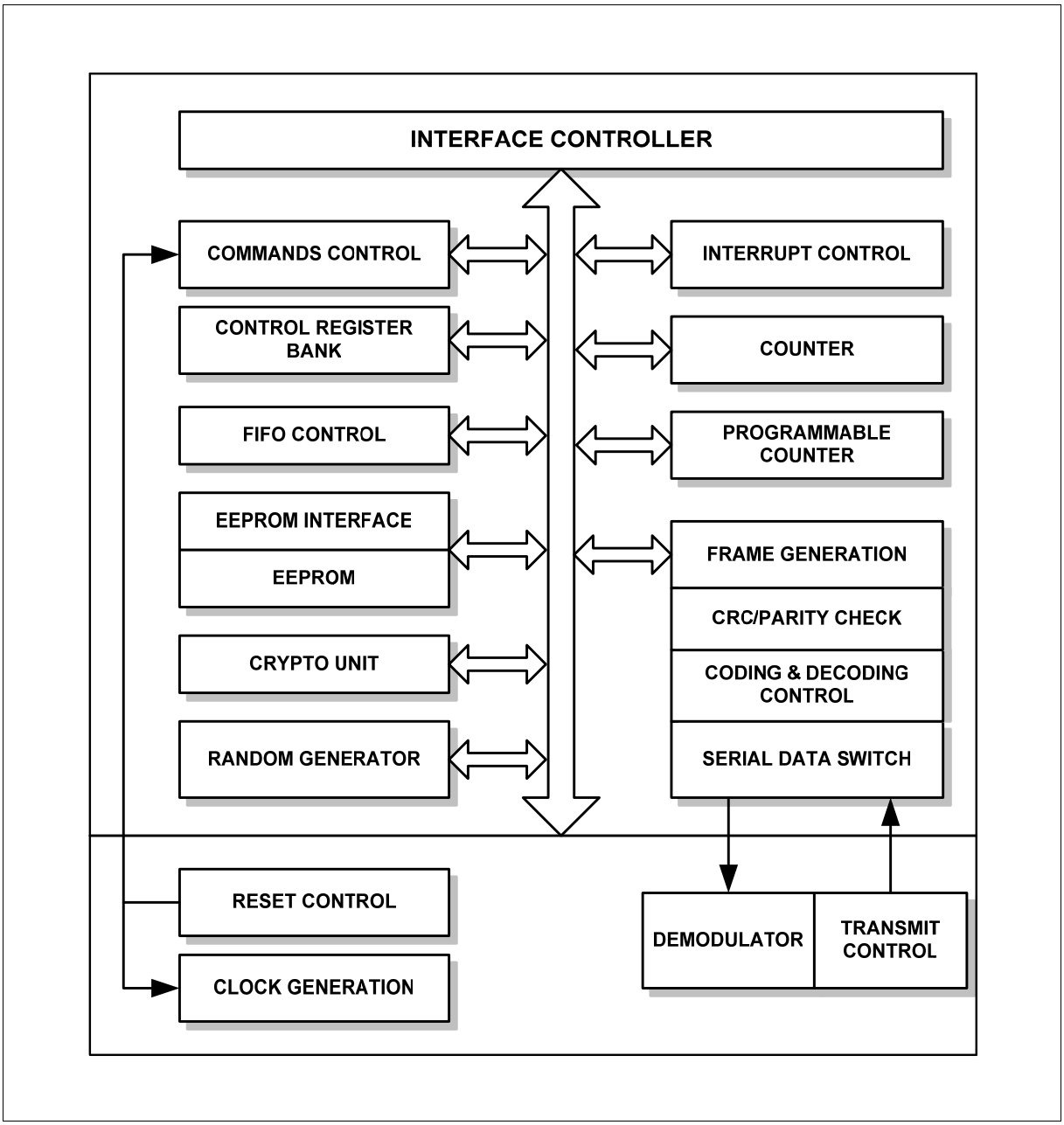


Figure 1-1 FM17XX Block Diagram

1.5. Packaging Type

1.5.1. 32- Pin SOP

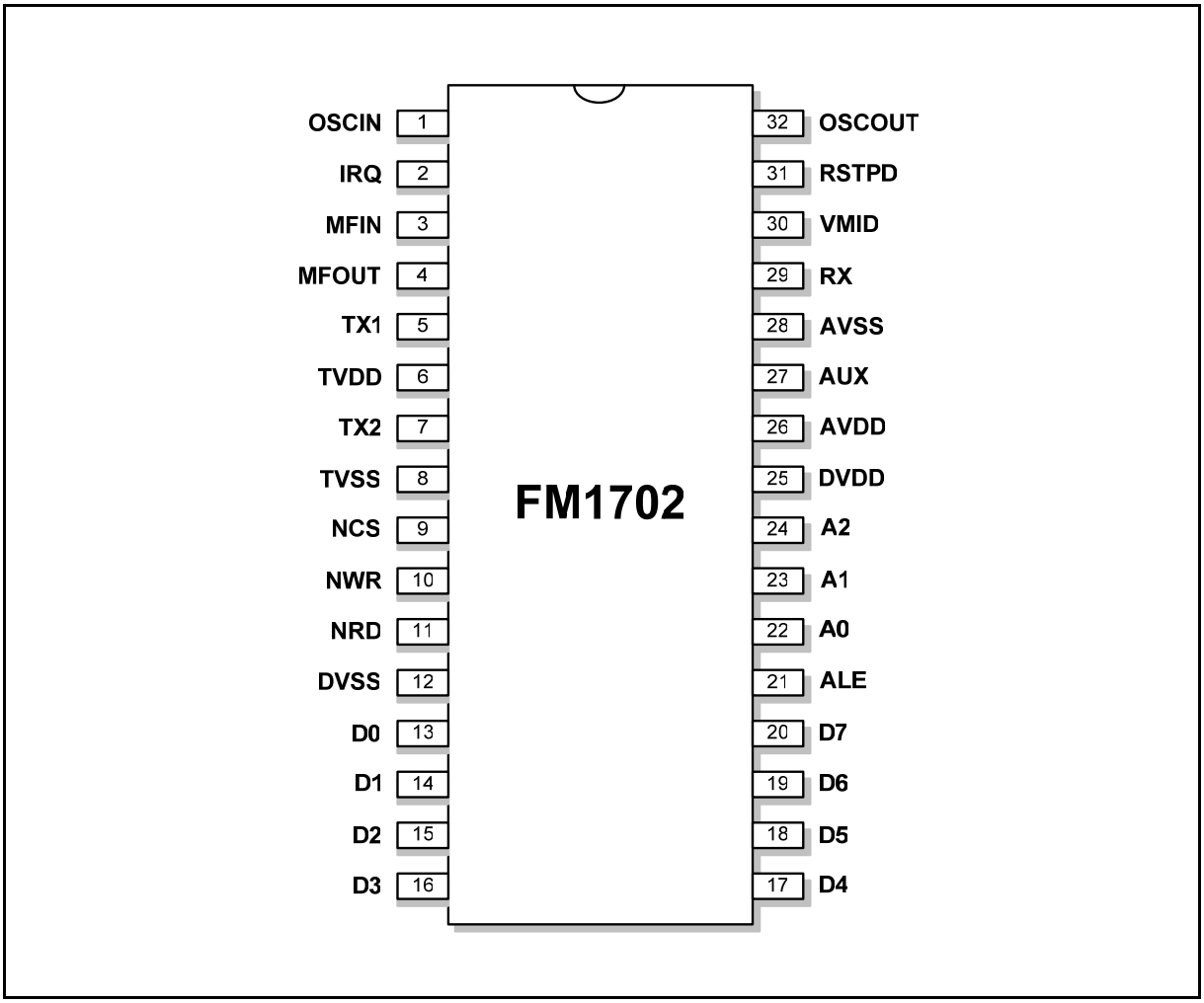


Figure 1-2 FM17XX 32-Pin SOP Pin Assignment

1.5.2. 24- Pin SOP

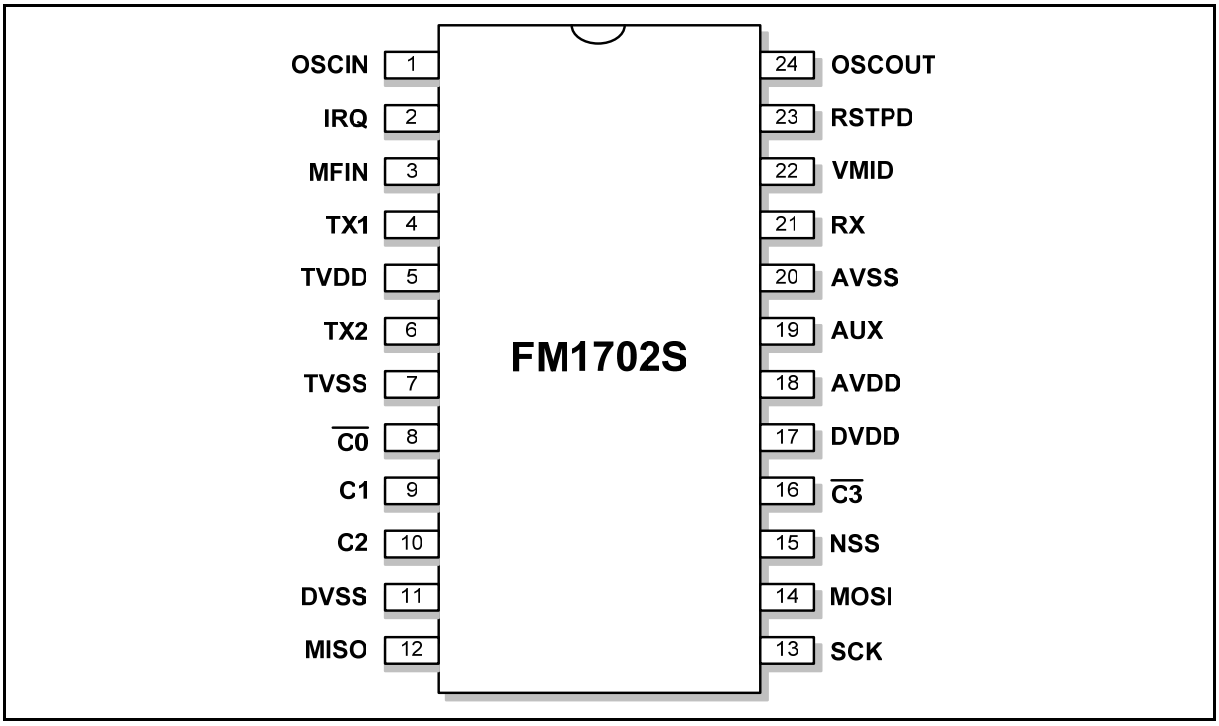


Figure 1-3 FM17XX 24-Pin SOP Pin Assignment

1.5.3. 28-Pin QFN

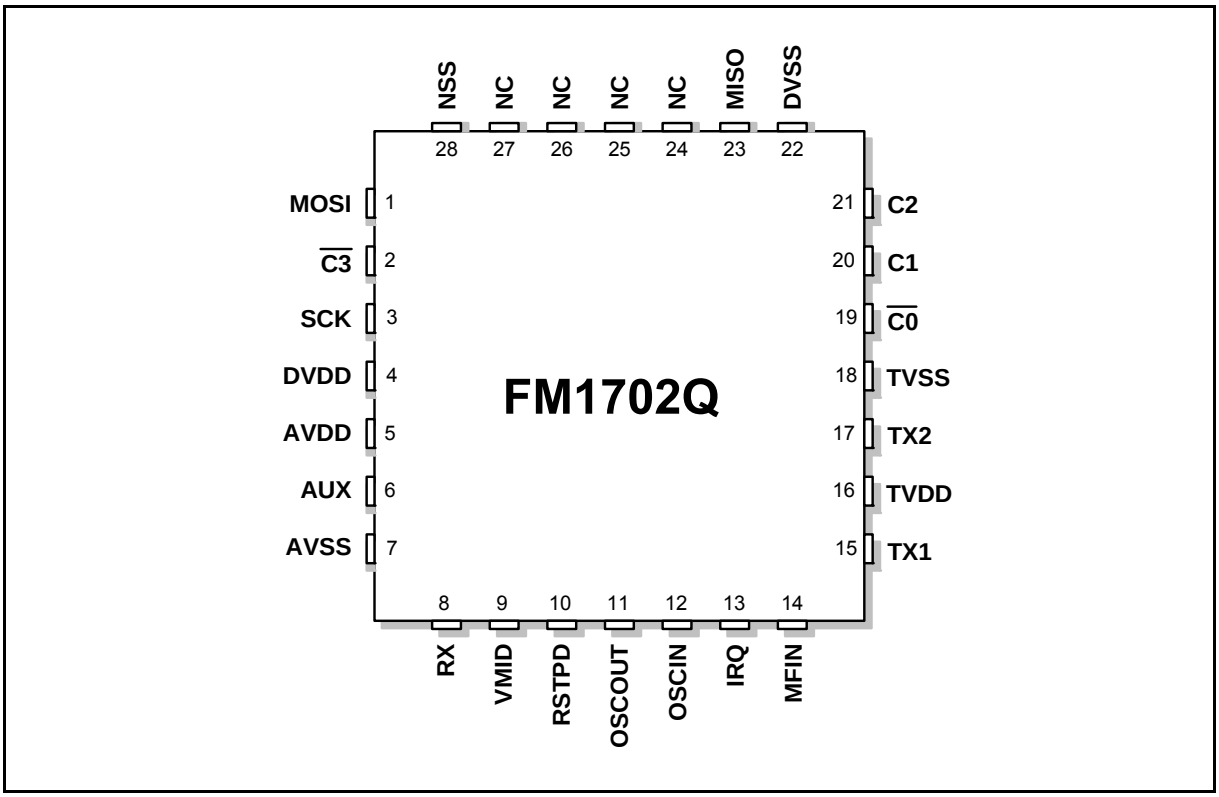


Figure 1-4 FM17XX 28-Pin QFN Pin Assignment

1.6. Pin Description

1.6.1. 32- Pin SOP Pin Description

PIN	SYMBOL	TYPE	DESCRIPTION
1	OSCIN	I	**Crystal Oscillator Input:** fosc = 13.56MHz
2	IRQ	O	**Interrupt Request:** send a signal for interrupt event
3	MFIN	I	**Serial Input:** accepts a digital, serial data stream according to ISO14443A
4	MFOUT	O	**Serial Output:** delivers a serial data stream according to ISO14443A
5	TX1	O	**Transmitter 1:** delivers the modulated 13.56 MHz energy carrier
6	TVDD	PWR	**Transmitter Power Supply:** supplies the output energy for TX1 and TX2
7	TX2	O	**Transmitter 2:** delivers the modulated 13.56 MHz energy carrier
8	TVSS	PWR	**Transmitter Ground**
9	NCS	I	**Not Chip Select:** selects and activates the µ-Processor interface of the FM17XX
10	NWR	I	**Not Write:** strobe to write data into the FM17XX register
	R/NW	I	**Read Not Write:** selects if a read or write cycle shall be performed.
	nWrite	I	**Not Write:** selects if a read or write cycle shall be performed(EPP interface)
11	NRD	I	**Not Read:** strobe to read data from the FM17XX register
	NDS	I	**Not Data Strobe:** strobe for the read and the write cycle
	nDstrb	I	**Not Data Strobe:** strobe for the read and the write cycle
12	DVSS	PWR	**Digital Ground**
13	D0	O	**Master In Slave Out (MISO)** (SPI interface）
13 … 20	D0—D7	I/O	**8 Bit Bi-directional Data Bus**
	AD0—AD7	I/O	**8 Bit Bi-directional Address and Data Bus**
21	ALE	I	**Address Latch Enable:** signal to latch AD0 to AD5 into the internal address latch when high
	AS	I	**Address Strobe:** strobe signal to latch AD0 to AD5 into the internal address latch when high
	nAStrb	I	**Not Address Strobe:** strobe signal to latch AD0 to AD5 into the internal address latch when LOW
	NSS	I	**Not Slave Select:** strobe for the SPI communication
22	A0	I	**Address Line 0:** Bit 0 of register address
	nWait	O	**Not Wait:** signals with LOW that an access-cycle may started and with HIGH that it may be finished（EPP interface）
	MOSI	I	**Master Out Slave In** (SPI interface)
23	A1	I	**Address Line 1:** Bit 1 of register address
24	A2	I	**Address Line 2:** Bit 2 of register address
	SCK	I	**Serial Clock:** Clock for the SPI interface
25	DVDD	PWR	**Digital Power Supply**

Table 1-2 FM17XX 32-Pin SOP Pin Description

PIN	SYMBOL	TYPE	DESCRIPTION
26	AVDD	PWR	**Analog Power Supply**
27	AUX	O	**Auxiliary Output:** This pin delivers analog test signals
28	AVSS	PWR	**Analog Ground**
29	RX	I	**Receiver Input:** Input pin for the cards response
30	VMID	PWR	**Internal Reference Voltage:** This pin delivers the internal reference voltage
31	RSTPD	I	**Reset and Power Down**
32	OSCOUT	O	**Crystal Oscillator Output:** Output of the inverting amplifier of the oscillator

Table 1-3 FM17XX 32-Pin SOP Pin Description (continued)

1.6.2. 24- Pin SOP Pin Description

PIN	SYMBOL	TYPE	DESCRIPTION
1	OSCIN	I	**Crystal Oscillator Input:** fosc = 13.56MHz
2	IRQ	O	**Interrupt Request:** output to signal an interrupt event
3	MFIN	I	**Serial Input:** accepts a digital, serial data stream according to ISO14443A
4	TX1	O	**Transmitter 1:** delivers the modulated 13.56 MHz energy carrier
5	TVDD	PWR	**Transmitter Power Supply:** supplies the output stage of TX1 and TX2
6	TX2	O	**Transmitter 2:** delivers the modulated 13.56 MHz energy carrier
7	TVSS	PWR	**Transmitter Ground**
8	CO	I	**LOW**
9	C1	I	**HIGH**
10	C2	I	**HIGH**
11	DVSS	PWR	**Digital Ground**
12	MISO	O	**Master In Slave Out (MISO)** (SPI interface）
13	SCK	I	**Serial Clock:** Clock for the SPI interface
14	MOSI	I	**Master Out Slave In** (SPI interface)
15	NSS	I	**Not Slave Select:** strobe for the SPI communication
16	C3	I	**LOW**
17	DVDD	PWR	**Digital Power Supply**
18	AVDD	PWR	**Analog Power Supply**
19	AUX	O	**Auxiliary Output:** This pin delivers analog test signals
20	AVSS	PWR	**Analog Ground**
21	RX	I	**Receiver Input:** Input pin for the cards response
22	VMID	PWR	**Internal Reference Voltage:** This pin delivers the internal reference voltage
23	RSTPD	I	**Reset and Power Down**
24	OSCOUT	O	**Crystal Oscillator Output:** Output of the inverting amplifier of the oscillator

Table 1-4 FM17XX 24-Pin SOP Pin Description

1.6.3. 28- Pin QFN Pin Description

PIN	SYMBOL	TYPE	DESCRIPTION
1	MOSI	I	**Master Out Slave In** (SPI interface)
2	C3	I	**LOW**
3	SCK	I	**Serial Clock:** Clock for the SPI interface
4	DVDD	PWR	**Digital Power Supply**
5	AVDD	PWR	**Analog Power Supply**
6	AUX	O	**Auxiliary Output:** This pin delivers analog test signals
7	AVSS	PWR	**Analog Ground**
8	RX	I	**Receiver Input:** Input pin for the cards response
9	VMID	PWR	**Internal Reference Voltage:** This pin delivers the internal reference voltage
10	RSTPD	I	**Reset and Power Down**
11	OSCOUT	O	**Crystal Oscillator Output:** Output of the inverting amplifier of the oscillator
12	OSCIN	I	**Crystal Oscillator Input:** fosc = 13.56MHz
13	IRQ	O	**Interrupt Request:** output to signal an interrupt event
14	MFIN	I	**Serial Input:** accepts a digital, serial data stream according to ISO14443A
15	TX1	O	**Transmitter 1:** delivers the modulated 13.56 MHz energy carrier
16	TVDD	PWR	**Transmitter Power Supply:** supplies the output stage of TX1 and TX2
17	TX2	O	**Transmitter 2:** delivers the modulated 13.56 MHz energy carrier
18	TVSS	PWR	**Transmitter Ground**
19	C0	I	**LOW**
20	C1	I	**HIGH**
21	C2	I	**HIGH**
22	DVSS	PWR	**Digital Ground**
23	MISO	O	**Master In Slave Out (MISO)** (SPI interface）
24	--	--	**NC**
25	--	--	**NC**
26	--	--	**NC**
27	--	--	**NC**
28	NSS	I	**Not Slave Select:** strobe for the SPI communication

Table 1-5 FM17XX 28-Pin QFN Pin Description

2. Command Set

COMMAND	CODE(HEX)	ACTION
StartUp	3F	Runs the Reset and Initialization Phase
Idle	00	No action; cancels current command execution
Transmit	1A	Transmits data from the FIFO
Receive	16	Activates receiver circuitry
Transceive	1E	Transmits data from FIFO buffer to the card
WriteE2	01	Write FIFO data to EEPROM
ReadE2	03	Read data from EEPROM, and puts it into FIFO
LoadKeyE2	0B	Copies a key from the EEPROM into the key buffer
LoadKey	19	Copies a key from the FIFO into the key buffer
Authent1	0C	Performs the first part of the authentication
Authent2	14	Performs the second part of the authentication
LoadConfig	07	Reads data from EEPROM and initializes the registers
CalcCRC	12	Activates the CRC-Coprocessor

Table 2-1 FM17XX Command Set

3. Electrical Characteristics

3.1. Absolute Maximum Ratings

SYMBOL	PARAMETERS	MIN	MAX	UNIT
$T_{amb.abs}$	Ambient or Storage Temperature Range	-40	+150	°C
DVDD AVDD TVDD	DC Supply Voltages	-0.5	6	V
$V_{in.abs}$	Absolute voltage on any digital pin to DVSS	-0.5	DVDD + 0.5	V
$V_{RX.abs}$	Absolute voltage on RX pin to AVSS	-0.5	AVDD + 0.5	V

Table 3-1 FM17XX Absolute Maximum Ratings

3.2. Operating Condition

SYMBOL	PARAMETERS	CONDITION	MIN	TYP	MAX	UNIT
T_{amb}	Ambient Temperature	--	-25	+25	+85	°C
DVDD	Digital Supply Voltage	DVSS = AVSS = TVSS = 0V	2.9	5.0	5.5	V
AVDD	Analog Supply Voltage	DVSS = AVSS = TVSS = 0V	2.9	5.0	5.5	V
TVDD	Transmitter Supply Voltage	DVSS = AVSS = TVSS = 0V	2.9	5.0	5.5	V

Table 3-2 FM17XX Operating Condition

3.3. Current Consumption

SYMBOL	PARAMETERS	CONDITION	MIN	TYP	MAX	UNIT
I_{DVDD}	Digital Supply Current	Idle Command		6	9	mA
		Stand By Command		3	5	mA
		Soft Power Down mode		800	1000	μA
		Hard Power Down mode		1	10	μA
I_{AVDD}	Analog Supply Current	Idle Command, Receiver On		25	40	mA
		Idle Command, Receiver Off		8	12	mA
		Stand By mode		6.5	9	mA
		Soft Power Down mode		1	10	μA
		Hard Power Down mode		1	10	μA
I_{TVDD}	Transmitter Supply Current	Continuous Wave			150	mA
		TX1、TX2 unconnected *TX1RFEn*, *TX2RFEn* = 1		4.5	6	mA
		TX1、TX2 unconnected *TX1RFEn*, *TX2RFEn* = 0		65	130	μA

Table 3-3 FM17XX Current Consumption

4. Timing for SPI Interface

SYMBOL	PARAMETERS	MIN	MAX	UNIT
t_{SCKL}	SCK low pulse width	100		ns
t_{SCKH}	SCK high pulse width	100		ns
t_{SHDX}	SCK high to data changes	20		ns
t_{DXSH}	data changes to SCK high	20		ns
t_{SLDX}	SCK low to data changes		15	ns
t_{SLNH}	SCK low to NSS high	20		ns

Table 4-1 FM17XX SPI Timing Specification

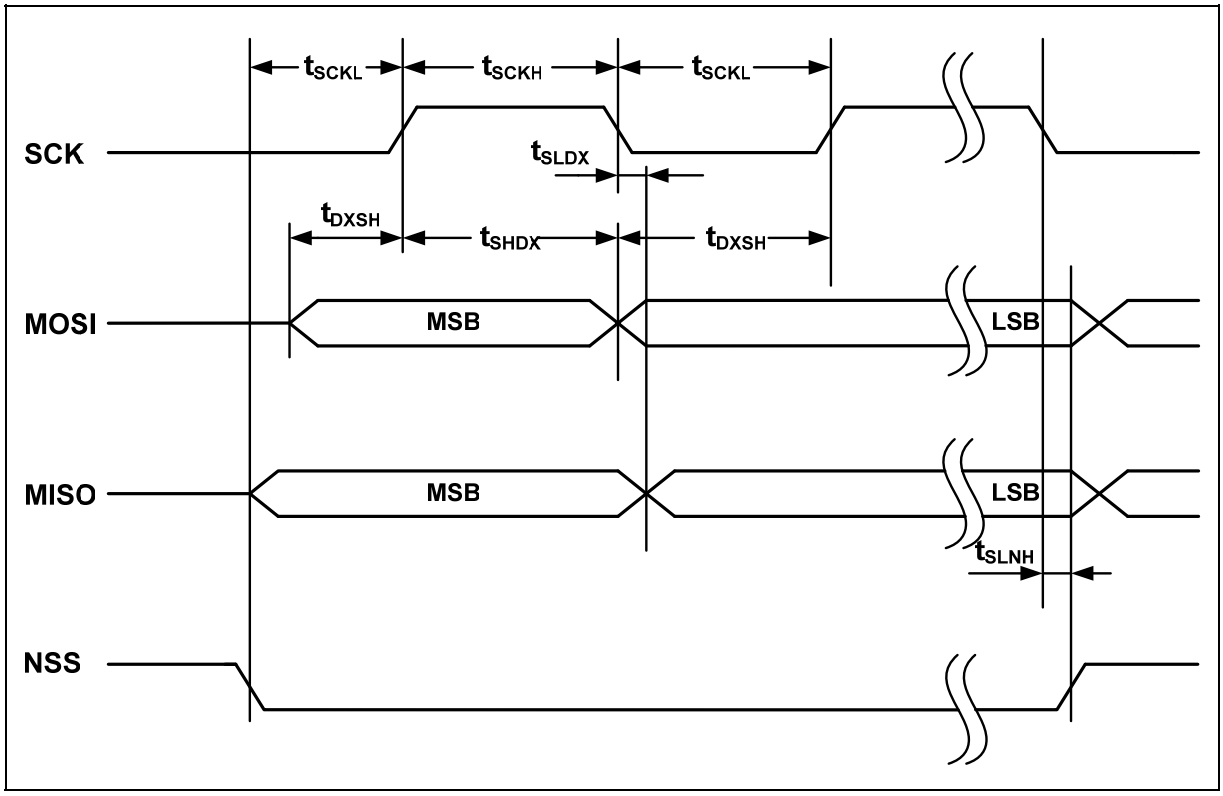


Figure 4-1 FM17XX Timing for SPI Interface

5. Typical Application

Typical application diagram is shown below:

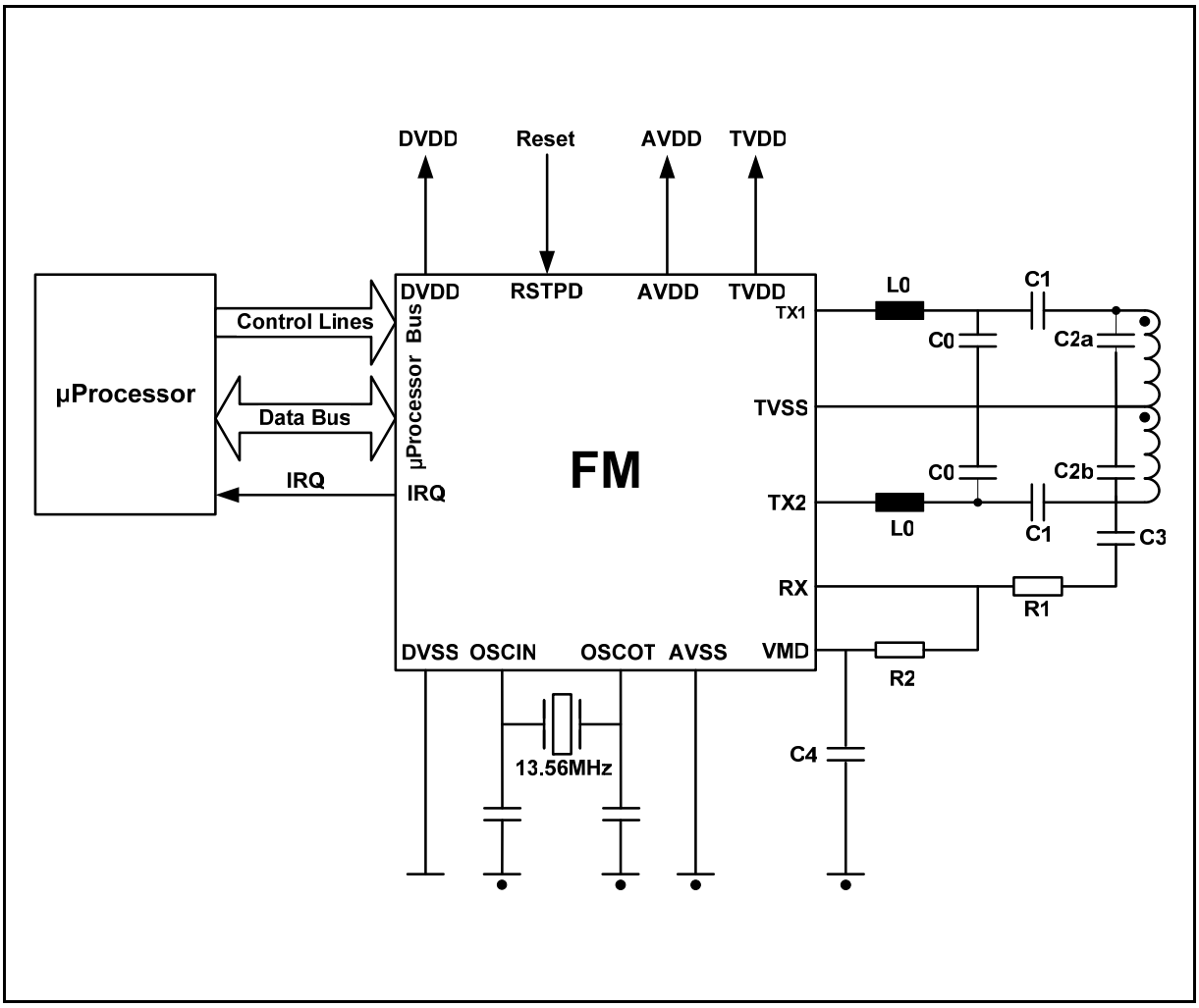


Figure 5-1 FM17XX Typical Application

6. Ordering Information

Ordering Code	HOST interface	Card interface	Encrypt Arithmetic	Package	Operation Temp.
FM1702	Parallel SPI	ISO 14443A	M1	SOP32	(-25℃ ~ 85℃)
FM1702S	SPI	ISO 14443A	M1	SOP24	
FM1702Q	SPI	ISO 14443A	M1	QFN28	
FM1702N	Parallel SPI	ISO 14443A	M1	SOP32(N)	
FM1702NL	Parallel SPI	ISO 14443A	M1	SOP32(N)	
FM1702SL	SPI	ISO 14443A	M1	SOP24	
FM1702SL/M	RS232	ISO 14443A	M1	SYS(1)	
FM1715	Parallel SPI	ISO 14443A/B	M1 SH	SOP32	
FM1715S	SPI	ISO 14443A/B	M1 SH	SOP24	
FM1715Q	SPI	ISO 14443A/B	M1 SH	QFN28	
FM1715N	Parallel SPI	ISO 14443A/B	M1 SH	SOP32(N)	
FM1715/M	RS232	ISO 14443A/B	M1 SH	SYS(1)	
FM1715NL	Parallel SPI	ISO 14443A/B	M1 SH	SOP32(N)	
FM1715SL	SPI	ISO 14443A/B	M1 SH	SOP24	
FM1725	Parallel SPI	ISO 14443A/B ISO 15693	M1 SH	SOP32	
FM1725S	SPI	ISO 14443A/B ISO 15693	M1 SH	SOP24	
FM1725Q	SPI	ISO 14443A/B ISO 15693	M1 SH	QFN28	
FM1725N	Parallel SPI	ISO 14443A/B ISO 15693	M1 SH	SOP32(N)	
FM1725NL	Parallel SPI	ISO 14443A/B ISO 15693	M1 SH	SOP32(N)	
FM1725SL	SPI	ISO 14443A/B ISO 15693	M1 SH	SOP24	

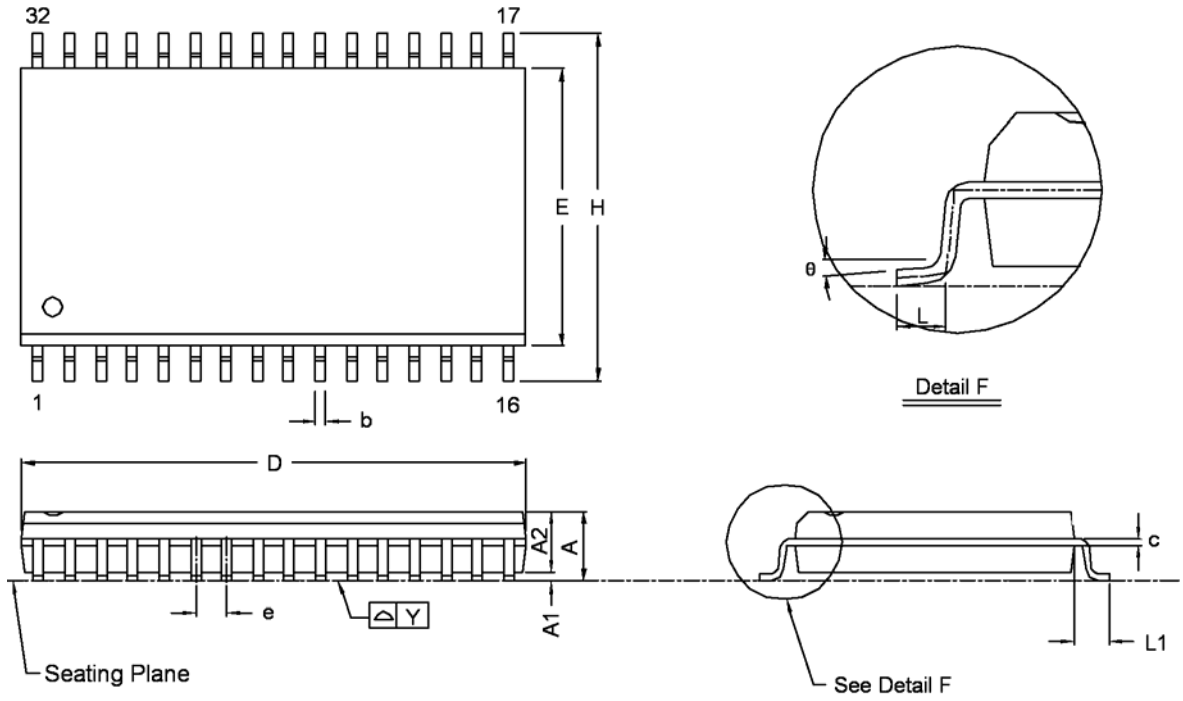
Table 6-1 FM17XX Ordering Information

Note:

1. “SYS” denotes system products.

7. Package Dimensions

7.1. 32- Pin SOP Package Dimensions

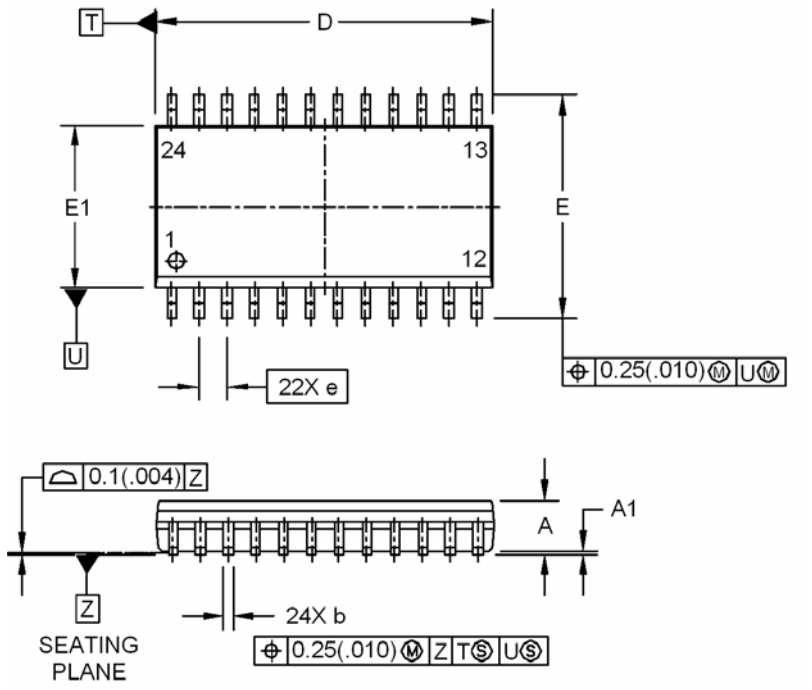


*CONTROLLING DIMENSION: MM

Symbol	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			2.997			0.118
A1	0.102			0.004		
A2	2.565	2.692	2.819	0.101	0.106	0.111
b	0.356	0.406	0.508	0.014	0.016	0.020
c	0.152	0.203	0.305	0.006	0.008	0.012
D	20.142	20.447	20.752	0.793	0.805	0.817
E	11.176	11.303	11.430	0.440	0.445	0.450
e	1.118	1.270	1.422	0.044	0.050	0.056
H	13.868	14.122	14.376	0.546	0.556	0.566
L	0.584	0.787	0.991	0.023	0.031	0.039
L1	1.194	1.397	1.600	0.047	0.055	0.063
Y			0.102			0.004
θ	0°		10°	0°		10°

Figure 7-1 FM17XX 32-Pin SOP Package Dimensions

7.2. 24- Pin SOP Package Dimensions



DIM	MILLIMETER		INCH		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	2.35	2.65	.093	.104	1. CONTROLLING DIMENSION: MILLIMETER. 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994. 3. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION. 4. DIMENSION b DOES NOT INCLUDE DAM BAR PROTRUSION. ALLOWABLE DAM BAR PROTRUSION SHALL BE 0.13(.005) TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
A1	0.13	0.29	.005	.011	
D	15.25	15.54	.601	.612	
E	10.05	10.55	.395	.415	
E1	7.40	7.60	.292	.299	
b	0.35	0.49	.014	.019	
c	0.23	0.32	.009	.013	
e	1.27 BSC		.050 BSC		
L	0.41	0.9	.016	.035	
h	0.25	0.75	.010	.029	
θ	0°	8°	0°	8°	

Figure 7-2 FM17XX 24-Pin SOP Package Dimensions

7.3. 28- Pin QFN Package Dimensions

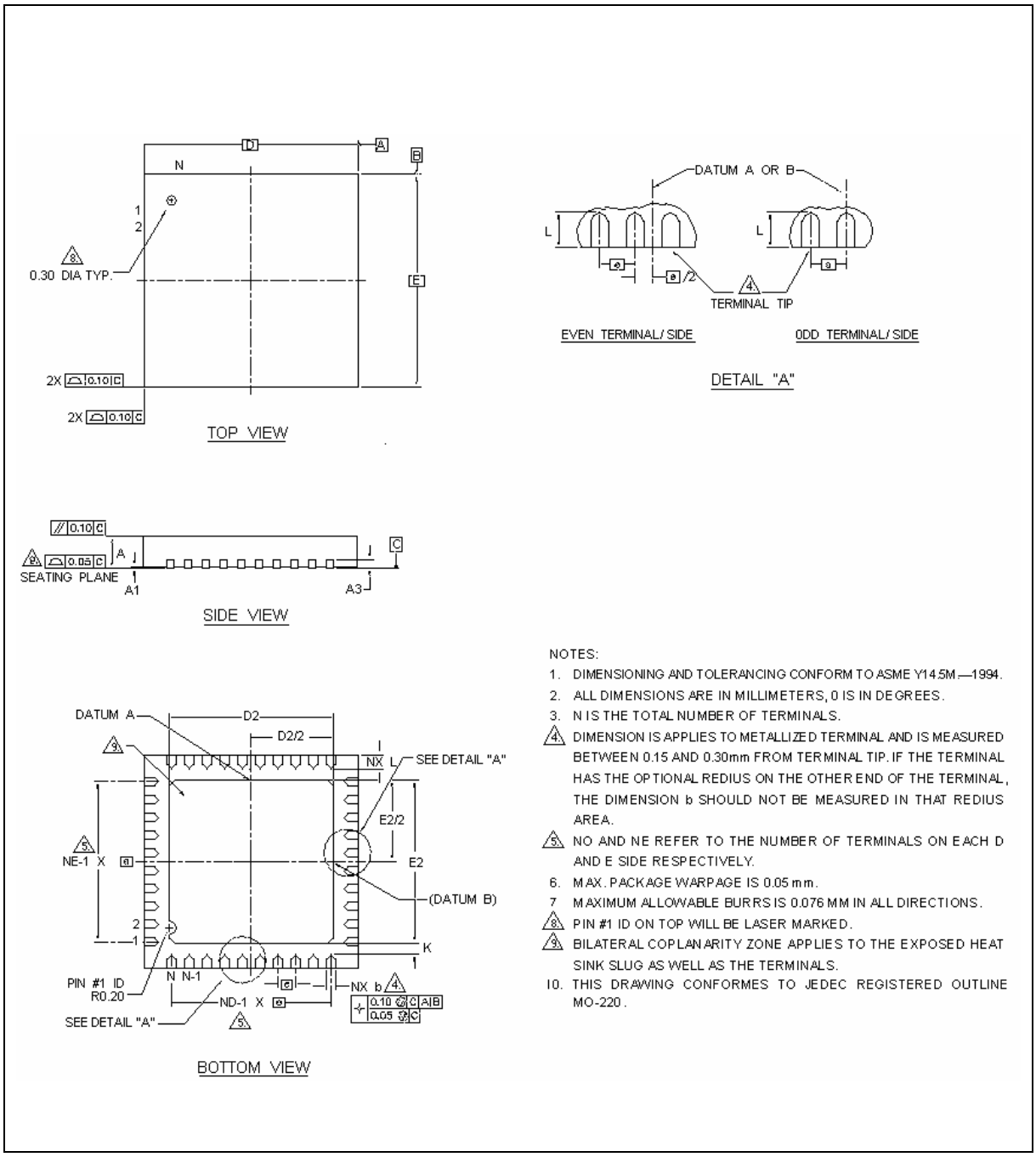


Figure 7-3 FM17XX 28-Pin QFN Package Dimensions

8. Revision History

Version	Publication date	Pages	Paragraph or Illustration	Revise Description
0.1	Mar. 2007	20		Initial Release.
0.2	Oct. 2007	20		Updated Format.
0.3	May. 2008	20	Sales and service	Updated the address of HK office.

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