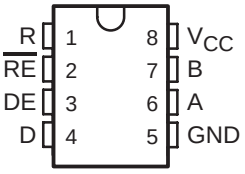
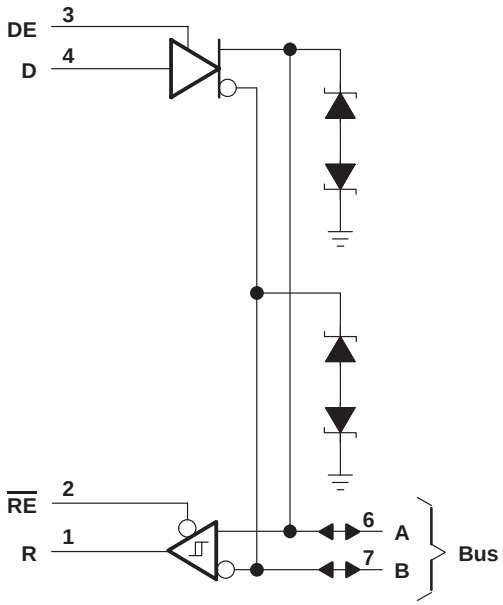
- **Integrated Transient Voltage Suppression**
- **ESD Protection for Bus Terminals Exceeds:**
  - **±30 kV IEC 61000-4-2, Contact Discharge**
  - **±15 kV IEC 61000-4-2, Air-Gap Discharge**
  - **±15 kV EIA/JEDEC Human Body Model**
- **Circuit Damage Protection of 400-W Peak (Typical) Per IEC 61000-4-5**
- **Controlled Driver Output-Voltage Slew Rates Allow Longer Cable Stub Lengths**
- **250-kbps in Electrically Noisy Environments**
- **Open-Circuit Fail-Safe Receiver Design**
- **1/4 Unit Load Allows for 128 Devices Connected on Bus**
- **Thermal Shutdown Protection**
- **Power-Up/-Down Glitch Protection**
- **Each Transceiver Meets or Exceeds the Requirements of TIA/EIA-485 (RS-485) and ISO/IEC 8482:1993(E) Standards**
- **Low Disabled Supply Current 300 μA Max**
- **Pin Compatible With SN75176**
- **Applications:**
  - **Industrial Networks**
  - **Utility Meters**
  - **Motor Control**

SN65LBC184D (Marked as 6LB184)
SN75LBC184D (Marked as 7LB184)
SN65LBC184P (Marked as 65LBC184)
SN75LBC184P (Marked as 75LBC184)
(TOP VIEW)



functional logic diagram (positive logic)



description

The SN75LBC184 and SN65LBC184 are differential data line transceivers in the trade-standard footprint of the SN75176 with built-in protection against high-energy noise transients. This feature provides a substantial increase in reliability for better immunity to noise transients coupled to the data cable over most existing devices. Use of these circuits provides a reliable low-cost direct-coupled (with no isolation transformer) data line interface without requiring any external components.

The SN75LBC184 and SN65LBC184 can withstand overvoltage transients of 400-W peak (typical). The conventional combination wave called out in IEC 61000-4-5 simulates the overvoltage transient and models a unidirectional surge caused by overvoltages from switching and secondary lightning transients.

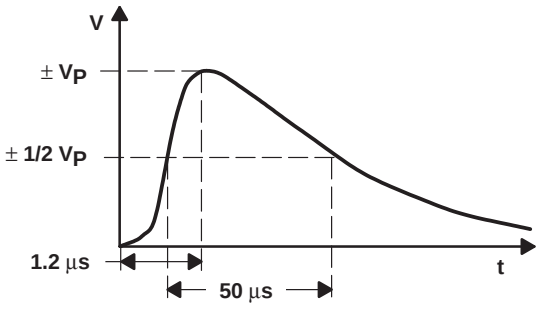


Figure 1. Surge Waveform — Combination Wave

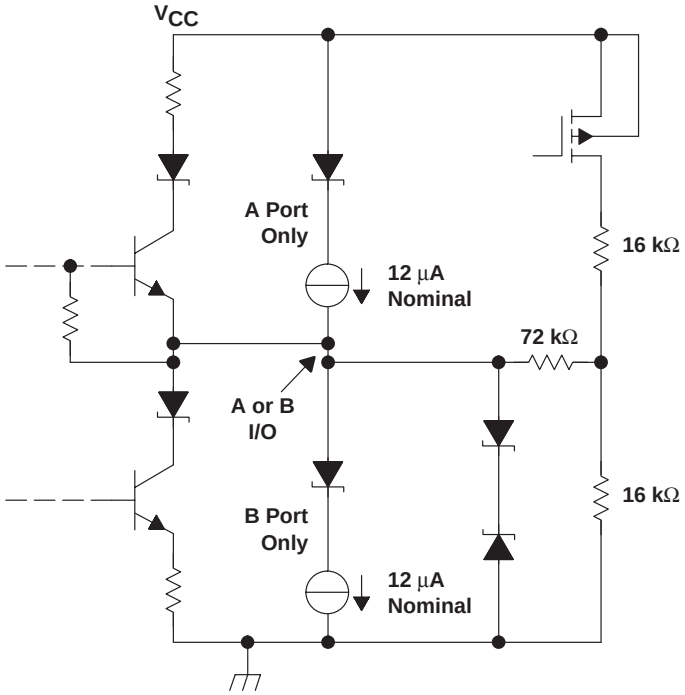
description (continued)

A biexponential function defined by separate rise and fall times for voltage and current simulates the combination wave. The standard 1.2 μs/50 μs combination waveform is shown in Figure 1 and in the test description in Figure 15.

The device also includes additional desirable features for party-line data buses in electrically noisy environment applications including industrial process control. The differential-driver design incorporates slew-rate-controlled outputs sufficient to transmit data up to 250 kbps. Slew-rate control allows longer unterminated cable runs and longer stub lengths from the main backbone than possible with uncontrolled and faster voltage transitions. A unique receiver design provides a fail-safe output of a high level when the inputs are left floating (open circuit). The SN75LBC184 and SN65LBC184 receiver also includes a high input resistance equivalent to one-fourth unit load allowing connection of up to 128 similar devices on the bus.

The SN75LBC184 is characterized for operation from 0°C to 70°C. The SN65LBC184 is characterized from −40°C to 85°C.

schematic of inputs and outputs



DRIVER FUNCTION TABLE

INPUT	ENABLE	OUTPUTS	
D	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

RECEIVER FUNCTION TABLE

DIFFERENTIAL INPUTS	ENABLE	OUTPUT
A − B	$\overline{RE}$	R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V < V_{ID} < 0.2 V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	H

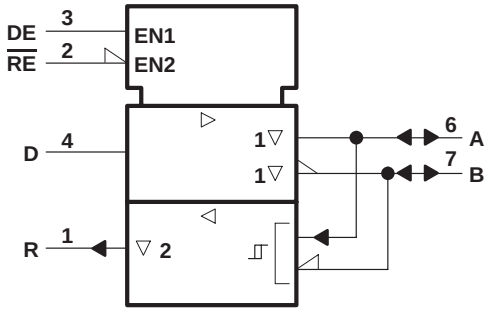
H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

AVAILABLE OPTIONS

T_A	PACKAGE	
	PLASTIC SMALL-OUTLINE† (JEDEC MS-012)	PLASTIC DUAL-IN-LINE PACKAGE (JEDEC MS-001)
0°C to 70°C	SN75LBC184D	SN75LBC184P
−40°C to 85°C	SN65LBC184D	SN65LBC184P

† Add R suffix for taped and reel.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free−air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . −0.5 V to 7 V
Continuous voltage range at any bus terminal . . . . . −15 V to 15 V
Data input/output voltage . . . . . −0.3 V to 7 V
Receiver output current, I_O . . . . . ±20 mA
Electrostatic discharge: Contact discharge (IEC61000-4-2) A, B, GND (see Note 2) . . . . . ±30 kV
Air discharge (IEC61000-4-2) A, B, GND (see Note 2) . . . . . ±15 kV
Human body model (see Note 3) A, B, GND (see Note 2) . . . . . ±15 kV
All pins . . . . . ±3 kV
All terminals (Class 3A) (see Note 2) . . . . . ±8 kV
All terminals (Class 3B) (see Note 2) . . . . . ±200 V
Electrical Fast Transient/Burst (IEC 61000−4−4) A, B, GND . . . . . ±4 kV
Continuous total power dissipation (see Note 4) . . . . . Internally Limited

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.
2. GND and bus terminal ESD protection is beyond readily available test equipment capabilities for IEC 61000-4-2, EIA/JEDEC test method A114-A and MIL-STD-883C method 3015. Ratings listed are limits of test equipment; device performance exceeds these limits.
3. Tested in accordance with JEDEC Standard 22, Test Method A114-A and IEC 60749−26.
4. The driver shuts down at a junction temperature of approximately 160°C. To operate below this temperature, see the Dissipation Rating Table.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

		MIN‡	TYP	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}		−7		12	V
High-level input voltage, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, $\lvert V_{ID} \rvert$				12	V
High-level output current, I_{OH}	Driver	−60			mA
	Receiver	−8			mA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			4	mA
Operating free-air temperature, T_A	SN75LBC184	0		70	°C
	SN65LBC184	−40		85	°C

‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet.

DRIVER SECTION

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		ALTERNATE SYMBOLS	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{CC}	Supply current	NA	DE = $\overline{RE}$ = 5 V, No Load		12	25	mA
			DE = 0 V, $\overline{RE}$ = 5 V, No Load		175	300	µA
I_{IH}	High-level input current (D, DE, $\overline{RE}$)	NA	V_I = 2.4 V			50	µA
I_{IL}	Low-level input current (D, DE, $\overline{RE}$)	NA	V_I = 0.4 V	−50			µA
I_{OS}	Short-circuit output current (see Note 5)	NA	V_O = −7 V	−250	−120		mA
			V_O = V_{CC}			250	
			V_O = 12 V			250	
I_{OZ}	High-impedance output current	NA		See Receiver I_I			mA
V_O	Output voltage	V_{oa}, V_{ob}	I_O = 0	0		V_{CC}	V
$V_{OC(PP)}$	Peak-to-peak change in common-mode output voltage during state transitions	NA	See Figures 5 and 6		0.8		V
V_{OC}	Common-mode output voltage	$\lvert V_{os}\rvert$	See Figure 4	1		3	V
$\lvert\Delta V_{OC(SS)}\rvert$	Magnitude of change, common-mode steady-state output voltage	$\lvert V_{os} - \overline{V}_{os}\rvert$	See Figure 5			0.1	V
$\lvert V_{OD}\rvert$	Magnitude of differential output voltage $\lvert V_A - V_B\rvert$	V_o	I_O = 0	1.5		6	V
			R_L = 54 Ω, See Figure 4	1.5			V
$\Delta\lvert V_{OD}\rvert$	Change in differential voltage magnitude between logic states	$\lvert\lvert V_t\rvert - \lvert\overline{V}_t\rvert\rvert$	R_L = 54 Ω			0.1	V

† All typical values are measured with T_A = 25°C and V_{CC} = 5 V.
NOTE 5: This parameter is measured with only one output being driven at a time.

switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(DH)}$	Differential output delay time, low-to-high-level output	R_L = 54 Ω, C_L = 50 pF, See Figure 5			1.3	µs
$t_{d(DL)}$	Differential-output delay time, high-to-low-level output				1.3	µs
t_{PLH}	Propagation delay time, low-to-high-level output			0.5	1.3	µs
t_{PHL}	Propagation delay time, high-to-low-level output			0.5	1.3	µs
$t_{sk(p)}$	Pulse skew ($\lvert t_{d(DH)} - t_{d(DL)}\rvert$)			75	150	ns
t_r	Rise time, single ended		0.25		1.2	µs
t_f	Fall time, single ended		0.25		1.2	µs
t_{PZH}	Output enable time to high level	R_L = 110 Ω, See Figure 2			3.5	µs
t_{PZL}	Output enable time to low level	R_L = 110 Ω, See Figure 3			3.5	µs
t_{PHZ}	Output disable time from high level	R_L = 110 Ω, See Figure 2			2	µs
t_{PLZ}	Output disable time from low level	R_L = 110 Ω, See Figure 3			2	µs

RECEIVER SECTION

electrical characteristics over recommended operating conditions (unless otherwise noted)

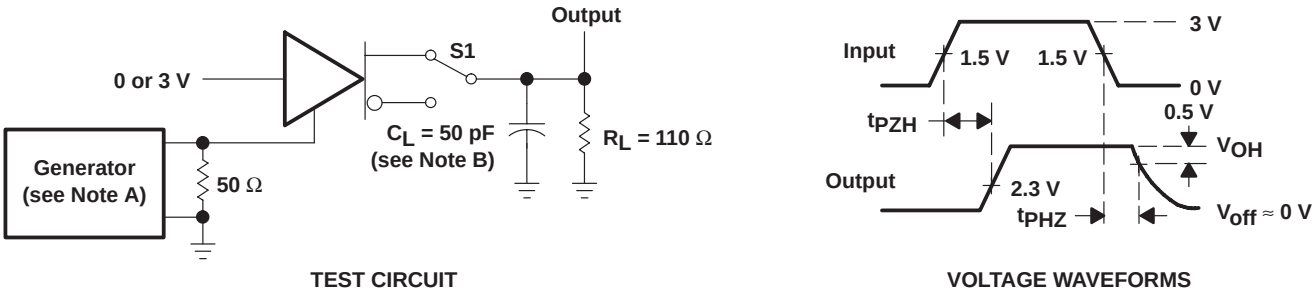
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I_{CC}	Supply current (total package)	DE = $\overline{RE}$ = 0 V, No Load				3.9	mA
		$\overline{RE}$ = 5 V, DE = 0 V, No Load				300	μA
I_I	Input current	Other input = 0 V	V_I = 12 V			250	μA
			V_I = 12 V, V_{CC} = 0			250	
			V_I = −7 V	−200			
			V_I = −7 V, V_{CC} = 0	−200			
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±100	μA
V_{hys}	Input hysteresis voltage				70		mV
V_{IT+}	Positive-going input threshold voltage					200	mV
V_{IT-}	Negative-going input threshold voltage			−200			mV
V_{OH}	High-level output voltage	I_{OH} = −8 mA	Figure 7	2.8			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA	Figure 7			0.4	V

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, See Figure 7			150	ns
t_{PHL}	Propagation delay time, high-to-low-level output				150	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{pHL} - t_{pLH} \rvert$)				50	ns
t_r	Rise time, single ended	See Figure 7		20		ns
t_f	Fall time, single ended			20		ns
t_{PZH}	Output enable time to high level	See Figure 8			100	ns
t_{PZL}	Output enable time to low level				100	ns
t_{PHZ}	Output disable time from high level				100	ns
t_{PLZ}	Output disable time from low level				100	ns

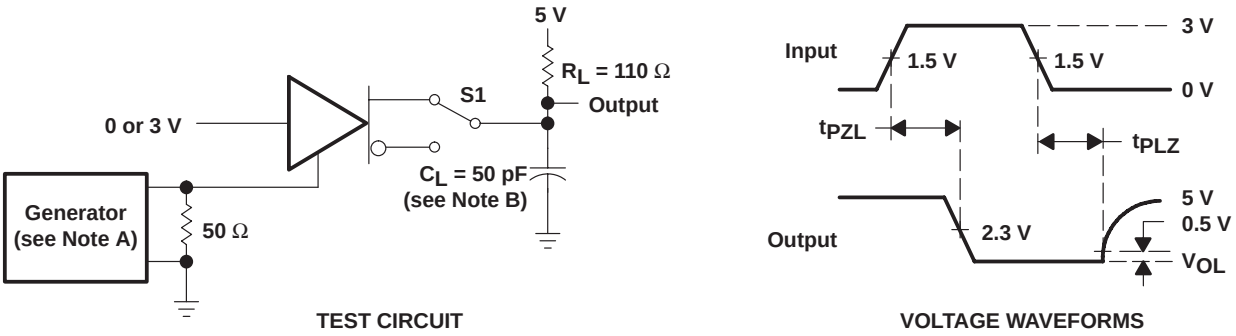
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1.25 kHz, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

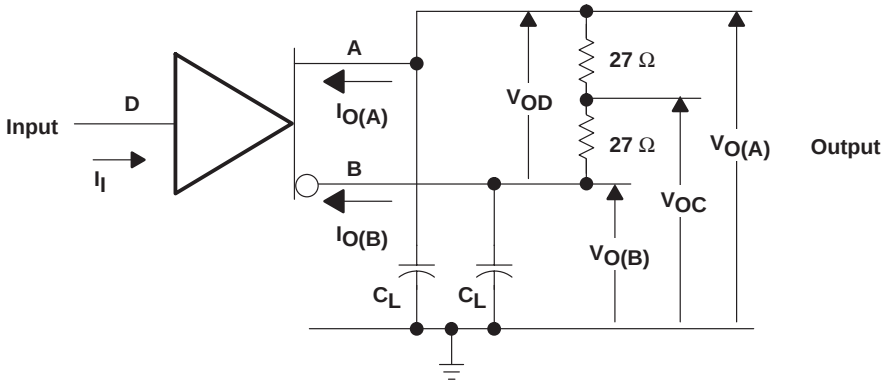
Figure 2. Driver t_{PZH} and t_{PHZ} Test Circuit and Voltage Waveforms



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1.25 kHz, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

Figure 3. Driver t_{PZL} and t_{PLZ} Test Circuit and Voltage Waveforms



NOTES: A. Resistance values are in ohms and are 1% tolerance.
B. C_L includes probe and jig capacitance.

Figure 4. Driver Test Circuit, Voltage, and Current Definitions

PARAMETER MEASUREMENT INFORMATION

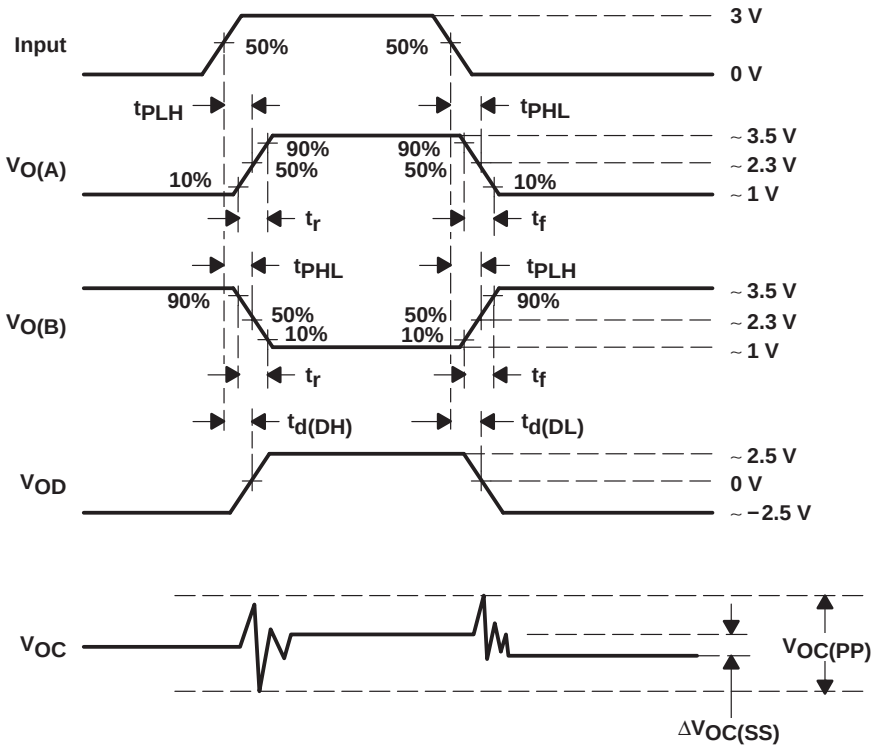
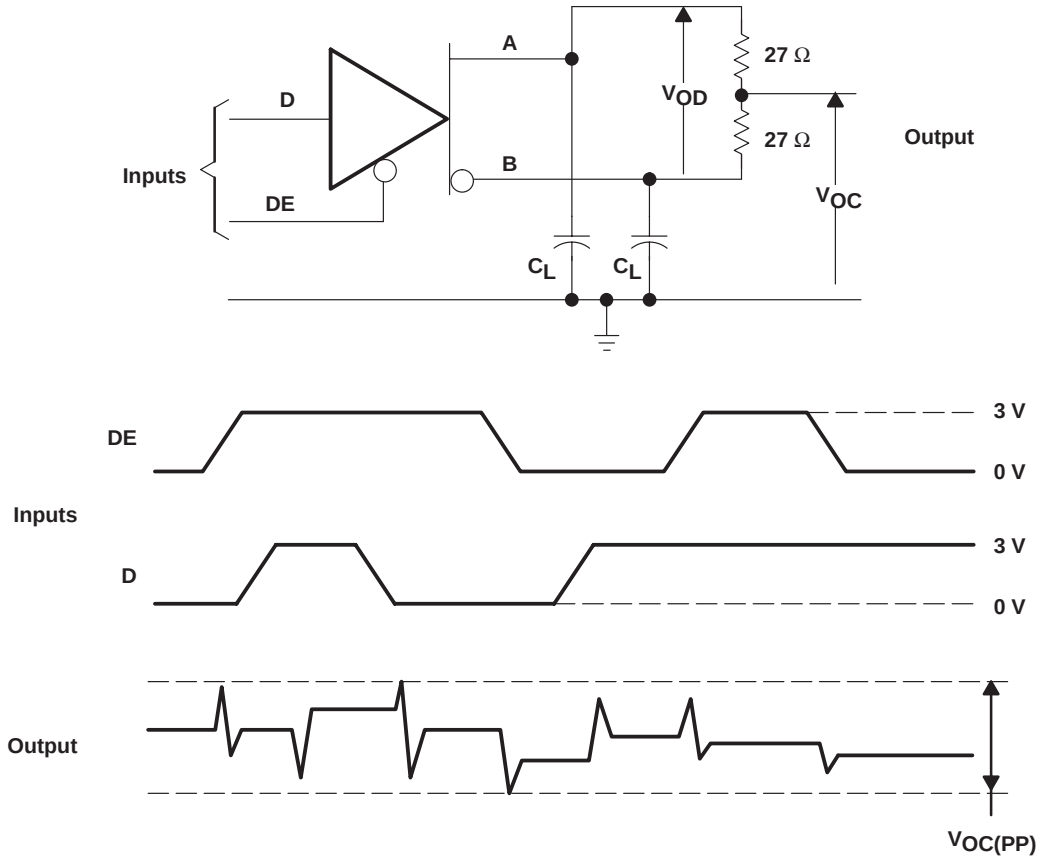


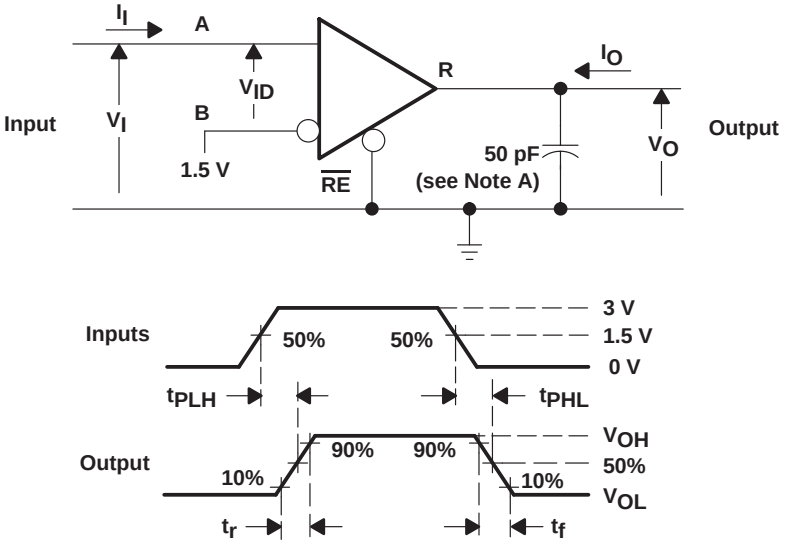
Figure 5. Driver Timing, Voltage and Current Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Resistance values are in ohms and are 1% tolerance.
B. C_L includes probe and jig capacitance (± 10%).

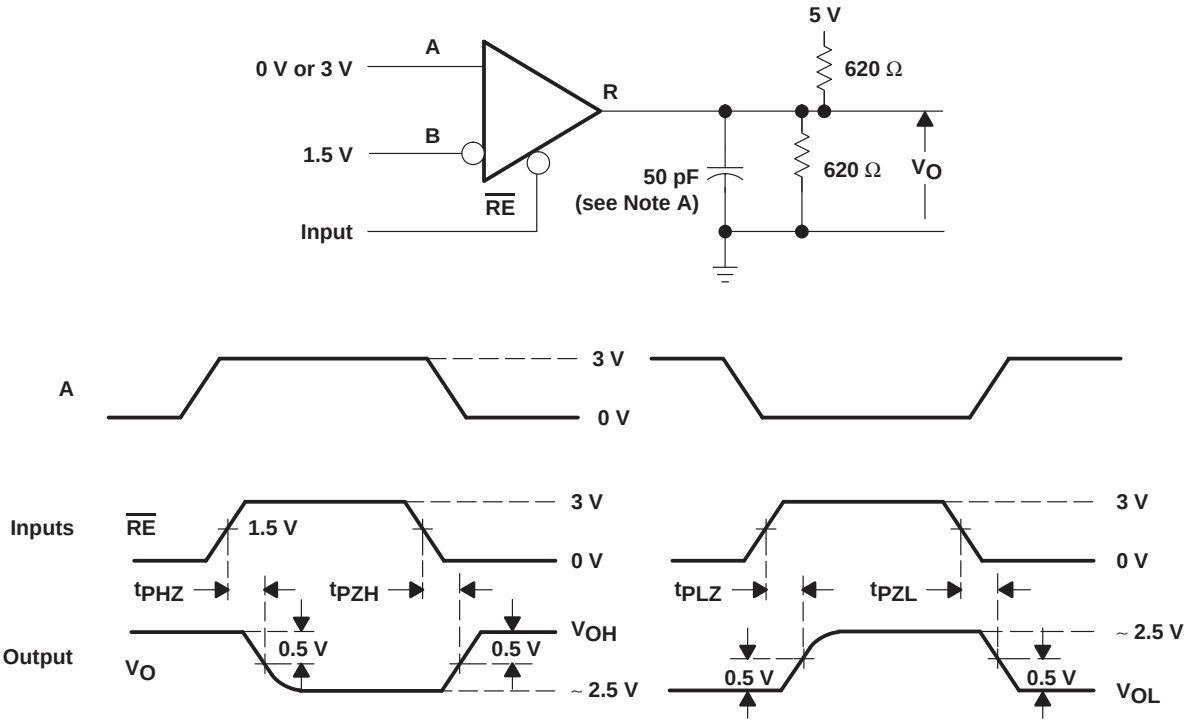
Figure 6. Driver $V_{OC(PP)}$ Test Circuit and Waveforms



NOTE A: This value includes probe and jig capacitance (± 10%).

Figure 7. Receiver t_{PLH} and t_{PHL} Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: This value includes probe and jig capacitance (± 10%).

Figure 8. Receiver t_{PZL}, t_{PLZ}, t_{PZH}, and t_{PHZ} Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

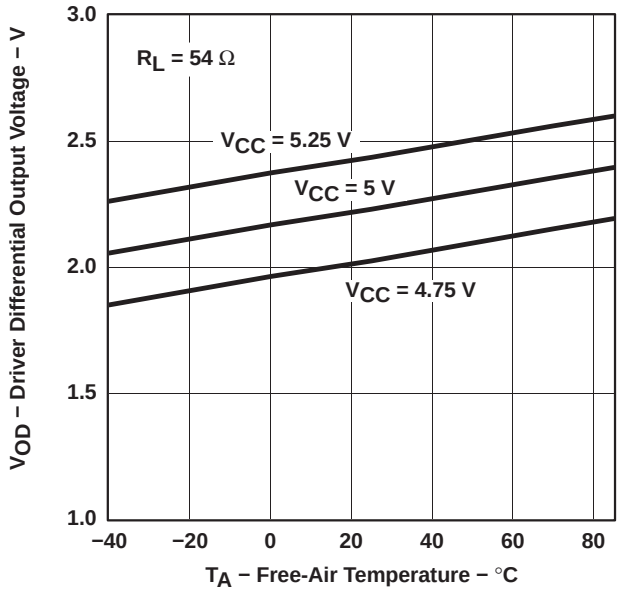


Figure 9

DRIVER PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

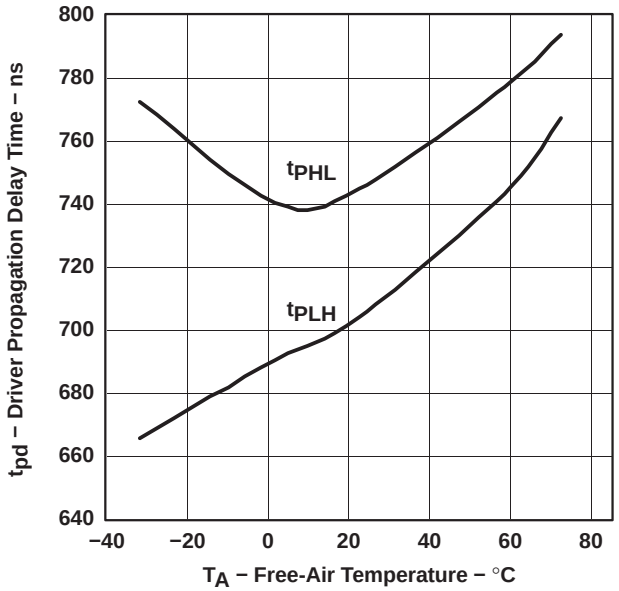


Figure 10

DRIVER TRANSITION TIME vs FREE-AIR TEMPERATURE

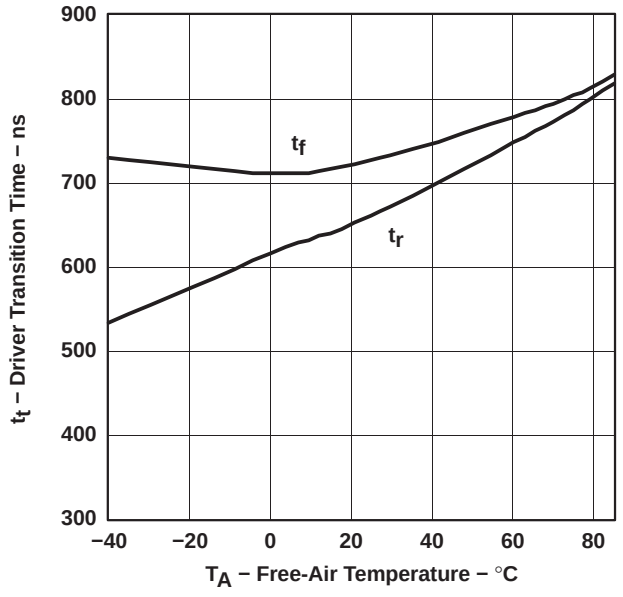


Figure 11

DIFFERENTIAL OUTPUT VOLTAGE vs OUTPUT CURRENT

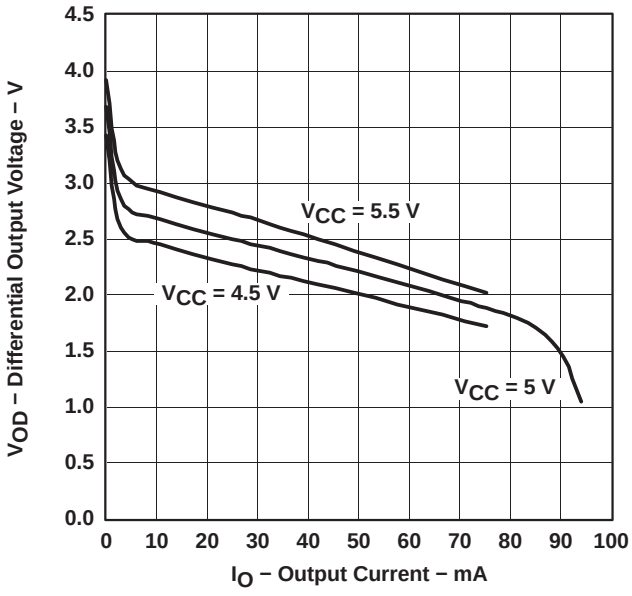


Figure 12

TYPICAL CHARACTERISTICS

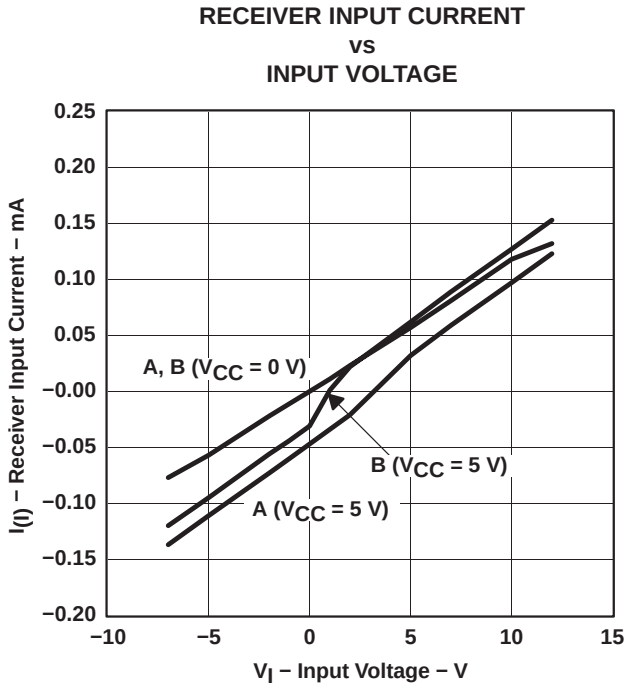
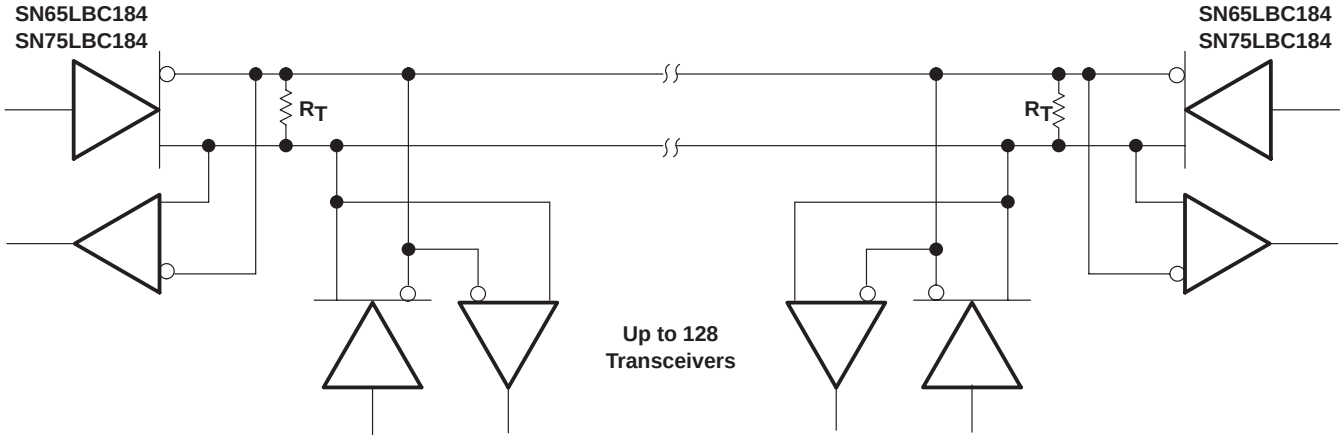


Figure 13

APPLICATION INFORMATION



NOTE A: The line should be terminated at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

Figure 14. Typical Application Circuit

APPLICATION INFORMATION

’LBC184 test description

The ’LBC184 is tested against the IEC 61000−4−5 recommended transient identified as the combination wave. The combination wave provides a 1.2-/50-μs open-circuit voltage waveform and a 8-/20-μs short-circuit current waveform shown in Figure 15. The testing is performed with a combination/hybrid pulse generator with an effective output impedance of 2 Ω. The setup for the overvoltage stress is shown in Figure 16 with all testing performed with power applied to the ’LBC184 circuit.

NOTE

High voltage transient testing is done on a sampling basis.

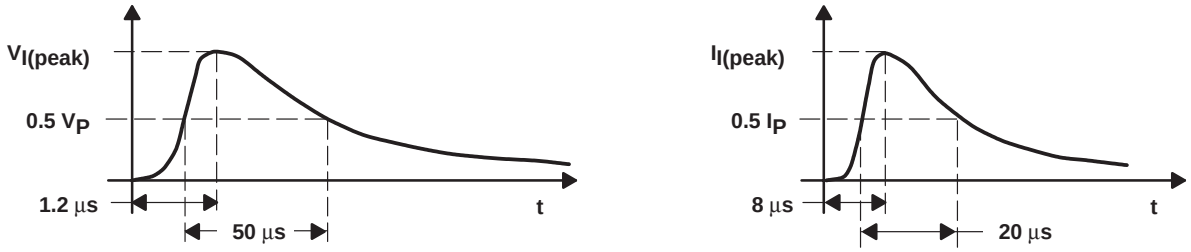


Figure 15. Short-Circuit Current Waveforms

The ’LBC184 is tested and evaluated for both maximum (single pulse) as well as life test (multiple pulse) capabilities. The ’LBC184 is evaluated against transients of both positive and negative polarity and all testing is performed with the worst-case transient polarity. Transient pulses are applied to the bus pins (A & B) across ground as shown in Figure 16.

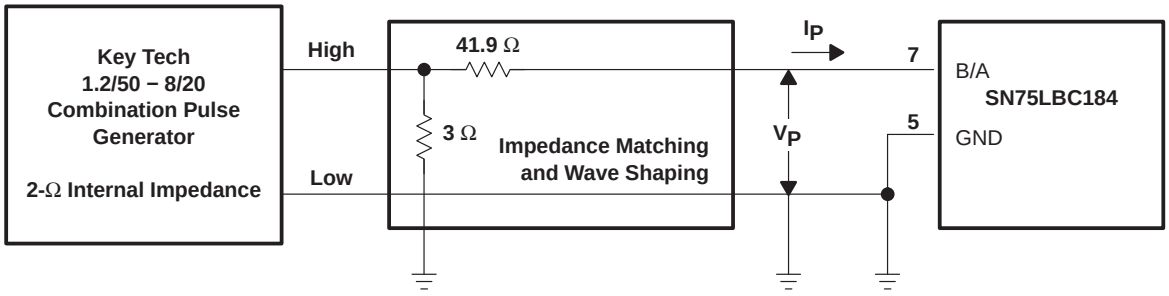


Figure 16. Overvoltage-Stress Test Circuit

An example waveform as seen by the ’LBC184 is shown in Figure 17. The bottom trace is current, the middle trace shows the clamping voltage of the device and the top trace is power as calculated from the voltage and current waveforms. This example shows a peak clamping voltage of 33.6 V and peak current of 16 A, thus yielding an absorbed peak power of 538 W.

NOTE

A circuit reset may be required to ensure normal data communications following a transient noise pulse of greater than 250 W peak.

APPLICATION INFORMATION

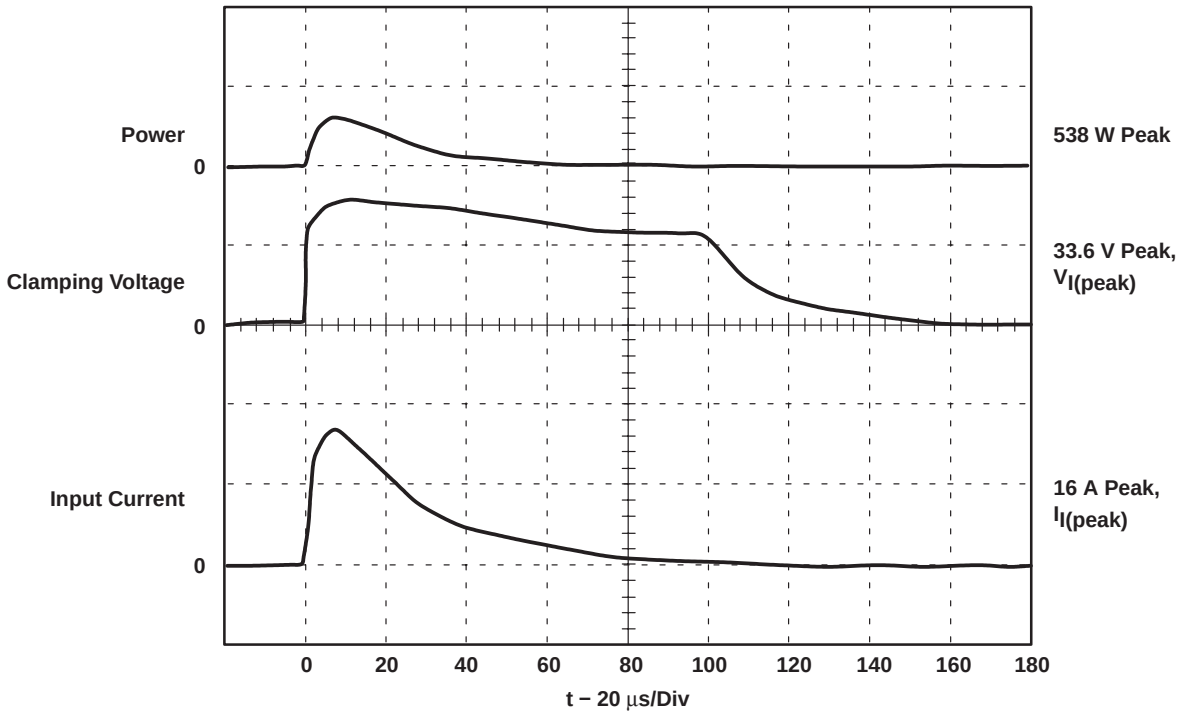


Figure 17. Typical Surge Waveform Measured At Terminals 5 and 7

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LBC184D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB184	Samples
SN65LBC184DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB184	Samples
SN65LBC184DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB184	Samples
SN65LBC184DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB184	Samples
SN65LBC184P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	65LBC184	Samples
SN65LBC184PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	65LBC184	Samples
SN75LBC184D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7LB184	Samples
SN75LBC184DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7LB184	Samples
SN75LBC184DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7LB184	Samples
SN75LBC184DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7LB184	Samples
SN75LBC184P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	75LBC184	Samples
SN75LBC184PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	75LBC184	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

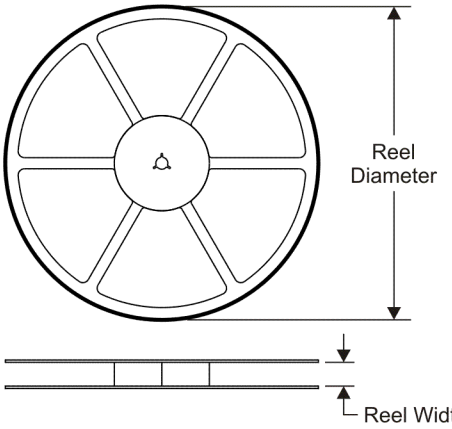
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

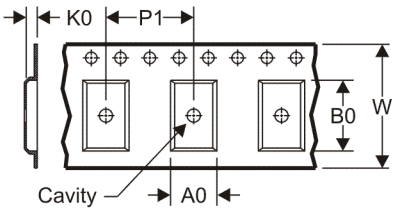
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

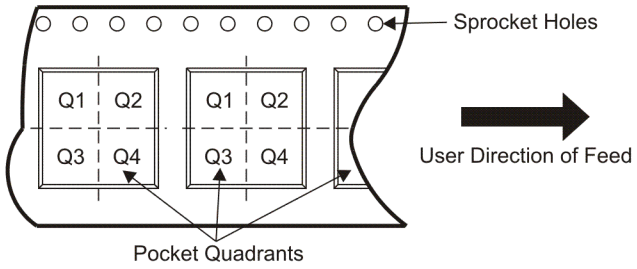


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

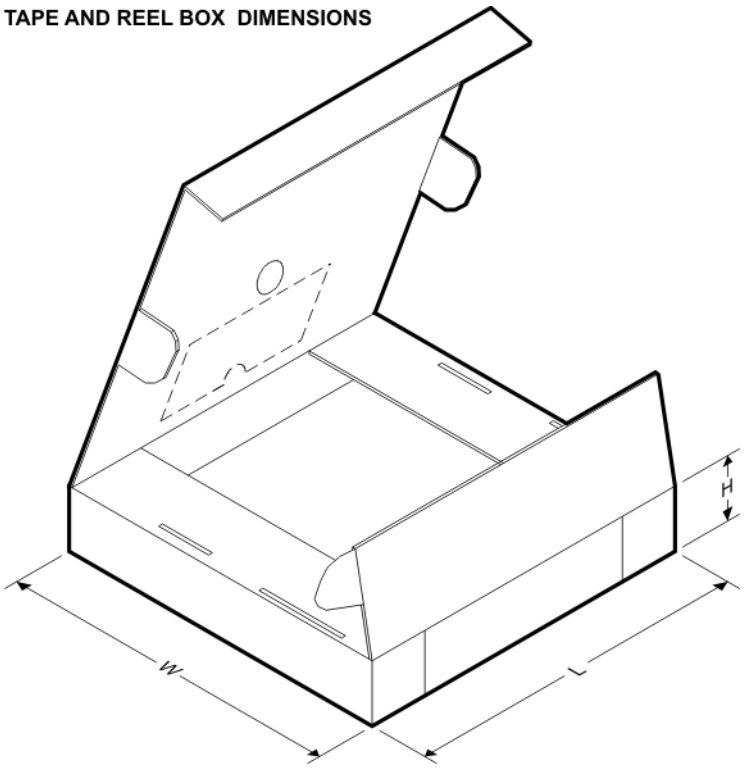
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC184DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75LBC184DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

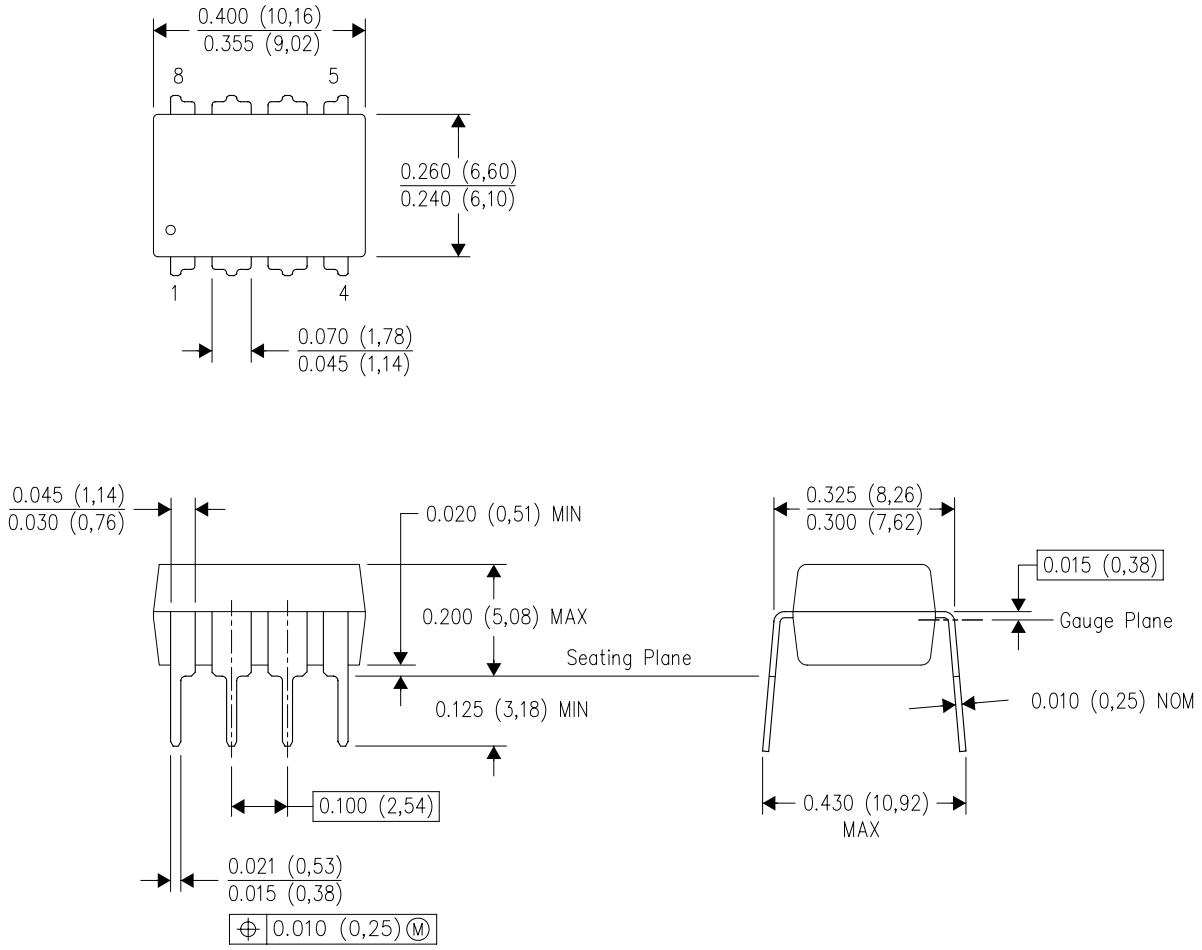
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

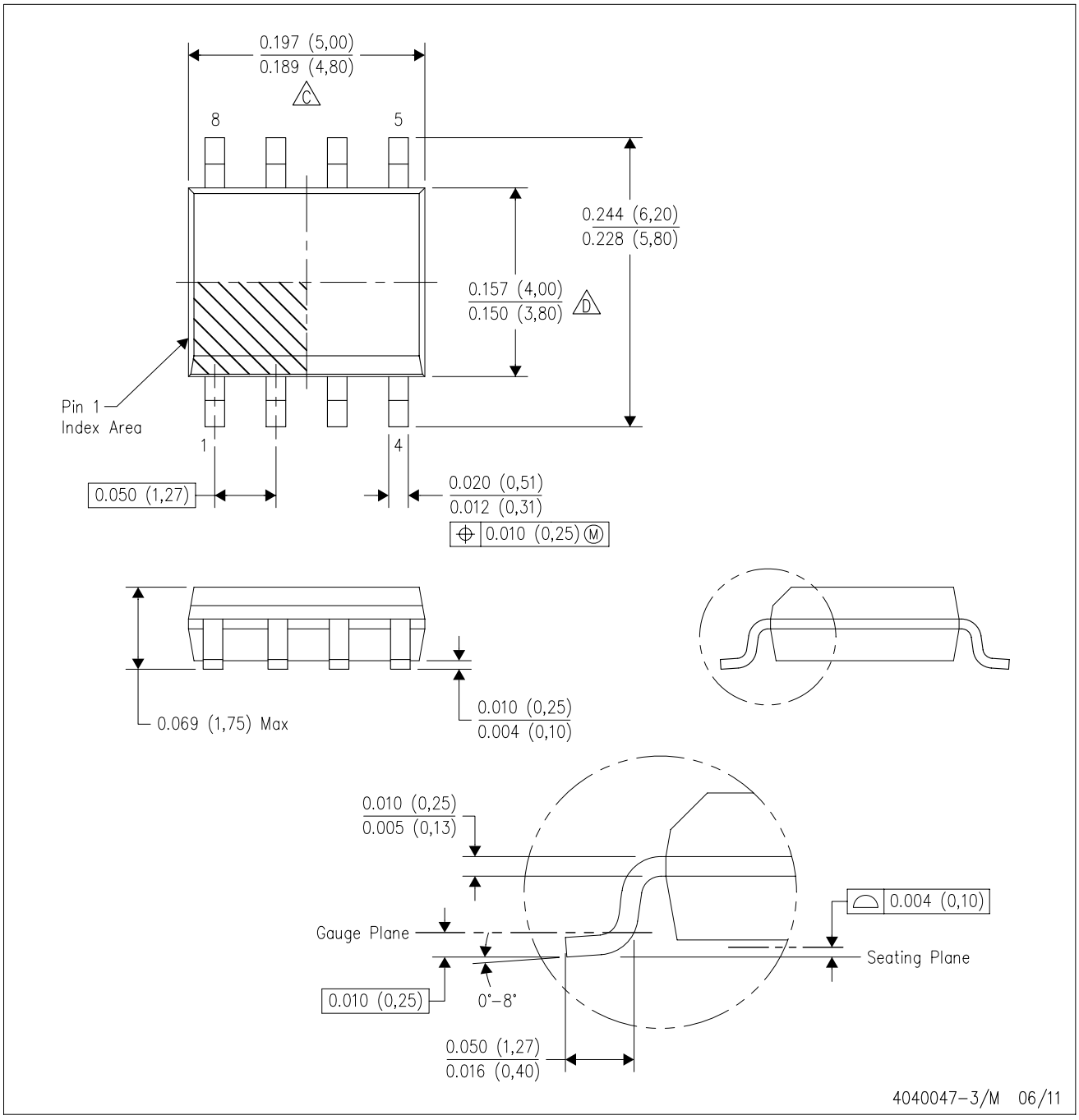
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC184DR	SOIC	D	8	2500	340.5	338.1	20.6
SN75LBC184DR	SOIC	D	8	2500	340.5	338.1	20.6

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



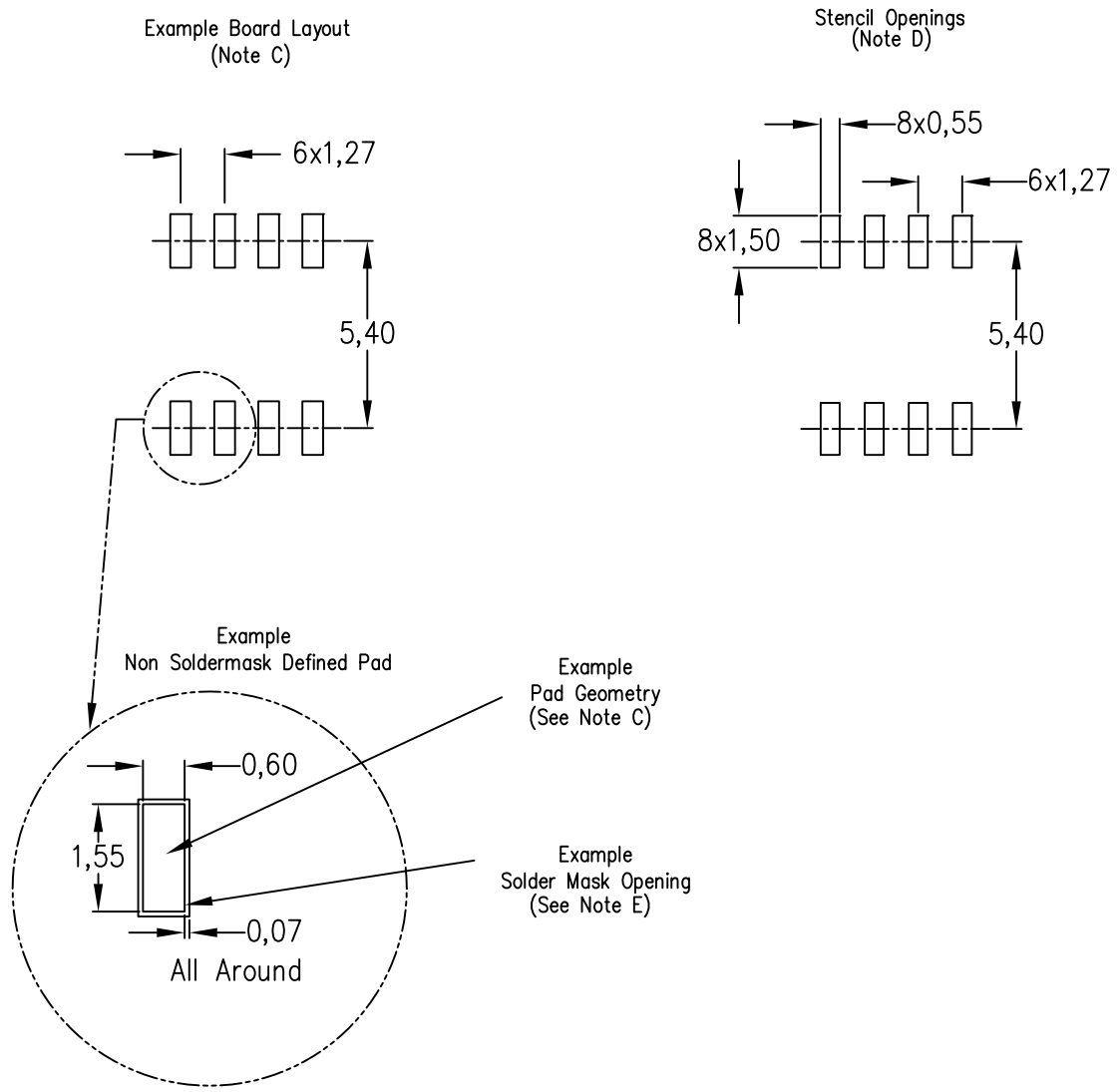
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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