# 12-Ω SPDT ANALOG SWITCH
# 5-V/3.3-V SINGLE-CHANNEL 2:1 MULTIPLEXER/DEMULTIPLEXER

## FEATURES

- **Overshoot and Undershoot Voltage Protection**
- **Isolation in Powered-Off Mode, $V_+$ = 0**
- **Specified Break-Before-Make Switching**
- **Low ON-State Resistance (12 Ω)**
- **Control Inputs Are 5-V Tolerant**
- **Low Charge Injection**
- **Excellent ON-State Resistance Matching**
- **Low Total Harmonic Distortion (THD)**
- **1.65-V to 5.5-V Single-Supply Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**

## APPLICATIONS

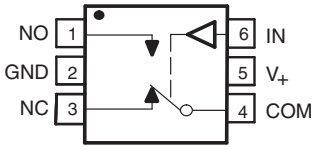
- **Sample-and-Hold Circuits**
- **Battery-Powered Equipment**
- **Audio and Video Signal Routing**
- **Communication Circuits**

## DESCRIPTION

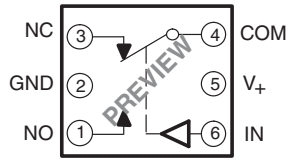
The TS5A63157 is a single-pole, double-throw (SPDT) analog switch designed to operate from 1.65 V to 5.5 V. This device can handle both digital and analog signals. Signals up to $V_+$ (peak) can be transmitted in either direction.

TI has integrated overshoot and undershoot protection circuitry. The TS5A63157 senses overshoot and undershoot events at the I/Os and responds by preventing voltage differentials from developing and turning the switch on.

**SOT-23 OR SC-70 PACKAGE**
**(TOP VIEW)**




**YEP OR YZP PACKAGE**
**(BOTTOM VIEW)**




### SUMMARY OF CHARACTERISTICS
### $V_+$ = 5 V, $T_A$ = 25°C

| | |
|---|---|
| Configuration | Single 2:1 Multiplexer/ Demultiplexer (1 × SPDT) |
| Number of channels | 1 |
| ON-state resistance ($r_{on}$) | 12 Ω |
| ON-state resistance match ($\Delta r_{on}$) | 0.15 Ω |
| ON-state resistance flatness ($r_{on(flat)}$) | 6 Ω |
| Turn-on/turn-off time ($t_{ON}/t_{OFF}$) | 5.7 ns/3.8 ns |
| Break-before-make time ($t_{BBM}$) | 0.5 ns |
| Charge injection ($Q_C$) | 7 pC |
| Bandwidth (BW) | 250 MHz |
| OFF isolation ($O_{ISO}$) | –57 dB at 10 MHz |
| Crosstalk ($X_{TALK}$) | –54 dB at 10 MHz |
| Total harmonic distortion (THD) | 0.01% |
| Leakage current ($I_{NO(OFF)}/I_{NC(OFF)}$) | ±1 μA |
| Power-supply current ($I_+$) | 10 μA |
| Undershoot protection | –2 V |
| Overshoot protection | $V_+$ + 2 V |
| Package options | 6-pin SOT-23, SC-70, and DSBGA |

### FUNCTION TABLE

| IN | NC TO COM, COM TO NC | NO TO COM, COM TO NO |
|---|---|---|
| L | ON | OFF |
| H | OFF | ON |

## ORDERING INFORMATION(1)

| $T_A$ | PACKAGE(2) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING(3) |
|---|---|---|---|---|
| –40°C to 85°C | NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP | Tape and reel | TS5A63157YEPR(4) | PREVIEW |
| | NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free) | Tape and reel | TS5A63157YZPR(4) | |
| | SOT (SOT-23) – DBV | Tape and reel | TS5A63157DBVR | JBE_ |
| | SOT (SC-70) – DCK | Tape and reel | TS5A63157DCKR | J7_ |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) DBV/DCK: The actual top-side marking has one additional character that designates the wafer faab/assembly site.
YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).
(4) Package preview

## PIN DESCRIPTION

| NO. | NAME | DESCRIPTION |
|---|---|---|
| 1 | NO | Normally open |
| 2 | GND | Digital ground |
| 3 | NC | Normally closed |
| 4 | COM | Common |
| 5 | $V_+$ | Power supply |
| 6 | IN | Digital control to connect COM to NO or NC |

## ABSOLUTE MINIMUM AND MAXIMUM RATINGS(1)(2)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_+$ | Supply voltage range(3) | | –0.5 | 6.5 | V |
| $V_{NO}$<br>$V_{NC}$<br>$V_{COM}$ | Analog voltage range(3)(4)(5) | | –0.5 | $V_+$ + 0.5 | V |
| $I_K$ | Analog port diode current | $V_{NC}$, $V_{NO}$, $V_{COM}$ < 0 or $V_{NO}$, $V_{NC}$, $V_{COM}$ > $V_+$ | –50 | 50 | mA |
| $I_{NO}$<br>$I_{NC}$<br>$I_{COM}$ | On-state switch current | $V_{NC}$, $V_{NO}$, $V_{COM}$ = 0 to $V_+$ | –50 | 50 | mA |
| $V_I$ | Digital input voltage range(3)(4) | | –0.5 | 6.5 | V |
| $I_{IK}$ | Digital input clamp current | $V_I$ < 0 | –50 | | mA |
| $I_+$ | Continuous current through $V_+$ | | –100 | 100 | mA |
| $I_{GND}$ | Continuous current through GND | | –100 | 100 | mA |
| $\theta_{JA}$ | Package thermal impedance | DBV package(6) | | 206 | °C/W |
| | | DCK package(6) | | 252 | |
| | | YEA/YZA package(6) | | 143 | |
| | | YEP/YZP package(7) | | 123 | |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 5.5 V maximum.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.
(7) The package thermal impedance is calculated in accordance with JESD 51-5.

## ELECTRICAL CHARACTERISTICS FOR 5-V SUPPLY

$V_+$ = 4.5 V to 5.5 V, $T_A$ = –40°C to 85°C (unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | | $T_A$ | $V_+$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| **Analog Switch** | | | | | | | | | |
| Analog signal range | $V_{COM}$, $V_{NO}$, $V_{NC}$ | | | | | 0 | | $V_+$ | V |
| Voltage undershoot | $V_{IKU}$ | 0 ≥ ($I_{NC}$, $I_{NO}$, or $I_{COM}$) ≥ –50 mA | | | 5.5 V | | | –2 | V |
| Peak ON-state resistance | $r_{peak}$ | 0 ≤ ($V_{NO}$ or $V_{NC}$) ≤ $V_+$, $I_{COM}$ = –30 mA, | Switch ON, See Figure 13 | 25°C | 4.5 V | | 4.6 | 11 | Ω |
| | | | | Full | | | | 13 | |
| ON-state resistance | $r_{on}$ | $V_{NO}$ or $V_{NC}$ = 0, $I_{COM}$ = 30 mA | Switch ON, See Figure 13 | 25°C | 4.5 V | | 4 | 6.5 | Ω |
| | | | | Full | | | | 8 | |
| | | $V_{NO}$ or $V_{NC}$ = 2.4 V, $I_{COM}$ = –30 mA | | 25°C | | | 4 | 8 | |
| | | | | Full | | | | 10 | |
| | | $V_{NO}$ or $V_{NC}$ = 4.5 V, $I_{COM}$ = –30 mA | | 25°C | | | 5.5 | 10 | |
| | | | | Full | | | | 12 | |
| ON-state resistance match between channels | $\Delta r_{on}$ | $V_{NO}$ or $V_{NC}$ = 3.15 V, $I_{COM}$ = –30 mA, | Switch ON, See Figure 13 | 25°C | 4.5 V | | 0.1 | 0.14 | Ω |
| | | | | Full | | | | 0.15 | |
| ON-state resistance flatness | $r_{on(flat)}$ | 0 ≤ ($V_{NO}$ or $V_{NC}$) ≤ $V_+$, $I_{COM}$ = –30 mA, | Switch ON, See Figure 13 | 25°C | 4.5 V | | 1.5 | 2 | Ω |
| | | | | Full | | | | 4 | |
| NC, NO OFF leakage current | $I_{NC(OFF)}$, $I_{NO(OFF)}$ | $V_{NC}$ or $V_{NO}$ = 0 to $V_+$, $V_{COM}$ = $V_+$ to 0 | Switch OFF, See Figure 14 | 25°C | 5.5 V | | 0.001 | 0.03 | µA |
| | | | | Full | | | | 0.05 | |
| | $I_{NC(PWROFF)}$, $I_{NOPWROFF)}$ | $V_{NC}$ or $V_{NO}$ = 0 to 5.5 V, $V_{COM}$ = 5.5 V to 0, | Switch OFF, See Figure 14 | 25°C | 0 | | 0.15 | 1 | |
| | | | | Full | | | | 5 | |
| COM OFF leakage current | $I_{COM(PWROFF)}$ | $V_{COM}$ = 0 to 5.5 V, $V_{NC}$ or $V_{NO}$ = 5.5 V to 0, | Switch ON, See Figure 14 | 25°C | 0 | | 0.2 | 1 | µA |
| | | | | Full | | | | 10 | |
| NC, NO ON leakage current | $I_{NC(ON)}$, $I_{NO(ON)}$ | $V_{NC}$ or $V_{NO}$ = 0 to $V_+$, $V_{COM}$ = Open, | Switch ON, See Figure 15 | 25°C | 5.5 V | | 0.001 | 0.01 | µA |
| | | | | Full | | | | 0.02 | |
| COM ON leakage current | $I_{COM(ON)}$ | $V_{NC}$ or $V_{NO}$ = Open, $V_{COM}$ = 0 to $V_+$, | Switch ON, See Figure 15 | 25°C | 5.5 V | | 0.003 | 0.03 | µA |
| | | | | Full | | | | 0.05 | |
| **Digital Control Input (IN)** | | | | | | | | | |
| Input logic high | $V_{IH}$ | | | Full | | $V_+$ × 0.7 | | 5.5 | V |
| Input logic low | $V_{IL}$ | | | Full | | 0 | | $V_+$ × 0.3 | V |
| Input leakage current | $I_{IH}$, $I_{IL}$ | $V_I$ = 5.5 V or 0 | | 25°C | 5.5 V | | 0.05 | 0.1 | µA |
| | | | | Full | | | | 0.02 | |

## ELECTRICAL CHARACTERISTICS FOR 5-V SUPPLY (continued)

$V_+$ = 4.5 V to 5.5 V, $T_A$ = –40°C to 85°C (unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | | $T_A$ | $V_+$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| **Dynamic** | | | | | | | | | |
| Turn-on time | $t_{ON}$ | $V_{COM}$ = $V_+$ or GND, $R_L$ = 500 Ω, | $C_L$ = 50 pF, See Figure 17 | 25°C | 5 V | 2 | 3.4 | 5 | ns |
| | | | | Full | 4.5 V to 5.5 V | 2 | | 5.5 | |
| Turn-off time | $t_{OFF}$ | $V_{COM}$ = $V_+$ or GND, $R_L$ = 500 Ω, | $C_L$ = 50 pF, See Figure 17 | 25°C | 5 V | 1 | 2.8 | 3.4 | ns |
| | | | | Full | 4.5 V to 5.5 V | 1 | | 3.8 | |
| Output voltage during undershoot | $V_{OUTU}$ | See Figure 18 | | | | 2.5 | $V_{OH}$ – 0.3 | | V |
| Output voltage during overshoot | $V_{OUTO}$ | See Figure 18 | | | | | $V_{OL}$ + 0.3 | 2 | V |
| Break-before-make time | $t_{BBM}$ | $V_{NC}$ = $V_{NO}$ = $V_+$/2, $R_L$ = 50 Ω, | $C_L$ = 50 pF, See Figure 19 | 25°C | 5 V | 0.5 | 5 | 12 | ns |
| | | | | Full | 4.5 V to 5.5 V | 0.5 | | 14 | |
| Charge injection | $Q_C$ | $V_{GEN}$ = 0, $R_{GEN}$ = 0, | $C_L$ = 0.1 nF, See Figure 23 | 25°C | 5 V | | –21 | | pC |
| NC, NO OFF capacitance | $C_{NC(OFF)}$, $C_{NO(OFF)}$ | $V_{NC}$ or $V_{NO}$ = $V_+$ or GND, Switch OFF, | See Figure 16 | 25°C | 5 V | | 5 | | pF |
| NC, NO ON capacitance | $C_{NC(ON)}$, $C_{NO(ON)}$ | $V_{NC}$ or $V_{NO}$ = $V_+$ or GND, Switch ON, | See Figure 16 | 25°C | 5 V | | 14.5 | | pF |
| COM ON capacitance | $C_{COM(ON)}$ | $V_{COM}$ = $V_+$ or GND, Switch ON, | See Figure 16 | 25°C | 5 V | | 14.5 | | pF |
| Digital input capacitance | $C_I$ | $V_I$ = $V_+$ or GND, | See Figure 16 | 25°C | 5 V | | 2.5 | | pF |
| Bandwidth | BW | $R_L$ = 50 Ω, Switch ON, | See Figure 20 | 25°C | 5 V | | 371 | | MHz |
| OFF isolation | $O_{ISO}$ | $R_L$ = 50 Ω, f = 10 MHz, | Switch OFF, See Figure 21 | 25°C | 5 V | | –61 | | dB |
| Crosstalk | $X_{TALK}$ | $R_L$ = 50 Ω, f = 10 MHz, | Switch ON, See Figure 22 | 25°C | 5 V | | –61 | | dB |
| Total harmonic distortion | THD | $R_L$ = 600 Ω, $C_L$ = 50 pF, | f = 20 Hz to 20 kHz, See Figure 24 | 25°C | 5 V | | 0.06 | | % |
| **Supply** | | | | | | | | | |
| Positive supply current | $I_+$ | $V_I$ = $V_+$ or GND, | Switch ON or OFF | 25°C | 5.5 V | | 0.01 | 0.1 | µA |
| | | | | Full | | | | 0.75 | |

## ELECTRICAL CHARACTERISTICS FOR 3.3-V SUPPLY

$V_+$ = 3 V to 3.6 V, $T_A$ = –40°C to 85°C (unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | | $T_A$ | $V_+$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| **Analog Switch** | | | | | | | | | |
| Analog signal range | $V_{COM}$, $V_{NO}$, $V_{NC}$ | | | | | 0 | | $V_+$ | V |
| Voltage undershoot | $V_{IKU}$ | 0 ≥ ($I_{NC}$, $I_{NO}$, or $I_{COM}$) ≥ –50 mA | | | 3.6 V | | | | V |
| Peak ON-state resistance | $r_{peak}$ | 0 ≤ ($V_{NO}$ or $V_{NC}$) ≤ $V_+$, $I_{COM}$ = –24 mA, | Switch ON, See Figure 13 | 25°C | 3 V | | 6.4 | 14 | Ω |
| | | | | Full | | | | 18 | |
| ON-state resistance | $r_{on}$ | $V_{NO}$ or $V_{NC}$ = 0, $I_{COM}$ = 24 mA | Switch ON, See Figure 13 | 25°C | 3 V | | 4.8 | 8 | Ω |
| | | | | Full | | | | 10 | |
| | | $V_{NO}$ or $V_{NC}$ = 3 V, $I_{COM}$ = –24 mA | | 25°C | | | 6.3 | 12 | |
| | | | | Full | | | | 15 | |
| ON-state resistance match between channels | $\Delta r_{on}$ | $V_{NO}$ or $V_{NC}$ = 2.1 V, $I_{COM}$ = –24 mA, | Switch ON, See Figure 13 | 25°C | 3 V | | 0.1 | 0.2 | Ω |
| | | | | Full | | | | 0.2 | |
| ON-state resistance flatness | $r_{on(flat)}$ | 0 ≤ ($V_{NO}$ or $V_{NC}$) ≤ $V_+$, $I_{COM}$ = –24 mA, | Switch ON, See Figure 13 | 25°C | 3 V | | 2.8 | 4 | Ω |
| | | | | Full | | | | 7 | |
| NC, NO OFF leakage current | $I_{NC(OFF)}$, $I_{NO(OFF)}$ | $V_{NC}$ or $V_{NO}$ = 0 to $V_+$, $V_{COM}$ = $V_+$ to 0 | Switch OFF, See Figure 14 | 25°C | 3.6 V | | 0 | 0.03 | µA |
| | | | | Full | | | | 0.05 | |
| | $I_{NC(PWROFF)}$, $I_{NOPWROFF)}$ | $V_{NC}$ or $V_{NO}$ = 0 to 3.6 V, $V_{COM}$ = 3.6 V to 0, | Switch OFF, See Figure 14 | 25°C | 0 | | 0.15 | 0.50 | |
| | | | | Full | | | | 2 | |
| COM OFF leakage current | $I_{COM(PWROFF)}$ | $V_{COM}$ = 0 to 3.6 V, $V_{NC}$ or $V_{NO}$ = 3.6 V to 0, | Switch ON, See Figure 14 | 25°C | 0 | | 0.2 | 0.5 | µA |
| | | | | Full | | | | 5 | |
| NC, NO ON leakage current | $I_{NC(ON)}$, $I_{NO(ON)}$ | $V_{NC}$ or $V_{NO}$ = 0 to $V_+$, $V_{COM}$ = Open, | Switch ON, See Figure 15 | 25°C | 3.6 V | | 0.001 | 0.01 | µA |
| | | | | Full | | | | 0.02 | |
| COM ON leakage current | $I_{COM(ON)}$ | $V_{NC}$ or $V_{NO}$ = Open, $V_{COM}$ = 0 to $V_+$, | Switch ON, See Figure 15 | 25°C | 3.6 V | | 0.003 | 0.03 | µA |
| | | | | Full | | | | 0.05 | |
| **Digital Control Input (IN)** | | | | | | | | | |
| Input logic high | $V_{IH}$ | | | Full | | $V_+$ × 0.7 | | 5.5 | V |
| Input logic low | $V_{IL}$ | | | Full | | 0 | | $V_+$ × 0.3 | V |
| Input leakage current | $I_{IH}$, $I_{IL}$ | $V_I$ = 5.5 V or 0 | | 25°C | 3.6 V | | 0.005 | 0.01 | µA |
| | | | | Full | | | | 0.02 | |

## ELECTRICAL CHARACTERISTICS FOR 3.3-V SUPPLY (continued)

$V_+$ = 3 V to 3.6 V, $T_A$ = –40°C to 85°C (unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | | $T_A$ | $V_+$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| **Dynamic** | | | | | | | | | |
| Turn-on time | $t_{ON}$ | $V_{COM}$ = $V_+$ or GND, $R_L$ = 500 Ω, | $C_L$ = 50 pF, See Figure 17 | 25°C | 3.3 V | 2 | 4.3 | 6.6 | ns |
| | | | | Full | 3 V to 3.6 V | 2 | | 7 | |
| Turn-off time | $t_{OFF}$ | $V_{COM}$ = $V_+$ or GND, $R_L$ = 500 Ω, | $C_L$ = 50 pF, See Figure 17 | 25°C | 3.3 V | 1 | 3.3 | 6.3 | ns |
| | | | | Full | 3 V to 3.6 V | 1 | | 7 | |
| Output voltage during undershoot | $V_{OUTU}$ | See Figure 18 | | | | 2.5 | $V_{OH}$ – 0.3 | | V |
| Output voltage during overshoot | $V_{OUTO}$ | See Figure 18 | | | | | $V_{OL}$ + 0.3 | 2 | V |
| Break-before-make time | $t_{BBM}$ | $V_{NC}$ = $V_{NO}$ = $V_+$/2, $R_L$ = 50 Ω, | $C_L$ = 50 pF, See Figure 19 | 25°C | 3.3 V | 0.5 | 7 | 17 | ns |
| | | | | Full | 3 V to 3.6 V | 0.5 | | 19.5 | |
| Charge injection | $Q_C$ | $V_{GEN}$ = 0, $R_{GEN}$ = 0, | $C_L$ = 0.1 nF, See Figure 23 | 25°C | 3.3 V | | –11.5 | | pC |
| NC, NO OFF capacitance | $C_{NC(OFF)}$, $C_{NO(OFF)}$ | $V_{NC}$ or $V_{NO}$ = $V_+$ or GND, Switch OFF, | See Figure 16 | 25°C | 3.3 V | | 5 | | pF |
| NC, NO ON capacitance | $C_{NC(ON)}$, $C_{NO(ON)}$ | $V_{NC}$ or $V_{NO}$ = $V_+$ or GND, Switch ON, | See Figure 16 | 25°C | 3.3 V | | 15 | | pF |
| COM ON capacitance | $C_{COM(ON)}$ | $V_{COM}$ = $V_+$ or GND, Switch ON, | See Figure 16 | 25°C | 3.3 V | | 15 | | pF |
| Digital input capacitance | $C_I$ | $V_I$ = $V_+$ or GND, | See Figure 16 | 25°C | 3.3 V | | 2.5 | | pF |
| Bandwidth | BW | $R_L$ = 50 Ω, Switch ON, | See Figure 20 | 25°C | 3.3 V | | 370 | | MHz |
| OFF isolation | $O_{ISO}$ | $R_L$ = 50 Ω, f = 10 MHz, | Switch OFF, See Figure 21 | 25°C | 3.3 V | | –60 | | dB |
| Crosstalk | $X_{TALK}$ | $R_L$ = 50 Ω, f = 10 MHz, | Switch ON, See Figure 22 | 25°C | 3.3 V | | –60 | | dB |
| Total harmonic distortion | THD | $R_L$ = 600 Ω, $C_L$ = 50 pF, | f = 20 Hz to 20 kHz, See Figure 24 | 25°C | 3.3 V | | 0.1 | | % |
| **Supply** | | | | | | | | | |
| Positive supply current | $I_+$ | $V_I$ = $V_+$ or GND, | Switch ON or OFF | 25°C | 3.6 V | | 0.05 | 0.1 | µA |
| | | | | Full | | | | 0.6 | |

## ELECTRICAL CHARACTERISTICS FOR 2.5-V SUPPLY

$V_+$ = 2.3 V to 2.7 V, $T_A$ = –40°C to 85°C (unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | | $T_A$ | $V_+$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| **Analog Switch** | | | | | | | | | |
| Analog signal range | $V_{COM}$, $V_{NO}$, $V_{NC}$ | | | | | 0 | | $V_+$ | V |
| Voltage undershoot | $V_{IKU}$ | 0 mA ≥ ($I_{NC}$, $I_{NO}$, or $I_{COM}$) ≥ –50 mA | | | 2.7 V | | | | V |
| Peak ON-state resistance | $r_{peak}$ | 0 ≤ ($V_{NO}$ or $V_{NC}$) ≤ $V_+$, $I_{COM}$ = –8 mA, | Switch ON, See Figure 13 | 25°C | 2.3 V | | 9.2 | 30 | Ω |
| | | | | Full | | | | 35 | |
| ON-state resistance | $r_{on}$ | $V_{NO}$ or $V_{NC}$ = 0, $I_{COM}$ = 8 mA | Switch ON, See Figure 13 | 25°C | 2.3 V | | 5.4 | 8.5 | Ω |
| | | | | Full | | | | 12 | |
| | | $V_{NO}$ or $V_{NC}$ = 2.3 V, $I_{COM}$ = –8 mA | | 25°C | | | 8.6 | 15.5 | |
| | | | | Full | | | | 25 | |
| ON-state resistance match between channels | $\Delta r_{on}$ | $V_{NO}$ or $V_{NC}$ = 1.6 V, $I_{COM}$ = –8 mA, | Switch ON, See Figure 13 | 25°C | 2.3 V | | 0.05 | 0.3 | Ω |
| | | | | Full | | | | 0.5 | |
| ON-state resistance flatness | $r_{on(flat)}$ | 0 ≤ ($V_{NO}$ or $V_{NC}$) ≤ $V_+$, $I_{COM}$ = –8 mA, | Switch ON, See Figure 13 | 25°C | 2.3 V | | 5 | 9 | Ω |
| | | | | Full | | | | 15 | |
| NC, NO OFF leakage current | $I_{NC(OFF)}$, $I_{NO(OFF)}$ | $V_{NC}$ or $V_{NO}$ = 0 to $V_+$, $V_{COM}$ = $V_+$ to 0, | Switch OFF, See Figure 14 | 25°C | 2.7 V | | 0 | 0.03 | µA |
| | | | | Full | | | | 0.05 | |
| | $I_{NC(PWROFF)}$, $I_{NOPWROFF)}$ | $V_{NC}$ or $V_{NO}$ = 0 to 2.7 V, $V_{COM}$ = 2.7 V to 0, | Switch OFF, See Figure 14 | 25°C | 0 | | 0.15 | 0.50 | |
| | | | | Full | | | | 0.75 | |
| COM OFF leakage current | $I_{COM(PWROFF)}$ | $V_{COM}$ = 0 to 2.7 V, $V_{NC}$ or $V_{NO}$ = 2.7 V to 0, | Switch ON, See Figure 14 | 25°C | 0 | | 0.2 | 0.5 | µA |
| | | | | Full | | | | 1 | |
| NC, NO ON leakage current | $I_{NC(ON)}$, $I_{NO(ON)}$ | $V_{NC}$ or $V_{NO}$ = 0 to $V_+$, $V_{COM}$ = Open, | Switch ON, See Figure 15 | 25°C | 2.7 V | | 0.001 | 0.01 | µA |
| | | | | Full | | | | 0.02 | |
| COM ON leakage current | $I_{COM(ON)}$ | $V_{NC}$ or $V_{NO}$ = Open, $V_{COM}$ = 0 to $V_+$, | Switch ON, See Figure 15 | 25°C | 2.7 V | | 0.003 | 0.03 | µA |
| | | | | Full | | | | 0.05 | |
| **Digital Control Input (IN)** | | | | | | | | | |
| Input logic high | $V_{IH}$ | | | Full | | $V_+$ × 0.75 | | 5.5 | V |
| Input logic low | $V_{IL}$ | | | Full | | 0 | | $V_+$ × 0.25 | V |
| Input leakage current | $I_{IH}$, $I_{IL}$ | $V_I$ = 5.5 V or 0 | | 25°C | 2.7 V | | 0.005 | 0.01 | µA |
| | | | | Full | | | | 0.02 | |

## ELECTRICAL CHARACTERISTICS FOR 2.5-V SUPPLY (continued)

$V_+$ = 2.3 V to 2.7 V, $T_A$ = –40°C to 85°C (unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | | $T_A$ | $V_+$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| **Dynamic** | | | | | | | | | |
| Turn-on time | $t_{ON}$ | $V_{COM}$ = $V_+$ or GND, $R_L$ = 500 Ω, | $C_L$ = 50 pF, See Figure 17 | 25°C | 2.5 V | 3 | 5.8 | 9.6 | ns |
| | | | | Full | 2.3 V to 2.7 V | 3 | | 12 | |
| Turn-off time | $t_{OFF}$ | $V_{COM}$ = $V_+$ or GND, $R_L$ = 500 Ω, | $C_L$ = 50 pF, See Figure 17 | 25°C | 2.5 V | 1.5 | 4.5 | 7.3 | ns |
| | | | | Full | 2.3 V to 2.7 V | 1.5 | | 7.5 | |
| Output voltage during undershoot | $V_{OUTU}$ | See Figure 18 | | | | 2.5 | $V_{OH}$ – 0.3 | | V |
| Output voltage during overshoot | $V_{OUTO}$ | See Figure 18 | | | | | $V_{OL}$ + 0.3 | 2 | V |
| Break-before-make time | $t_{BBM}$ | $V_{NC}$ = $V_{NO}$ = $V_+$/2, $R_L$ = 50 Ω, | $C_L$ = 50 pF, See Figure 19 | 25°C | 2.5 V | 0.5 | 10 | 25 | ns |
| | | | | Full | 2.3 V to 2.7 V | 0.5 | | 28.5 | |
| Charge injection | $Q_C$ | $V_{GEN}$ = 0, $R_{GEN}$ = 0, | $C_L$ = 0.1 nF, See Figure 23 | 25°C | 2.5 V | | –8 | | pC |
| NC, NO OFF capacitance | $C_{NC(OFF)}$, $C_{NO(OFF)}$ | $V_{NC}$ or $V_{NO}$ = $V_+$ or GND, Switch OFF, | See Figure 16 | 25°C | 2.5 V | | 5 | | pF |
| NC, NO ON capacitance | $C_{NC(ON)}$, $C_{NO(ON)}$ | $V_{NC}$ or $V_{NO}$ = $V_+$ or GND, Switch ON, | See Figure 16 | 25°C | 2.5 V | | 15 | | pF |
| COM ON capacitance | $C_{COM(ON)}$ | $V_{COM}$ = $V_+$ or GND, Switch ON, | See Figure 16 | 25°C | 2.5 V | | 15 | | pF |
| Digital input capacitance | $C_I$ | $V_I$ = $V_+$ or GND, | See Figure 16 | 25°C | 2.5 V | | 2.5 | | pF |
| Bandwidth | BW | $R_L$ = 50 Ω, Switch ON, | See Figure 20 | 25°C | 2.5 V | | 367 | | MHz |
| OFF isolation | $O_{ISO}$ | $R_L$ = 50 Ω, f = 10 MHz, | Switch OFF, See Figure 21 | 25°C | 2.5 V | | –60 | | dB |
| Crosstalk | $X_{TALK}$ | $R_L$ = 50 Ω, f = 10 MHz, | Switch ON, See Figure 22 | 25°C | 2.5 V | | –60 | | dB |
| Total harmonic distortion | THD | $R_L$ = 600 Ω, $C_L$ = 50 pF, | f = 20 Hz to 20 kHz, See Figure 24 | 25°C | 2.5 V | | 0.15 | | % |
| **Supply** | | | | | | | | | |
| Positive supply current | $I_+$ | $V_I$ = $V_+$ or GND, | Switch ON or OFF | 25°C | 2.7 V | | 0.05 | 0.1 | nA |
| | | | | Full | | | | 0.5 | |

## ELECTRICAL CHARACTERISTICS FOR 1.8-V SUPPLY

$V_+$ = 1.65 V to 1.95 V, $T_A$ = –40°C to 85°C (unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | | $T_A$ | $V_+$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| **Analog Switch** | | | | | | | | | |
| Analog signal range | $V_{COM}$, $V_{NO}$, $V_{NC}$ | | | | | 0 | | $V_+$ | V |
| Voltage undershoot | $V_{IKU}$ | 0 ≥ ($I_{NC}$, $I_{NO}$, or $I_{COM}$) ≥ –50 mA | | | 1.95 V | | | | V |
| Peak ON-state resistance | $r_{peak}$ | 0 ≤ ($V_{NO}$ or $V_{NC}$) ≤ $V_+$, $I_{COM}$ = –4 mA, | Switch ON, See Figure 13 | 25°C | 1.65 V | | 13.8 | 60 | Ω |
| | | | | Full | | | | 120 | |
| ON-state resistance | $r_{on}$ | $V_{NO}$ or $V_{NC}$ = 0, $I_{COM}$ = 4 mA | Switch ON, See Figure 13 | 25°C | 1.65 V | | 5.9 | 15 | Ω |
| | | | | Full | | | | 15 | |
| | | $V_{NO}$ or $V_{NC}$ = 1.65 V, $I_{COM}$ = –4 mA | | 25°C | | | 12.8 | 40 | |
| | | | | Full | | | | 45 | |
| ON-state resistance match between channels | $\Delta r_{on}$ | $V_{NO}$ or $V_{NC}$ = 1.15 V, $I_{COM}$ = –4 mA, | Switch ON, See Figure 13 | 25°C | 1.65 V | | 0.1 | 0.5 | Ω |
| | | | | Full | | | | 0.8 | |
| ON-state resistance flatness | $r_{on(flat)}$ | 0 ≤ ($V_{NO}$ or $V_{NC}$) ≤ $V_+$, $I_{COM}$ = –4 mA, | Switch ON, See Figure 13 | 25°C | 1.65 V | | 26.5 | 60 | Ω |
| | | | | Full | | | | 80 | |
| NC, NO OFF leakage current | $I_{NC(OFF)}$, $I_{NO(OFF)}$ | $V_{NC}$ or $V_{NO}$ = 0 to $V_+$, $V_{COM}$ = $V_+$ to 0, | Switch OFF, See Figure 14 | 25°C | 1.95 V | | 0 | 0.03 | µA |
| | | | | Full | | | | 0.05 | |
| | $I_{NC(PWROFF)}$, $I_{NOPWROFF)}$ | $V_{NC}$ or $V_{NO}$ = 0 to 1.95 V, $V_{COM}$ = 1.95 V to 0, | Switch OFF, See Figure 14 | 25°C | 0 | | 0.15 | 0.50 | |
| | | | | Full | | | | 0.75 | |
| COM OFF leakage current | $I_{COM(PWROFF)}$ | $V_{COM}$ = 0 to 1.95 V, $V_{NC}$ or $V_{NO}$ = 1.95 V to 0, | Switch ON, See Figure 14 | 25°C | 0 | | 0.2 | 0.5 | µA |
| | | | | Full | | | | 1 | |
| NC, NO ON leakage current | $I_{NC(ON)}$, $I_{NO(ON)}$ | $V_{NC}$ or $V_{NO}$ = 0 to $V_+$, $V_{COM}$ = Open, | Switch ON, See Figure 15 | 25°C | 1.95 V | | 0.001 | 0.01 | µA |
| | | | | Full | | | | 0.02 | |
| COM ON leakage current | $I_{COM(ON)}$ | $V_{NC}$ or $V_{NO}$ = Open, $V_{COM}$ = 0 to $V_+$, | Switch ON, See Figure 15 | 25°C | 1.95 V | | 0.003 | 0.03 | µA |
| | | | | Full | | | | 0.05 | |
| **Digital Control Input (IN)** | | | | | | | | | |
| Input logic high | $V_{IH}$ | | | Full | | $V_+$ × 0.75 | | 5.5 | V |
| Input logic low | $V_{IL}$ | | | Full | | 0 | | $V_+$ × 0.25 | V |
| Input leakage current | $I_{IH}$, $I_{IL}$ | $V_I$ = 5.5 V or 0 | | 25°C | 1.95 V | | 0.005 | 0.01 | µA |
| | | | | Full | | | | 0.02 | |

## ELECTRICAL CHARACTERISTICS FOR 1.8-V SUPPLY (continued)

$V_+$ = 1.65 V to 1.95 V, $T_A$ = –40°C to 85°C (unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | | $T_A$ | $V_+$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| **Dynamic** | | | | | | | | | |
| Turn-on time | $t_{ON}$ | $V_{COM}$ = $V_+$ or GND, $R_L$ = 500 Ω, | $C_L$ = 50 pF, See Figure 17 | 25°C | 1.8 V | | 9.5 | 23 | ns |
| | | | | Full | 1.65 V to 1.95 V | | | 24 | |
| Turn-off time | $t_{OFF}$ | $V_{COM}$ = $V_+$ or GND, $R_L$ = 500 Ω, | $C_L$ = 50 pF, See Figure 17 | 25°C | 1.8 V | | 5.9 | 10 | ns |
| | | | | Full | 1.65 V to 1.95 V | | | 12 | |
| Output voltage during undershoot | $V_{OUTU}$ | See Figure 18 | | | | 2.5 | $V_{OH}$ – 0.3 | | V |
| Output voltage during overshoot | $V_{OUTO}$ | See Figure 18 | | | | | $V_{OL}$ + 0.3 | 2 | V |
| Break-before-make time | $t_{BBM}$ | $V_{NC}$ = $V_{NO}$ = $V_+$/2, $R_L$ = 50 Ω, | $C_L$ = 50 pF, See Figure 19 | 25°C | 1.8 V | 0.5 | 18 | 50 | ns |
| | | | | Full | 1.65 V to 1.95 V | 0.5 | | 55 | |
| Charge injection | $Q_C$ | $V_{GEN}$ = 0, $R_{GEN}$ = 0, | $C_L$ = 0.1 nF, See Figure 23 | 25°C | 1.8 V | | –5 | | pC |
| NC, NO OFF capacitance | $C_{NC(OFF)}$, $C_{NO(OFF)}$ | $V_{NC}$ or $V_{NO}$ = $V_+$ or GND, Switch OFF, | See Figure 16 | 25°C | 1.8 V | | 5.5 | | pF |
| NC, NO ON capacitance | $C_{NC(ON)}$, $C_{NO(ON)}$ | $V_{NC}$ or $V_{NO}$ = $V_+$ or GND, Switch ON, | See Figure 16 | 25°C | 1.8 V | | 15.5 | | pF |
| COM ON capacitance | $C_{COM(ON)}$ | $V_{COM}$ = $V_+$ or GND, Switch ON, | See Figure 16 | 25°C | 1.8 V | | 15.5 | | pF |
| Digital input capacitance | $C_I$ | $V_I$ = $V_+$ or GND, | See Figure 16 | 25°C | 1.8 V | | 2.5 | | pF |
| Bandwidth | BW | $R_L$ = 50 Ω, Switch ON, | See Figure 20 | 25°C | 1.8 V | | 369 | | MHz |
| OFF isolation | $O_{ISO}$ | $R_L$ = 50 Ω, f = 10 MHz, | Switch OFF, See Figure 21 | 25°C | 1.8 V | | –60 | | dB |
| Crosstalk | $X_{TALK}$ | $R_L$ = 50 Ω, f = 10 MHz, | Switch ON, See Figure 22 | 25°C | 1.8 V | | –60 | | dB |
| Total harmonic distortion | THD | $R_L$ = 600 Ω, $C_L$ = 50 pF, | f = 20 Hz to 20 kHz, See Figure 24 | 25°C | 1.8 V | | 0.4 | | % |
| **Supply** | | | | | | | | | |
| Positive supply current | $I_+$ | $V_I$ = $V_+$ or GND, | Switch ON or OFF | 25°C | 1.95 V | | 0.05 | 0.06 | µA |
| | | | | Full | | | | 0.3 | |

## TYPICAL PERFORMANCE

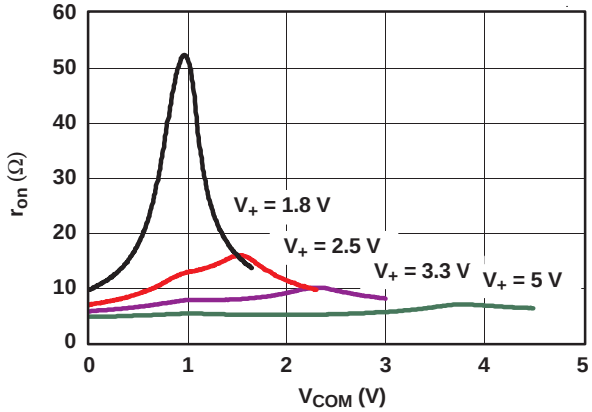



**Figure 1. $r_{on}$ vs $V_{COM}$**

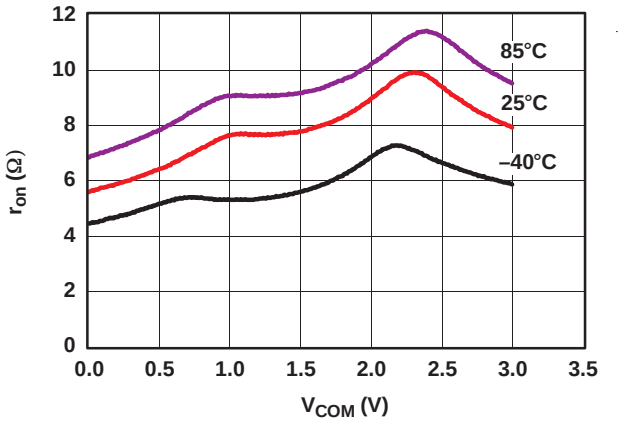



**Figure 2. $r_{on}$ vs $V_{COM}$ ($V_+$ = 3 V)**

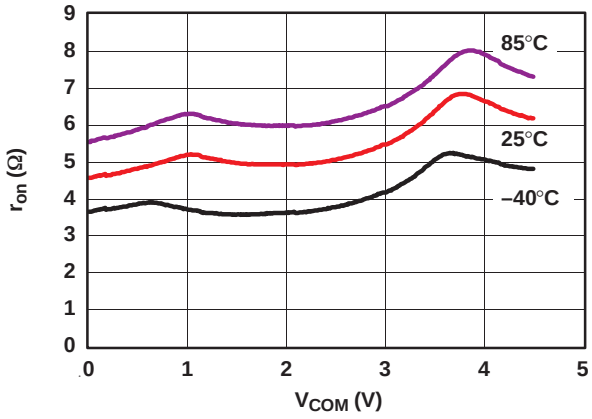



**Figure 3. $r_{on}$ vs $V_{COM}$ ($V_+$ = 5 V)**

## TYPICAL PERFORMANCE (continued)

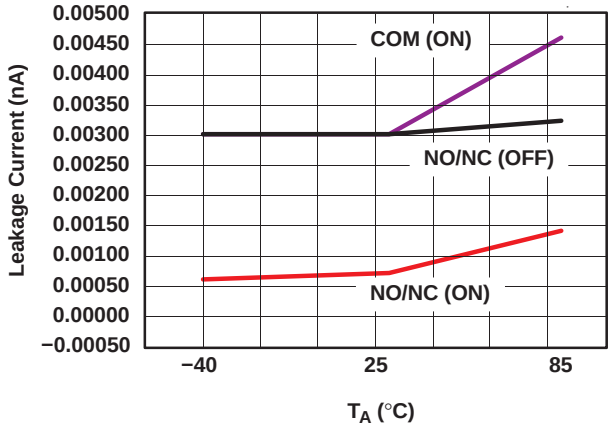



**Figure 4. Leakage Current vs Temperature ($V_+$ = 5.5 V)**

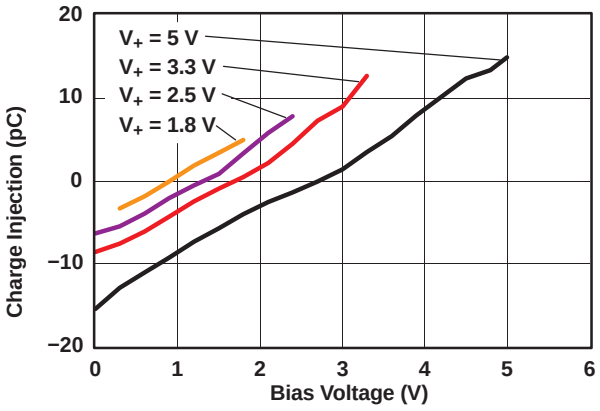



**Figure 5. Charge Injection ($Q_C$) vs $V_{COM}$**

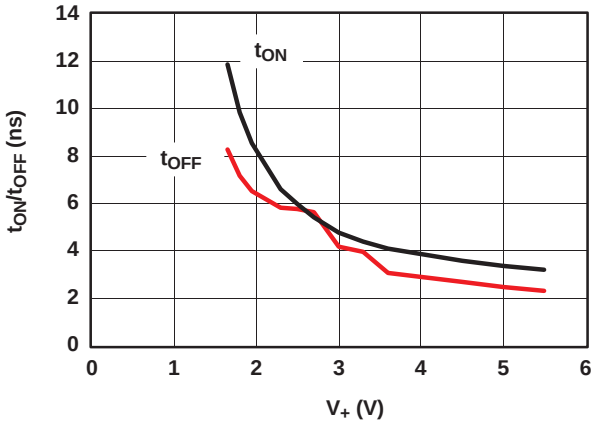



**Figure 6. $t_{ON}$ and $t_{OFF}$ vs Supply Voltage**

## TYPICAL PERFORMANCE (continued)

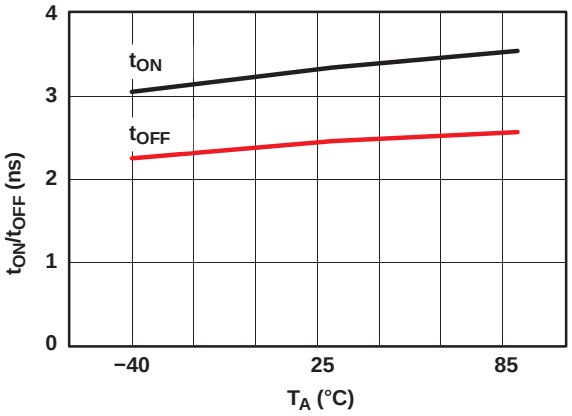



**Figure 7. $t_{ON}$ and $t_{OFF}$ vs Temperature ($V_+$ = 5 V)**

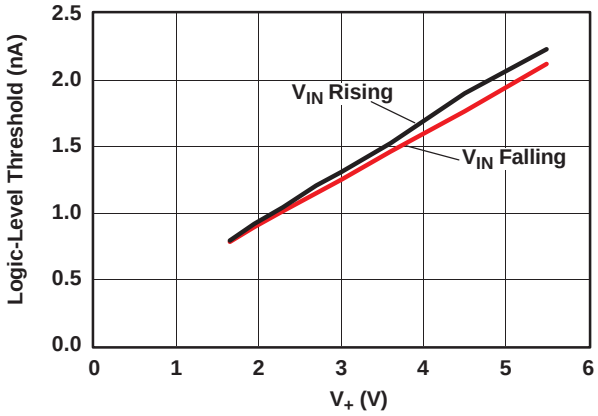



**Figure 8. Logic-Level Threshold vs $V_+$**

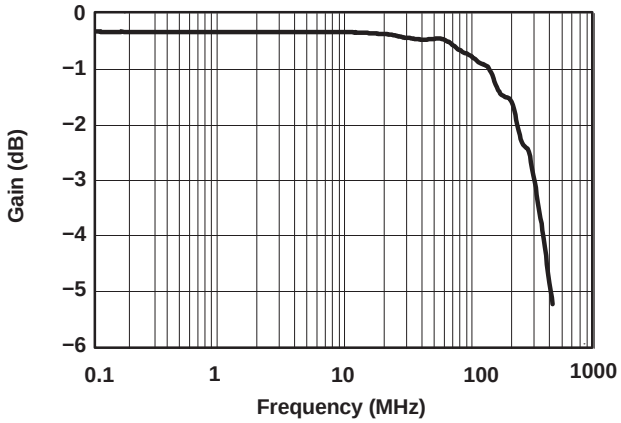



**Figure 9. Bandwidth ($V_+$ = 3.3 V)**

## TYPICAL PERFORMANCE (continued)

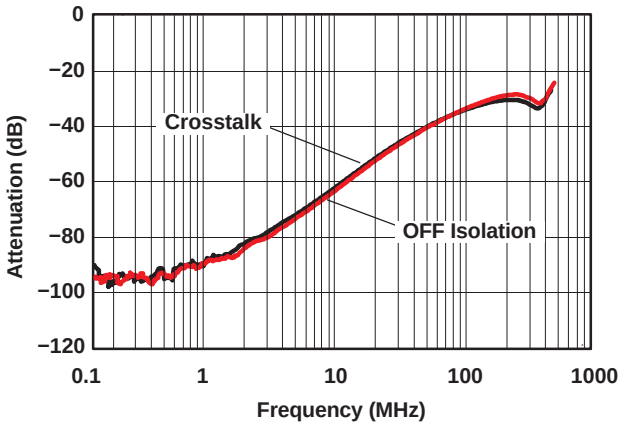



**Figure 10. OFF Isolation and Crosstalk ($V_+$ = 3.3 V)**

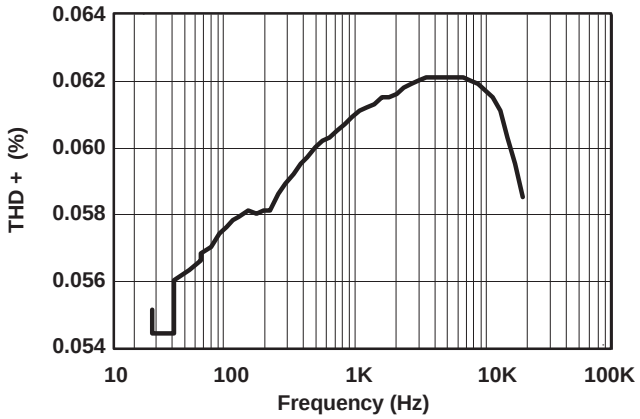



**Figure 11. Total Harmonic Distortion (THD) vs Frequency ($V_+$ = 3.3 V)**

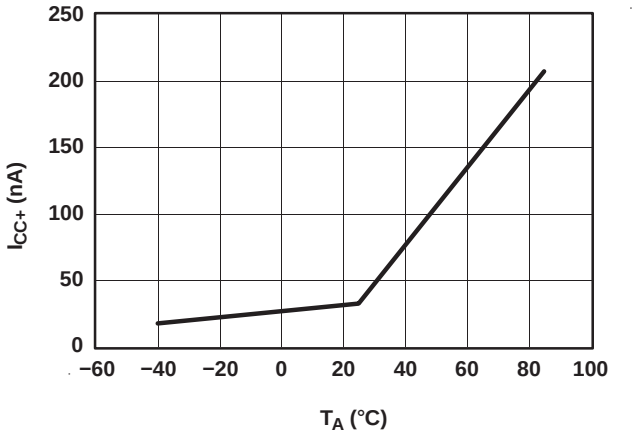



**Figure 12. Power-Supply Current vs Temperature ($V_+$ = 5 V)**

## PARAMETER DESCRIPTION

| SYMBOL | DESCRIPTION |
|---|---|
| $V_{COM}$ | Voltage at COM |
| $V_{NC}$ | Voltage at NC |
| $V_{NO}$ | Voltage at NO |
| $r_{on}$ | Resistance between COM and NC or COM and NO ports when the channel is ON |
| $r_{peak}$ | Peak on-state resistance over a specified voltage range |
| $\Delta r_{on}$ | Difference of $r_{on}$ between channels in a specific device |
| $r_{on(flat)}$ | Difference between the maximum and minimum value of $r_{on}$ in a channel over the specified range of conditions |
| $I_{NC(OFF)}$ | Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state |
| $I_{NC(PWROFF)}$ | Leakage current measured at the NC port during the power-down condition, $V_+ = 0$ |
| $I_{NO(OFF)}$ | Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state |
| $I_{NO(PWROFF)}$ | Leakage current measured at the NO port during the power-down condition, $V_+ = 0$ |
| $I_{NC(ON)}$ | Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open |
| $I_{NO(ON)}$ | Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open |
| $I_{COM(ON)}$ | Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the ON state and the output (NC or NO) open |
| $I_{COM(PWROFF)}$ | Leakage current measured at the COM port during the power-down condition, $V_+ = 0$ |
| $V_{IH}$ | Minimum input voltage for logic high for the control input (IN) |
| $V_{IL}$ | Maximum input voltage for logic low for the control input (IN) |
| $V_I$ | Voltage at the control input (IN) |
| $I_{IH}$, $I_{IL}$ | Leakage current measured at the control input (IN) |
| $t_{ON}$ | Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning ON. |
| $t_{OFF}$ | Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning OFF. |
| $t_{BBM}$ | Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state. |
| $Q_C$ | Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NO or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input.Charge injection, $Q_C = C_L \times \Delta V_{COM}$, $C_L$ is the load capacitance and $\Delta V_{COM}$ is the change in analog output voltage. |
| $C_{NC(OFF)}$ | Capacitance at the NC port when the corresponding channel (NC to COM) is OFF |
| $C_{NO(OFF)}$ | Capacitance at the NO port when the corresponding channel (NO to COM) is OFF |
| $C_{NC(ON)}$ | Capacitance at the NC port when the corresponding channel (NC to COM) is ON |
| $C_{NO(ON)}$ | Capacitance at the NO port when the corresponding channel (NO to COM) is ON |
| $C_{COM(ON)}$ | Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON |
| $C_I$ | Capacitance of control input (IN) |
| $O_{ISO}$ | OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state. |
| $X_{TALK}$ | Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured in a specific frequency and in dB. |
| BW | Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain. |
| THD | Total harmonic distortion is defined as the ratio of the root mean square (RMS) value of the second, third, and higher harmonics to the magnitude of fundamental harmonic. |
| $I_+$ | Static power-supply current with the control (IN) pin at $V_+$ or GND |
| $V_{OUTU}$ | Output voltage during an undershoot event. This is measured by turning off a specific channel and applying an undershoot voltage at the input of the switch. |
| $V_{OUTO}$ | Output voltage during an overshoot event. This is measured by turning off a specific channel and applying an overshoot voltage at the input of the switch. |

## PARAMETER MEASUREMENT INFORMATION

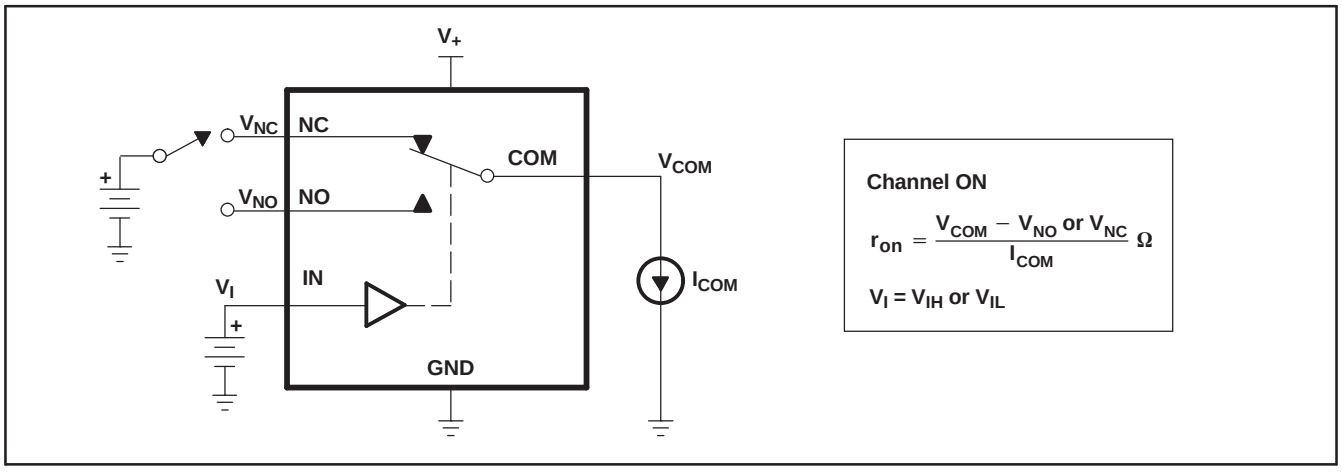



**Figure 13. ON-State Resistance ($r_{on}$)**

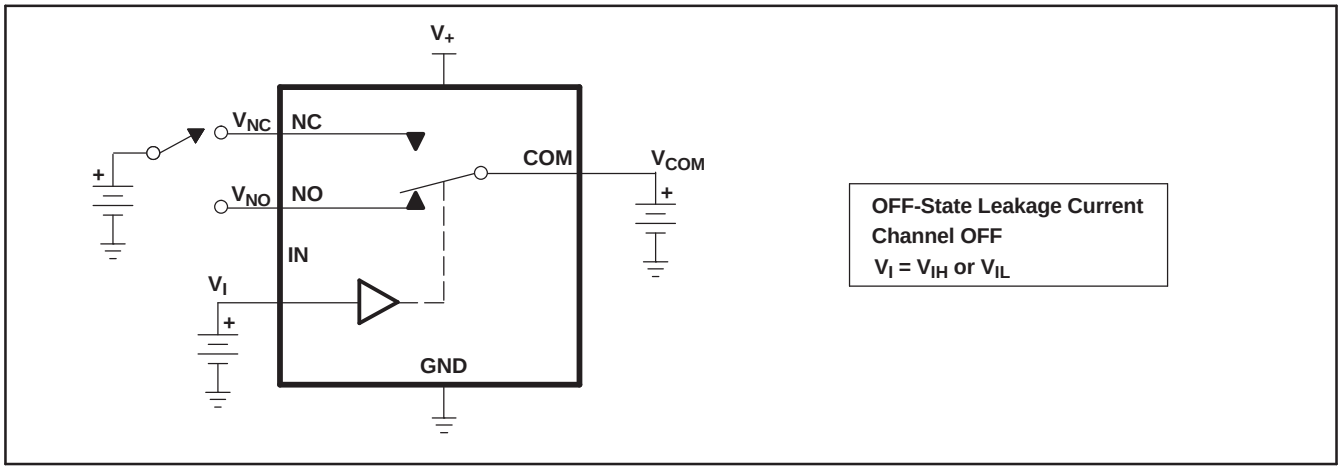



**Figure 14. OFF-State Leakage Current**
**($I_{NC(OFF)}$, $I_{NC(PWROFF)}$, $I_{NO(OFF)}$, $I_{NO(PWROFF)}$, $I_{COM(OFF)}$, $I_{COM(PWROFF)}$)**

## PARAMETER MEASUREMENT INFORMATION (continued)

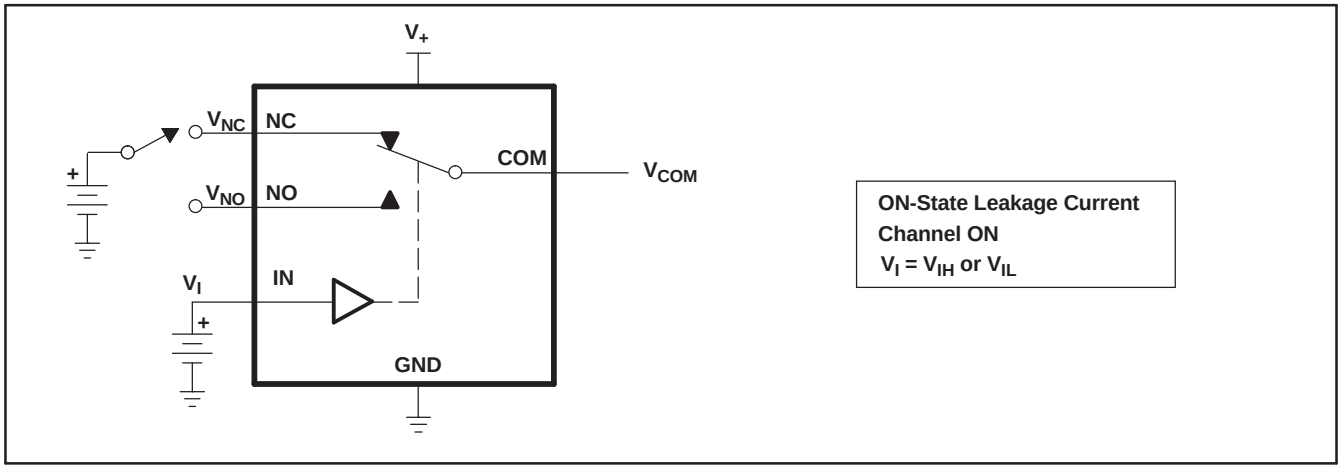



**Figure 15. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)**

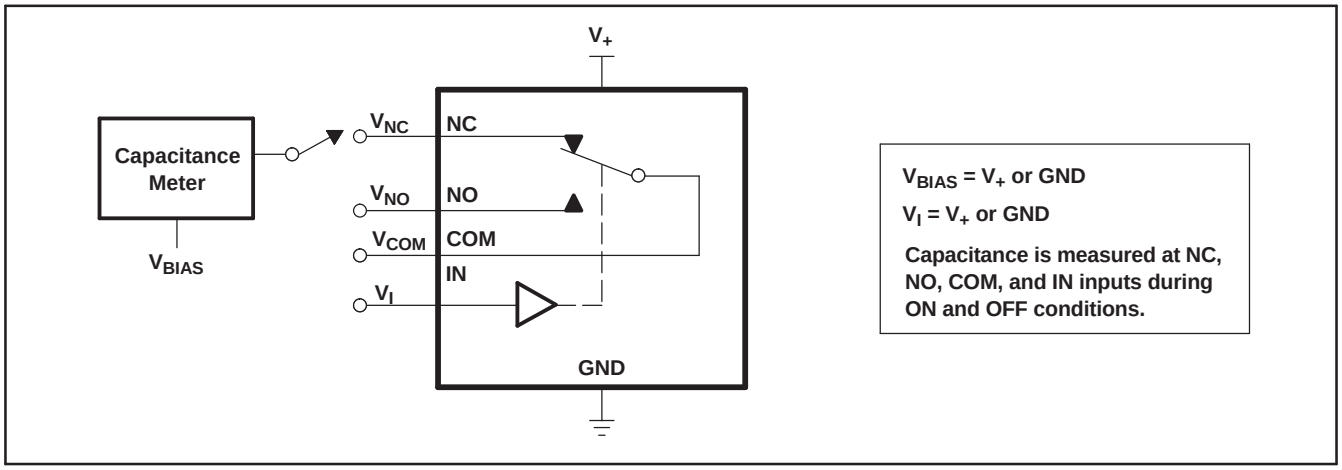
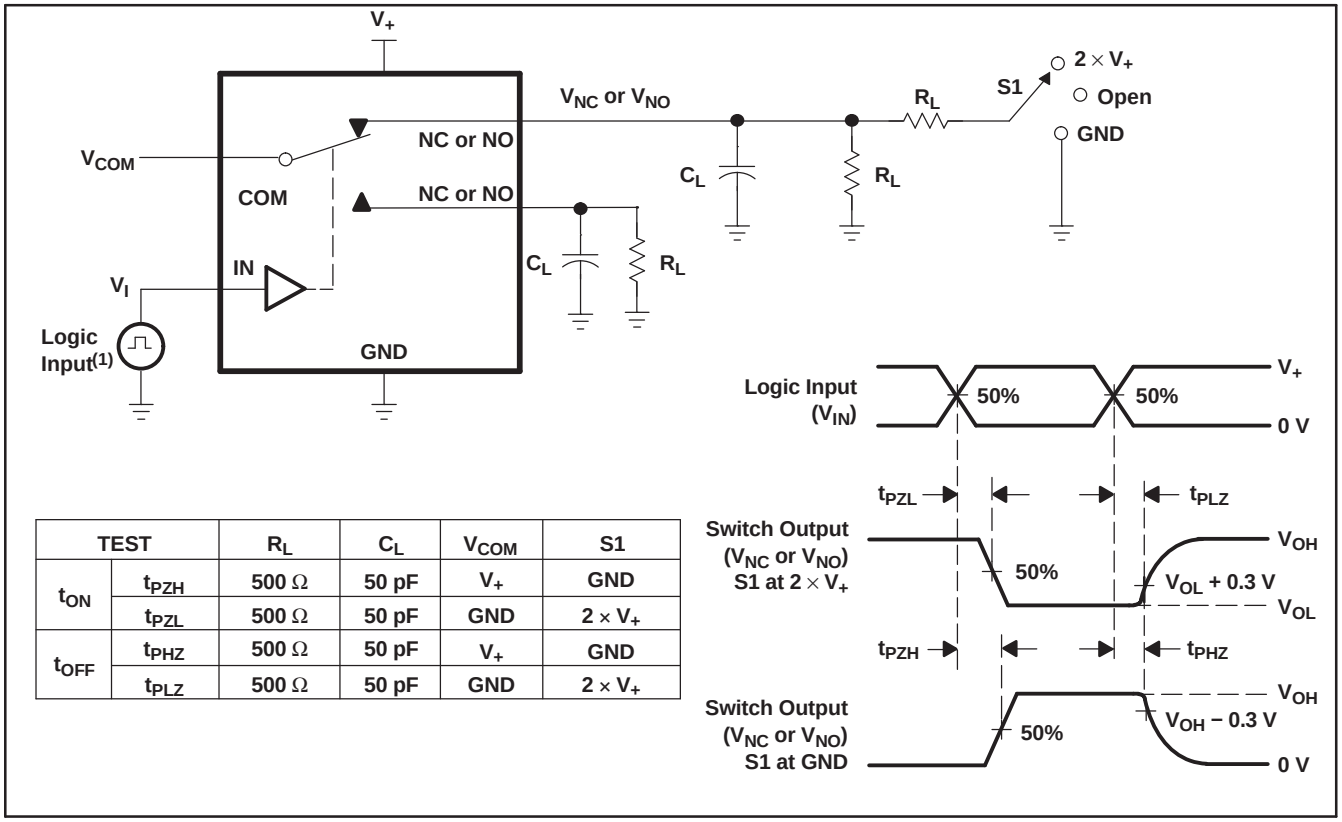



**Figure 16. Capacitance ($C_{IN}$, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)**

## PARAMETER MEASUREMENT INFORMATION (continued)

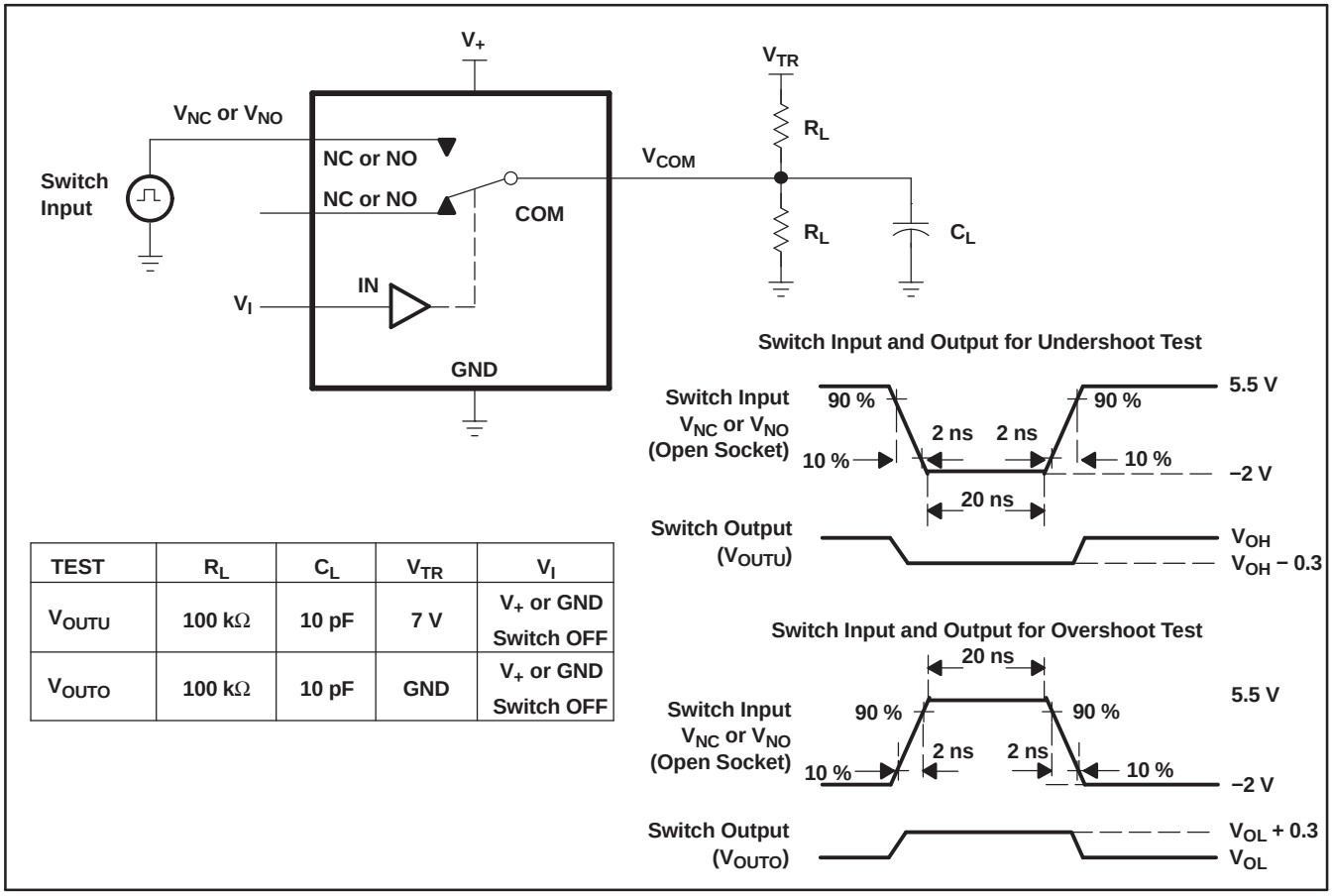



| TEST | | $R_L$ | $C_L$ | $V_{COM}$ | S1 |
|---|---|---|---|---|---|
| $t_{ON}$ | $t_{PZH}$ | 500 Ω | 50 pF | $V_+$ | GND |
| | $t_{PZL}$ | 500 Ω | 50 pF | GND | 2 × $V_+$ |
| $t_{OFF}$ | $t_{PHZ}$ | 500 Ω | 50 pF | $V_+$ | GND |
| | $t_{PLZ}$ | 500 Ω | 50 pF | GND | 2 × $V_+$ |

(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ < 5 ns, $t_f$ < 5 ns.

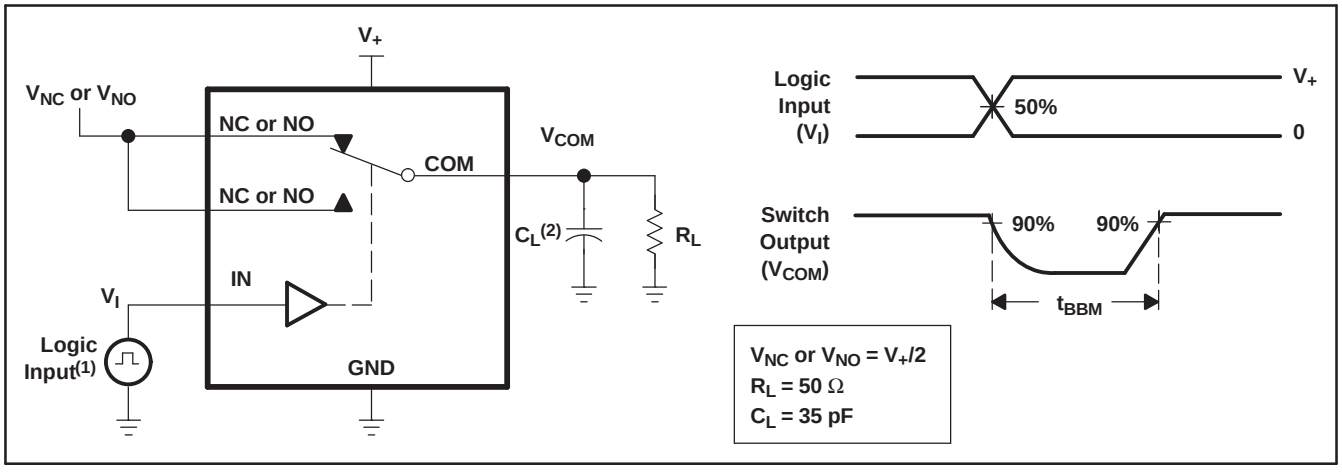
**Figure 17. Turn-On ($t_{ON}$) and Turn-Off ($t_{OFF}$) Time**

## PARAMETER MEASUREMENT INFORMATION (continued)




| TEST | $R_L$ | $C_L$ | $V_{TR}$ | $V_I$ |
|---|---|---|---|---|
| $V_{OUTU}$ | 100 kΩ | 10 pF | 7 V | $V_+$ or GND<br>Switch OFF |
| $V_{OUTO}$ | 100 kΩ | 10 pF | GND | $V_+$ or GND<br>Switch OFF |

**Figure 18. Undershoot and Overshoot Test**




(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ < 5 ns, $t_f$ < 5 ns.

(2) $C_L$ includes probe and jig capacitance.

**Figure 19. Break-Before-Make ($t_{BBM}$) Time**

## PARAMETER MEASUREMENT INFORMATION (continued)

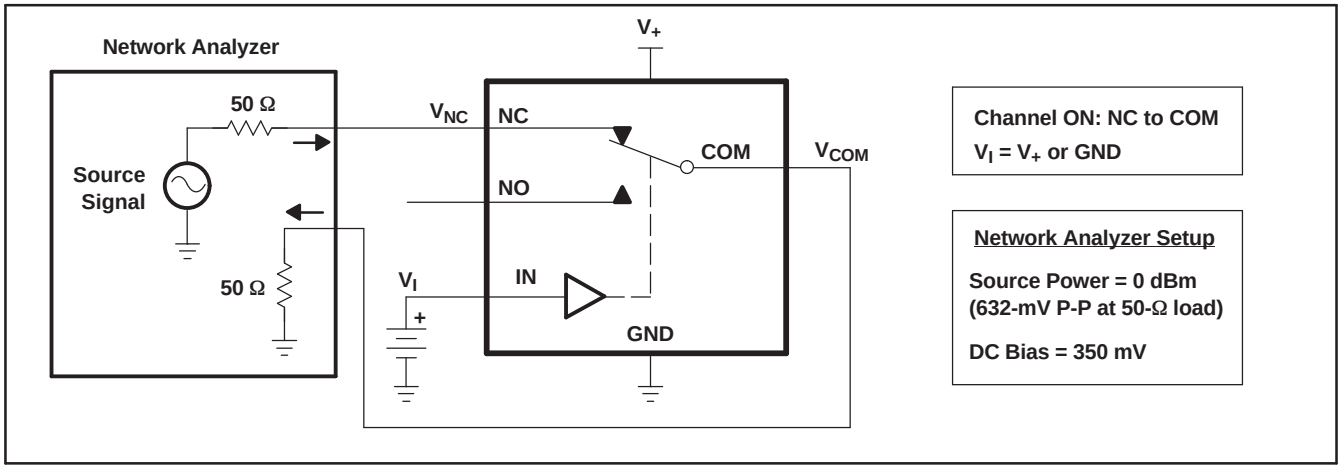



**Figure 20. Bandwidth (BW)**

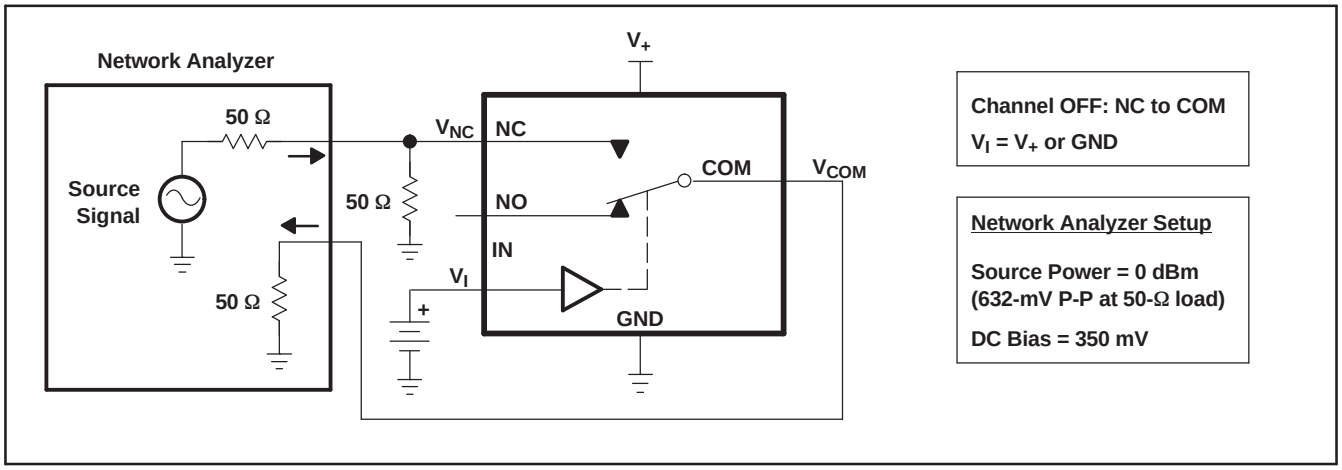



**Figure 21. OFF Isolation ($O_{ISO}$)**

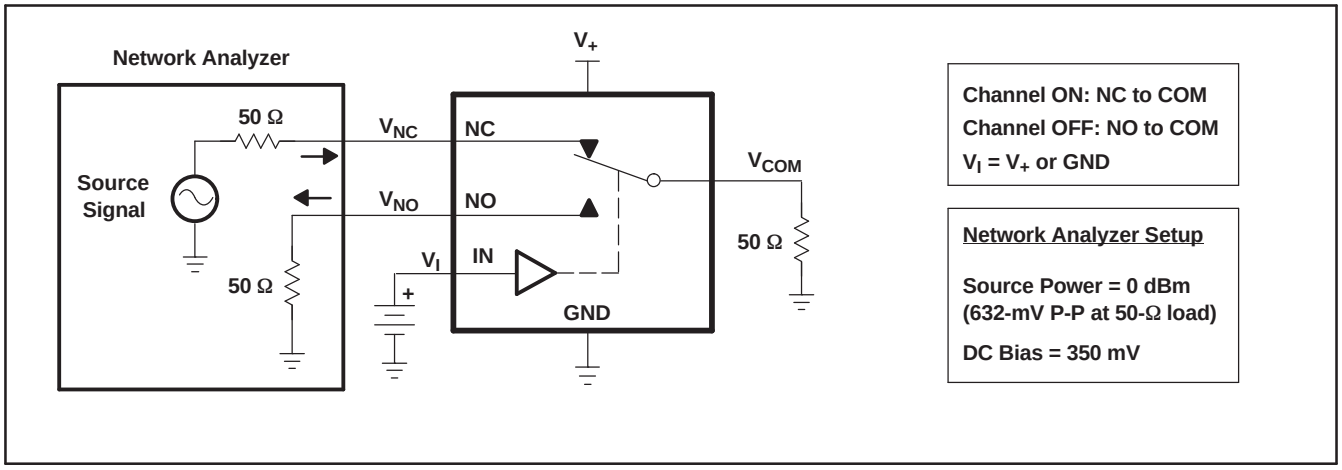
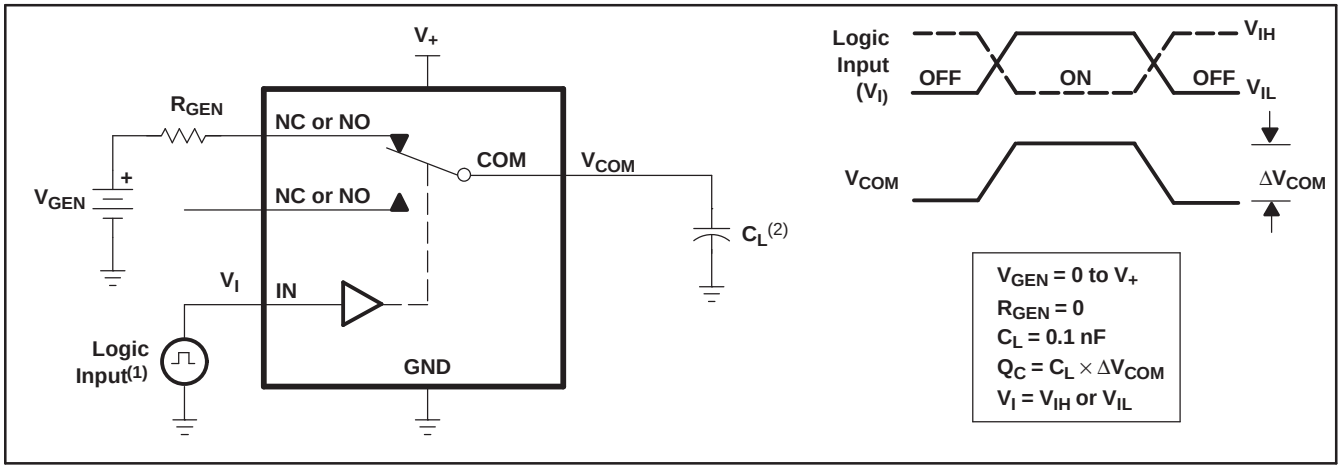



**Figure 22. Crosstalk ($X_{TALK}$)**

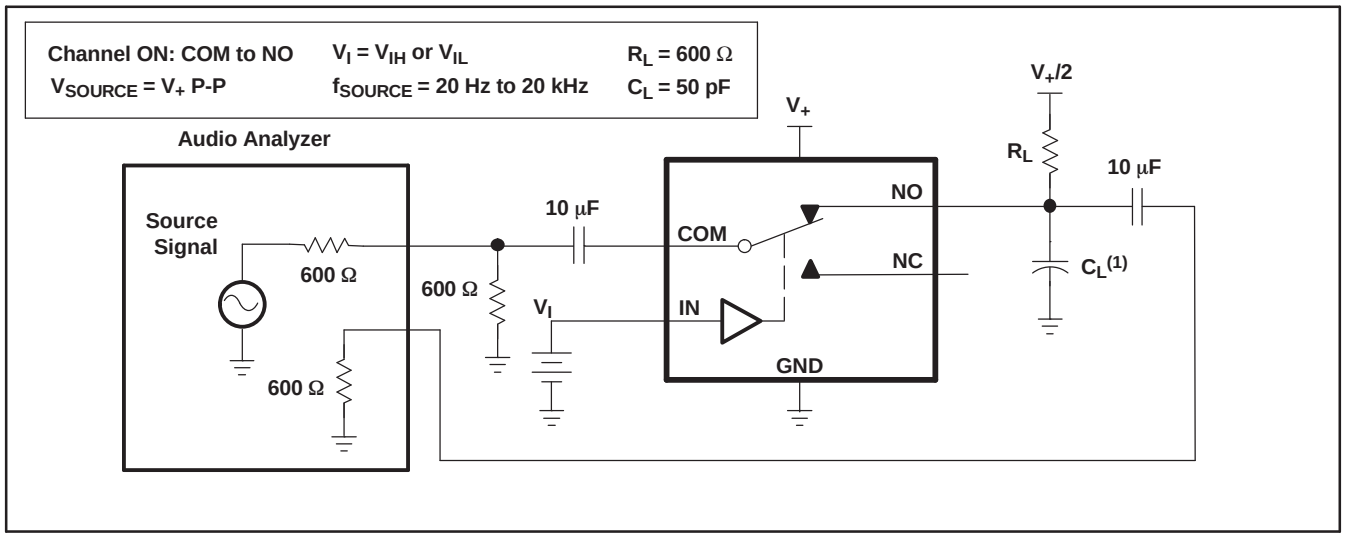
## PARAMETER MEASUREMENT INFORMATION (continued)




(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ < 5 ns, $t_f$ < 5 ns.

(2) $C_L$ includes probe and jig capacitance.

**Figure 23. Charge Injection ($Q_C$)**




(1) $C_L$ includes probe and jig capacitance.

**Figure 24. Total Harmonic Distortion (THD)**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TS5A63157DBVR | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (JBEF ~ JBER) | Samples |
| TS5A63157DBVRG4 | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | JBEF | Samples |
| TS5A63157DCKR | ACTIVE | SC70 | DCK | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (J75 ~ J7F ~ J7R) | Samples |
| TS5A63157DCKRG4 | ACTIVE | SC70 | DCK | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (J75 ~ J7F ~ J7R) | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

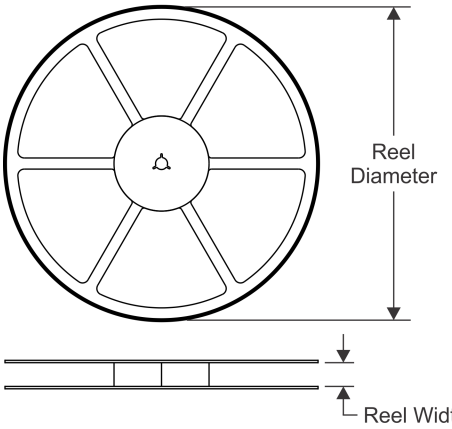
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

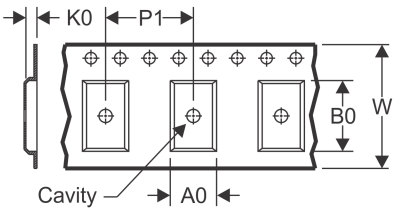
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

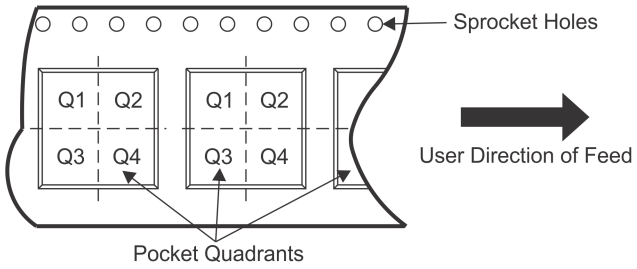



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

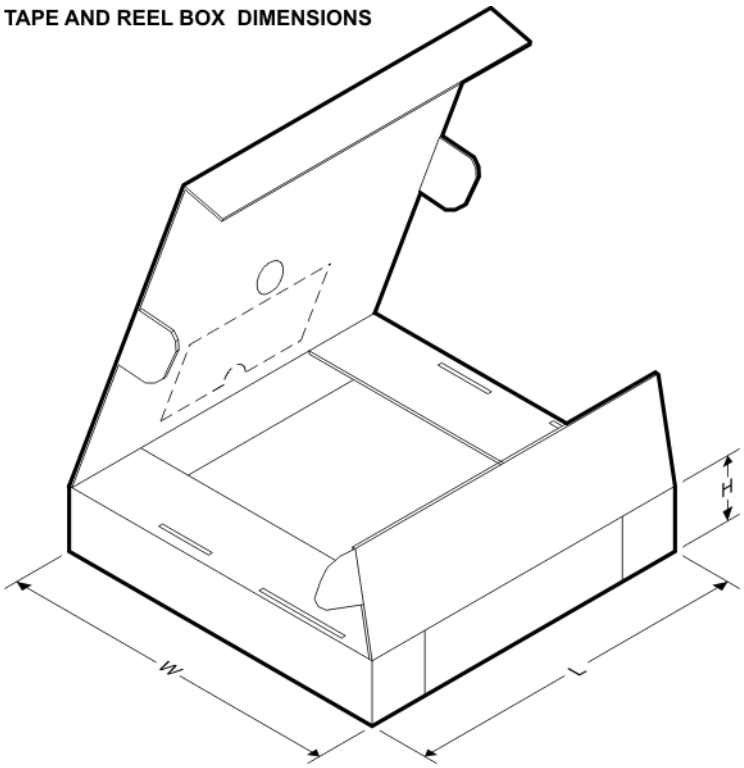
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TS5A63157DBVR | SOT-23 | DBV | 6 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TS5A63157DBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TS5A63157DBVRG4 | SOT-23 | DBV | 6 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TS5A63157DCKR | SC70 | DCK | 6 | 3000 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| TS5A63157DCKR | SC70 | DCK | 6 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |

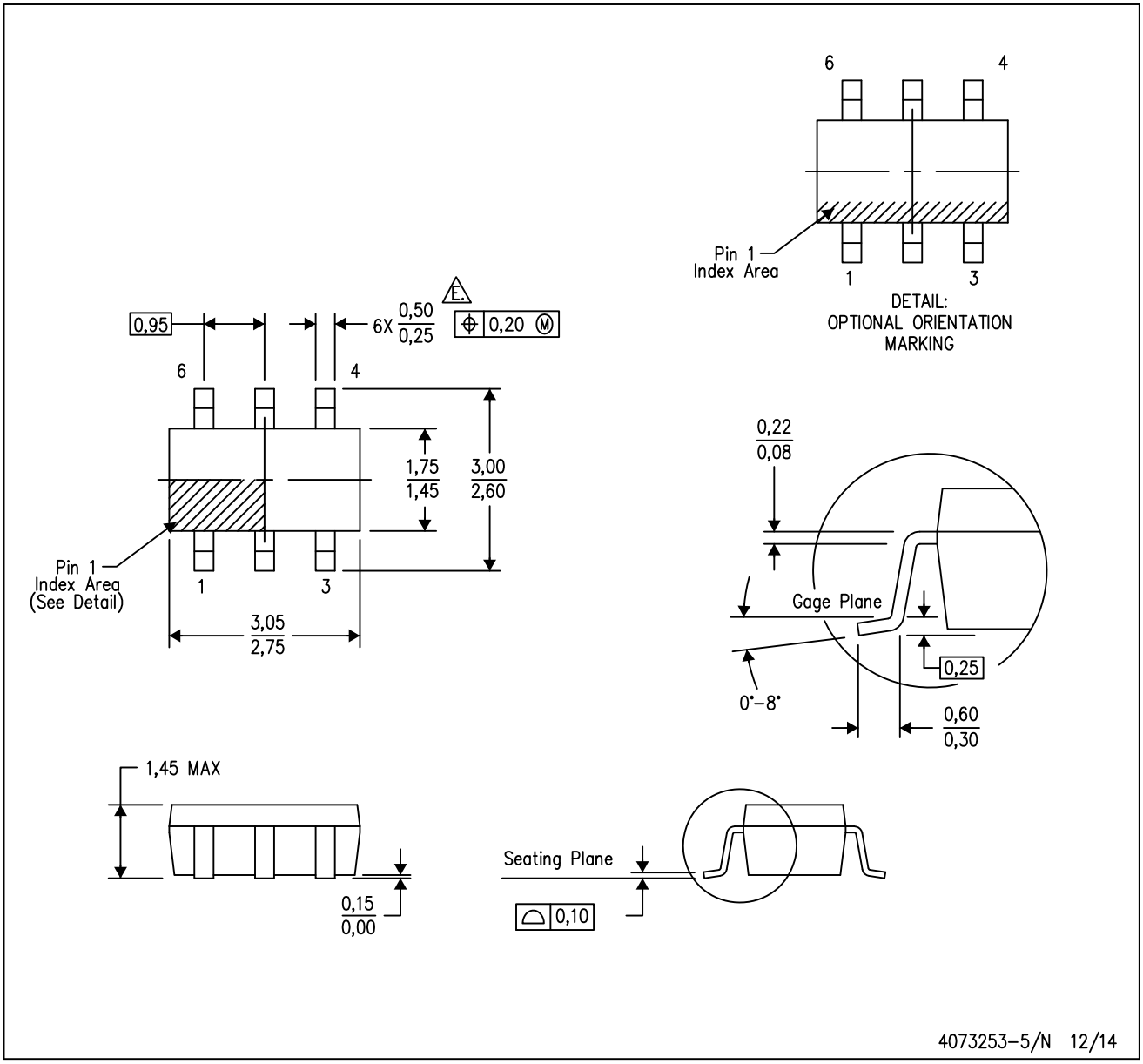
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

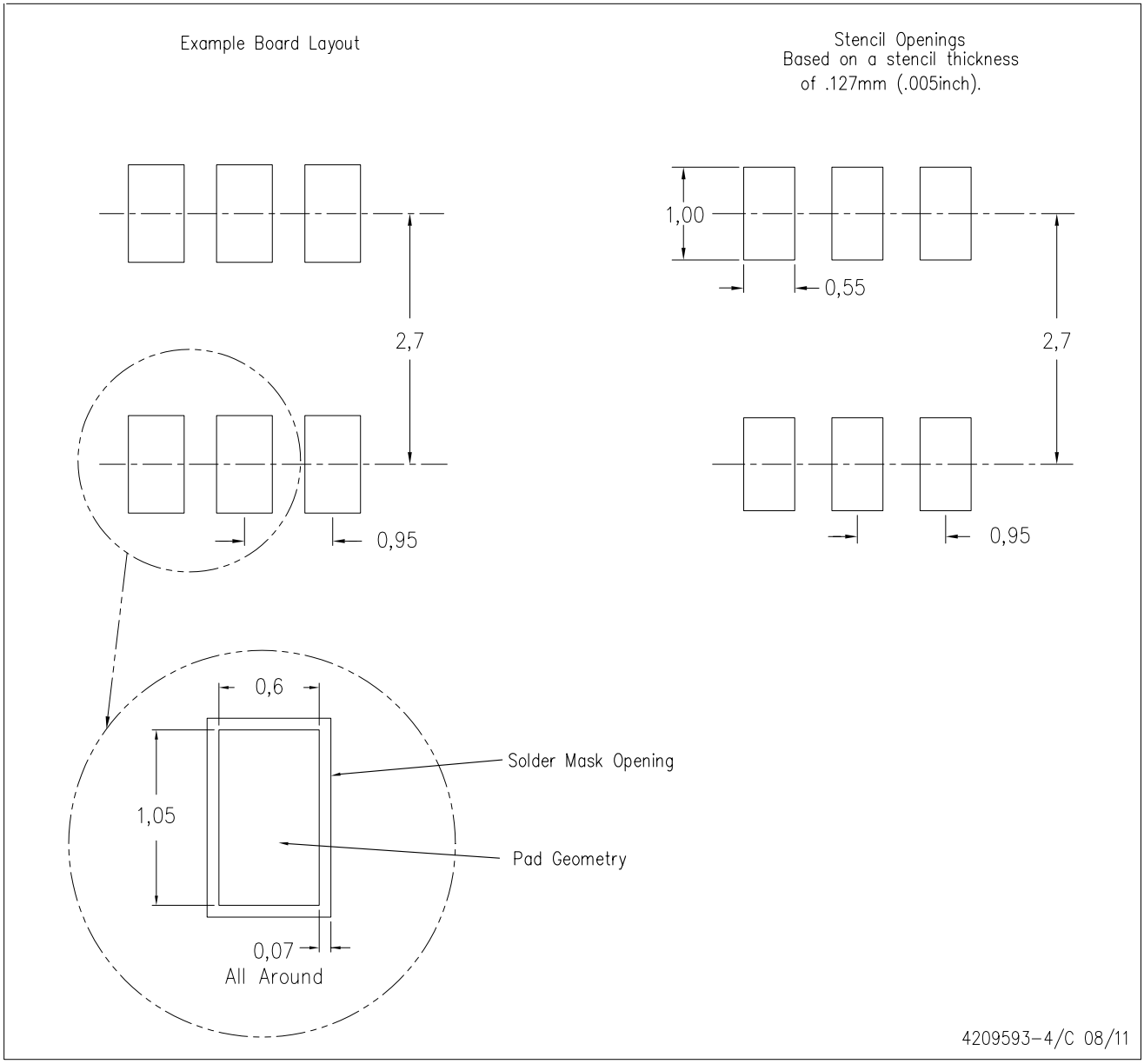
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TS5A63157DBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| TS5A63157DBVR | SOT-23 | DBV | 6 | 3000 | 202.0 | 201.0 | 28.0 |
| TS5A63157DBVRG4 | SOT-23 | DBV | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| TS5A63157DCKR | SC70 | DCK | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| TS5A63157DCKR | SC70 | DCK | 6 | 3000 | 180.0 | 180.0 | 18.0 |

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



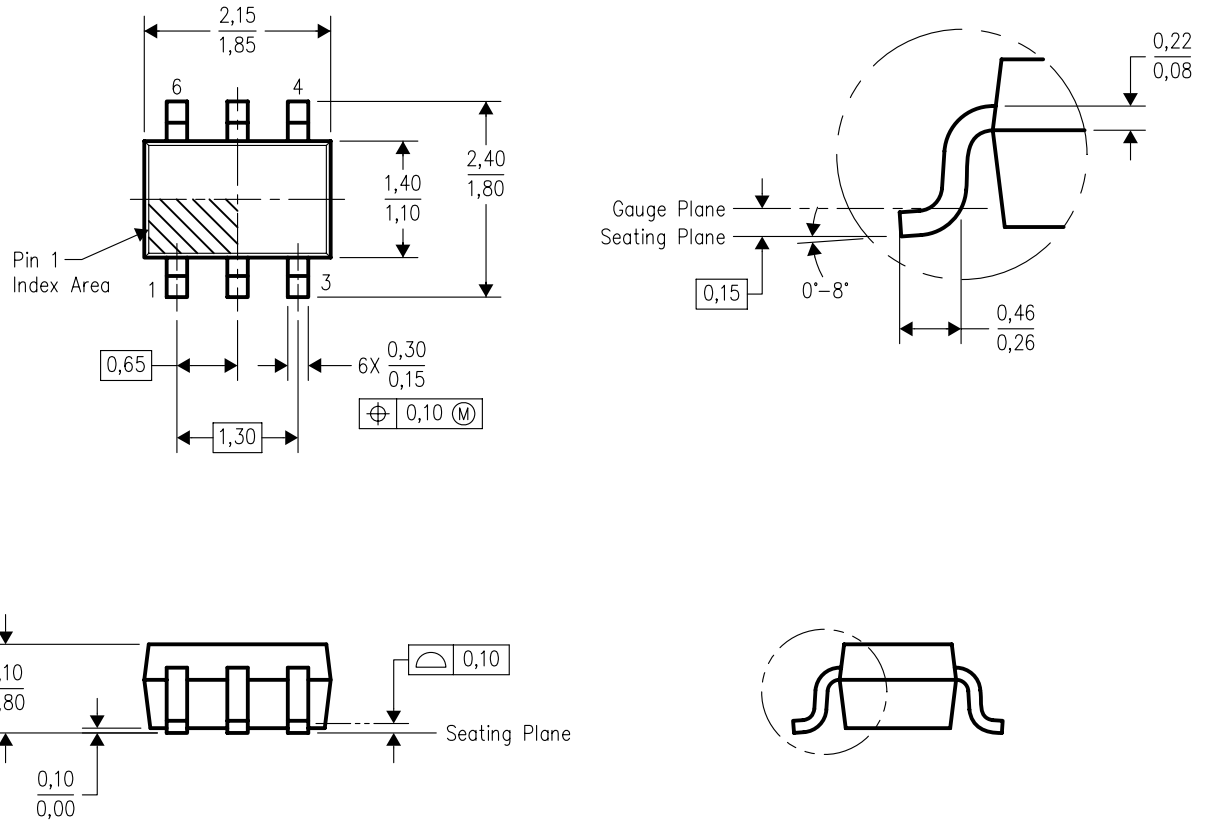

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

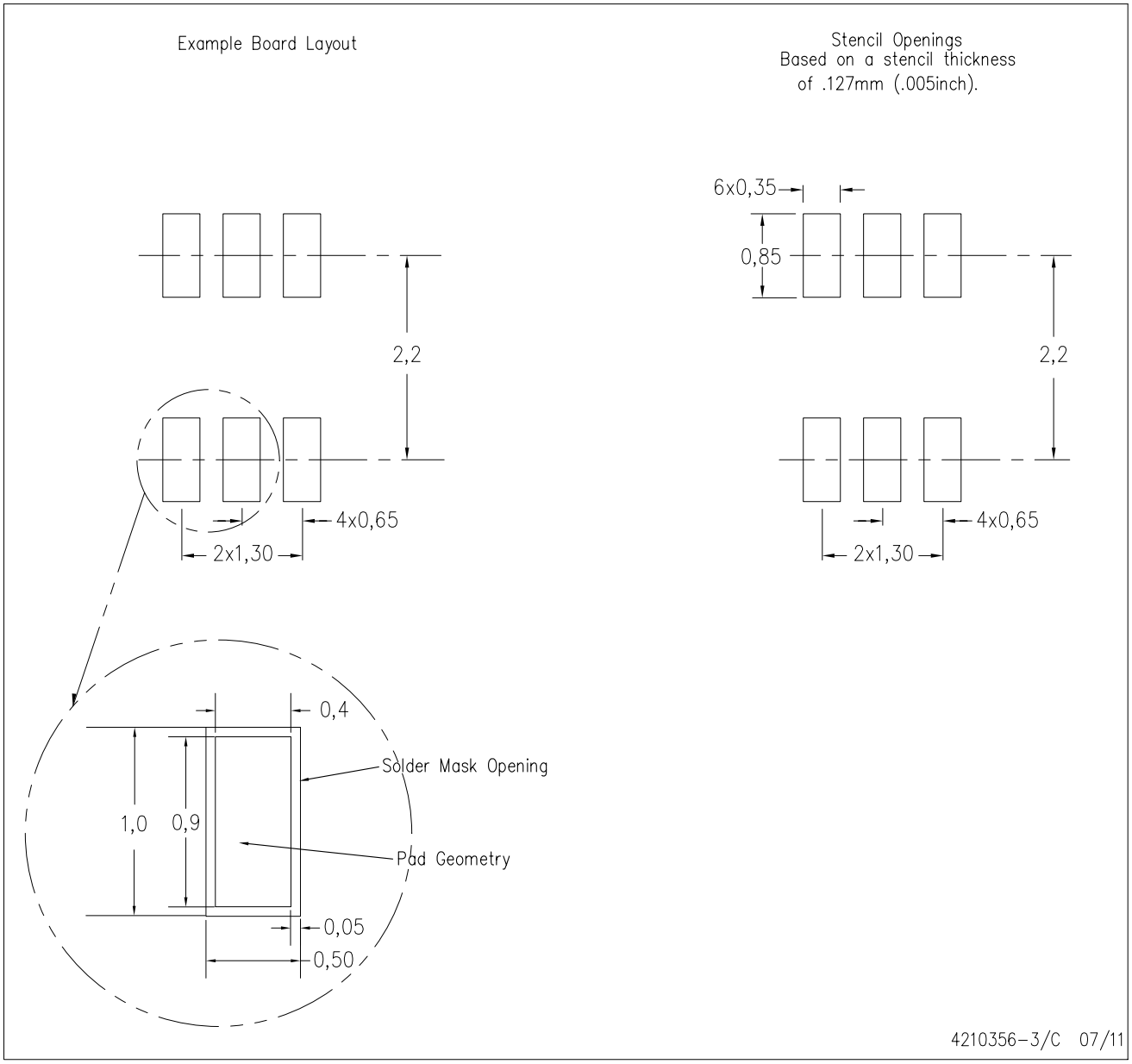
## DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE




4093553–4/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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