TEXAS INSTRUMENTS

bq32000

SLUS900E – DECEMBER 2008 – REVISED AUGUST 2015

bq32000 Real-Time Clock (RTC)

1 Features

- Automatic Switchover to Backup Supply
- I^{2}C Interface Supports Serial Clock up to 400 kHz
- Uses 32.768-kHz Crystal With –63-ppm to +126-ppm Adjustment
- Integrated Oscillator-Fail Detection
- 8-Pin SOIC Package
- –40°C to 85°C Ambient Operating Temperature

2 Applications

- General Consumer Electronics

3 Description

The bq32000 device is a compatible replacement for industry standard real-time clocks.

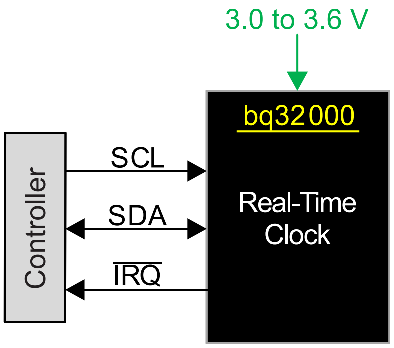
The bq32000 features an automatic backup supply with integrated trickle charger. The backup supply can be implemented using a capacitor or non-rechargeable battery. The bq32000 has a programmable calibration adjustment from –63 ppm to +126 ppm. The bq32000 registers include an OF (oscillator fail) flag indicating the status of the RTC oscillator, as well as a STOP bit that allows the host processor to disable the oscillator. The time registers are normally updated once per second, and all the registers are updated at the same time to prevent a timekeeping glitch. The bq32000 includes automatic leap-year compensation.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq32000	SOIC (8)	4.90 mm x 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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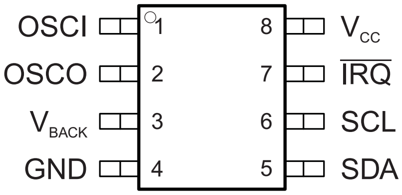
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (November 2011) to Revision E	Page
• Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section.	1
• Added Storage Temperature to Absolute Maximum Ratings	4
• Changed V_{CC} = 0 to VCC needs a pulse.	5

5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	**NO.**		
POWER AND GROUND			
GND	4	-	Ground
V_{BACK}	3	-	Backup device power
V_{CC}	8	-	Main device power
SERIAL INTERFACE			
SCL	6	I	I^2C serial interface clock
SDA	5	I/O	I^2C serial data
INTERRUPT			
$\overline{IRQ}$	7	O	Configurable interrupt output. Open-drain output.
OSCILLATOR			
OSCI	1	-	Oscillator input
OSCO	2	-	Oscillator output

6 Specifications

6.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage, V_{IN}	V_{CC} to GND	–0.3	4	V
	All other pins to GND	–0.3	V_{CC} + 0.3	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–60	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage, V_{CC} to GND	3		3.6	V
T_A	Operating free-air temperature	–40		85	°C
f_o	Crystal resonant frequency		32.768		kHz
R_S	Crystal series resistance			70	kΩ
C_L	Crystal load capacitance	10.8	12	13.2	pF

6.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC[1]		bq32000 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	114.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	59.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.9	°C/W
ψ_{JT}	Junction-to-board characterization parameter	55	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_{CC}	V_{CC} supply current			100		μA
V_{BACK}	Backup supply voltage	Operating	1.4		V_{CC}	V
		Switchover	2.0		V_{CC}	
I_{BACK}	Backup supply current	V_{CC} needs a pulse (1), V_{BACK} = 3 V, Oscillator on, T_A = 25°C		1.2	1.5	μA
LOGIC LEVEL INPUTS						
V_{IL}	Input low voltage				0.3 V_{CC}	V
V_{IH}	Input high voltage		0.7 V_{CC}			V
I_{IN}	Input current	$0 V \le V_{IN} \le V_{CC}$	-1		1	μA
LOGIC LEVEL OUTPUTS						
V_{OL}	Output low voltage	I_{OL} = 3 mA			0.4	V
I_L	Leakage current		-1		1	μA
REAL-TIME CLOCK CHARACTERISTICS						
	Pre-calibration accuracy	V_{CC} = 3.3 V, V_{BACK} = 3 V, Oscillator on, T_A = 25°C		±35 (2)		ppm

(1) The currents measured after issuing a pulse on V_{CC}. The pulse amplitude 0-V_{CC}; pulse width min 1 ms.
(2) Typical accuracy is measured using reference board design and KDS DMX-26S surface-mount 32.768-kHz crystal. Variation in board design and crystal section results in different typical accuracy.

6.6 I^2C Timing Requirements

		STANDARD MODE		FAST MODE		UNIT
		MIN	MAX	MIN	MAX	
f_{scl}	I^2C clock frequency	0	100	0	400	kHz
t_{sch}	I^2C clock high time	4		0.6		μs
t_{scl}	I^2C clock low time	4.7		1.3		μs
t_{sp}	I^2C spike time	0	50	0	50	ns
t_{sds}	I^2C serial data setup time	250		100		ns
t_{sdh}	I^2C serial data hold time	0		0		ns
t_{icr}	I^2C input rise time		1000	$20 + 0.1C_b$ (1)	300	ns
t_{icf}	I^2C input fall time		300	$20 + 0.1C_b$ (1)	300	ns
t_{ocf}	I^2C output fall time		300	$20 + 0.1C_b$ (1)	300	μs
t_{buf}	I^2C bus free time	4.7		1.3		μs
t_{sts}	I^2C Start setup time	4.7		0.6		μs
t_{sth}	I^2C Start hold time	4		0.6		μs
t_{sps}	I^2C Stop setup time	4		0.6		μs
$t_{vd(data)}$	Valid data time (SCL low to SDA valid)		1		1	μs
$t_{vd(ack)}$	Valid data time of ACK (ACK signal from SCL low to SDA low)		1		1	μs

(1) C_b = total capacitance of one bus line in pF

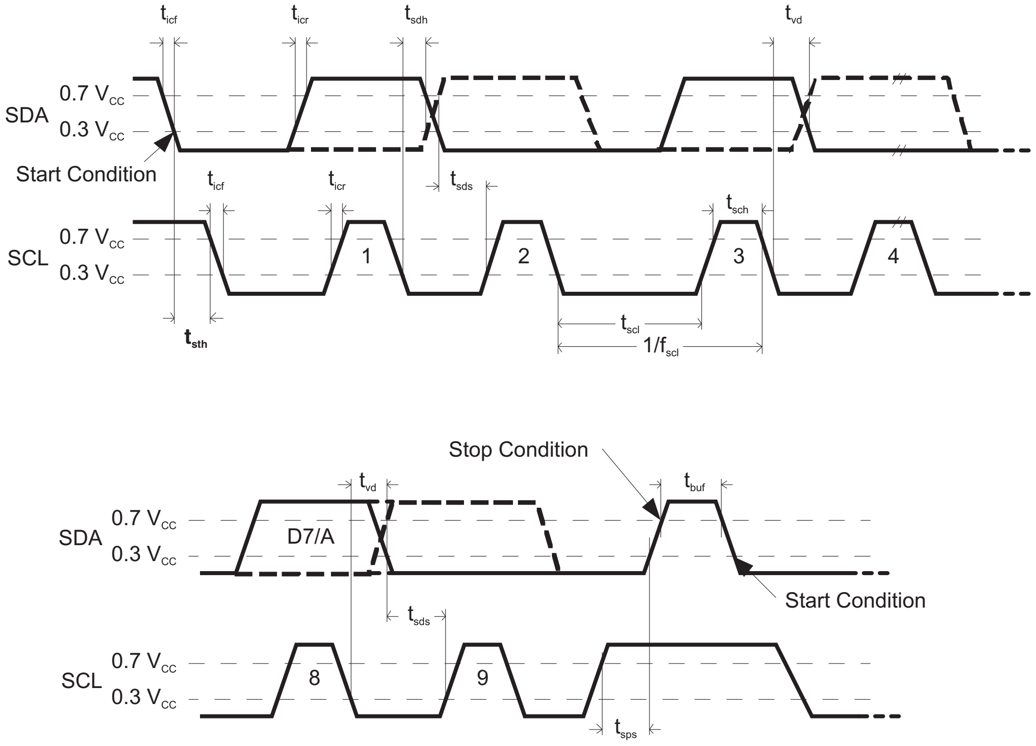


Figure 1. I^2C Timing Diagram

6.7 Typical Characteristics

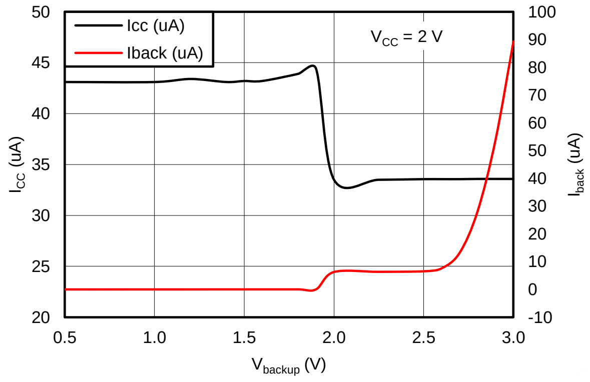


Figure 2. Current Consumption vs Backup Supply Voltage

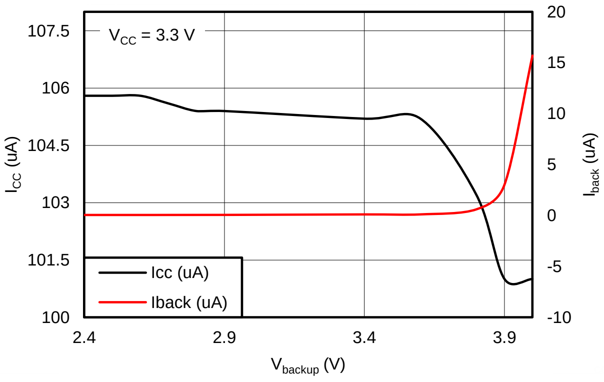


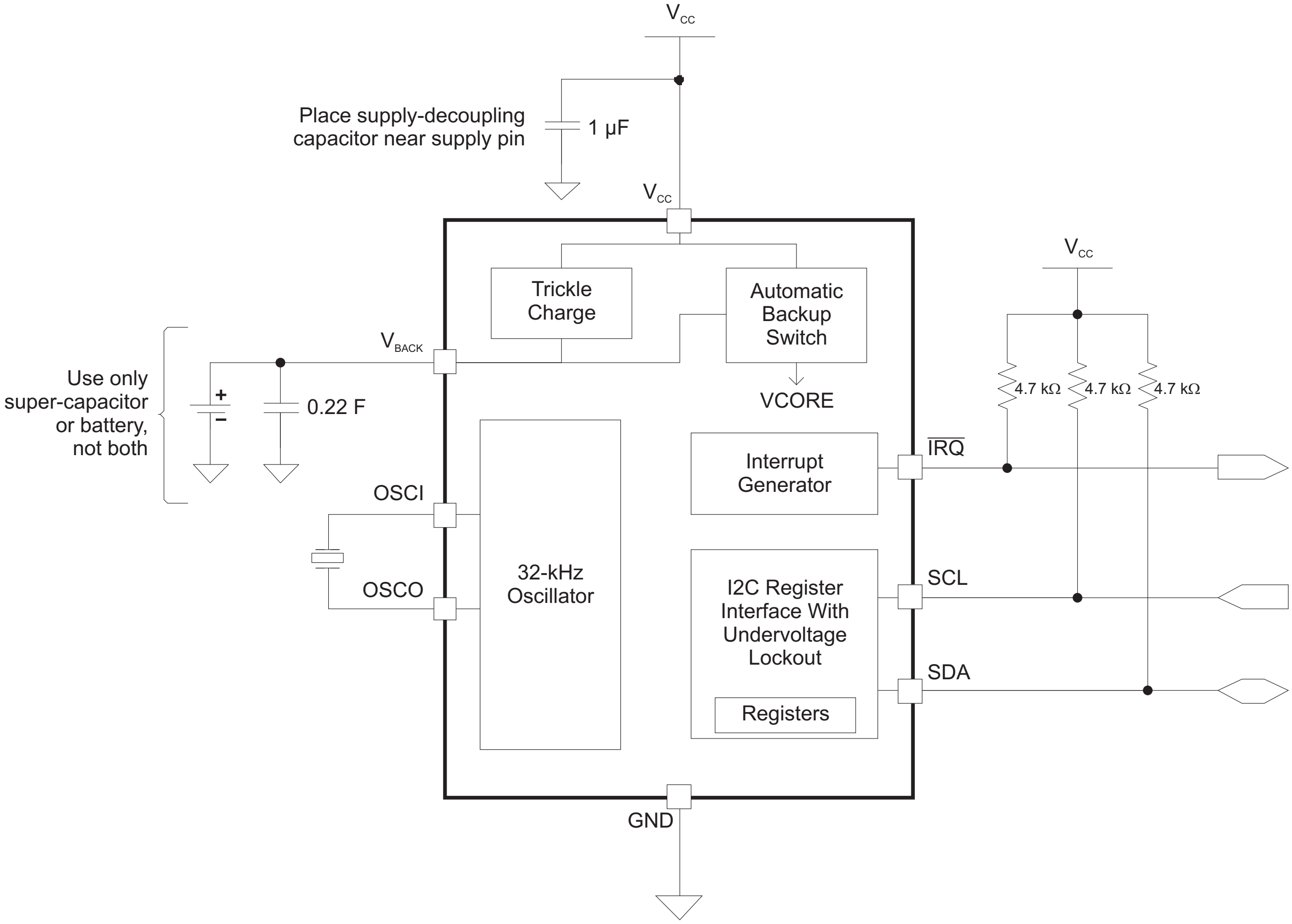
Figure 3. Current Consumption vs Backup Supply Voltage

7 Detailed Description

7.1 Overview

The bq32000 is a real-time clock that features an automatic backup supply with an integrated trickle charger.

7.2 Functional Block Diagram



NOTE: All pullup resistors should be connected to V_{CC} such that no pullup is applied during backup supply operation.

7.3 Feature Description

7.3.1 $\overline{\text{IRQ}}$ Function

The $\overline{\text{IRQ}}$ pin of the bq32000 functions as a general-purpose output or a frequency test output. The function of $\overline{\text{IRQ}}$ is configurable in the device register space by setting the FT, FTF, and OUT bits. On initial power cycles, the OUT bit is set to one, and the FTF and FT bits are set to zero. On subsequent power-ups, with backup supply present, the OUT bit remains unchanged, and the FTF and FT bits are set to zero. When operating on backup supply, the $\overline{\text{IRQ}}$ pin function is unused. $\overline{\text{IRQ}}$ pullup resistor should be tied to V_{CC} to prevent $\overline{\text{IRQ}}$ operation when operating on backup supply. The effect of the calibration logic is not normally observable when $\overline{\text{IRQ}}$ is configured to output 1 Hz. The calibration logic functions by periodically adjusting the width of the 1-Hz clock. The calibration effect is observable only every eight or sixteen minutes, depending on the sign of the calibration.

Feature Description (continued)

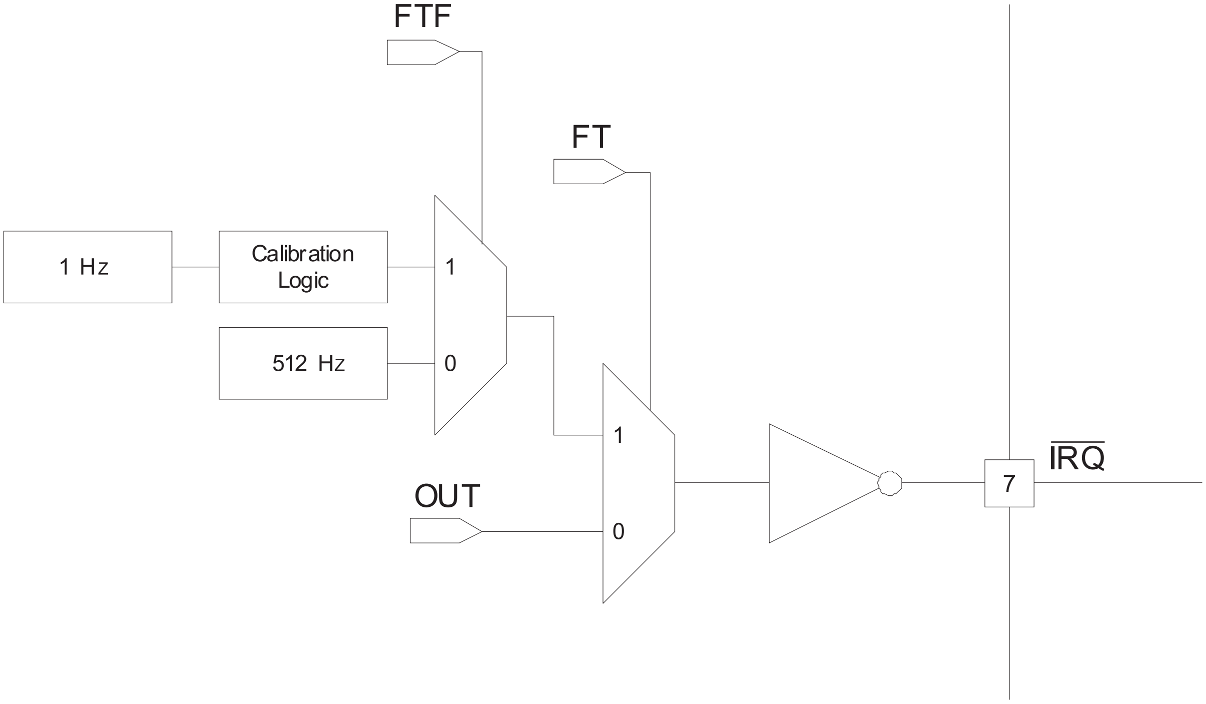


Figure 4. $\overline{\text{IRQ}}$ Pin Functional Diagram

Table 1. $\overline{\text{IRQ}}$ Function

FT	OUT	FTF	$\overline{\text{IRQ}}$ STATE
1	X	1	1 Hz
1	X	0	512 Hz
0	1	X	1
0	0	X	0

7.3.2 V_{BACK} Switchover

The bq32000 has an internal switchover circuit that causes the device to switch from main power supply to backup power supply when the voltage of the main supply pin V_{CC} drops below a minimum threshold. The V_{BACK} switchover circuit uses an internal reference voltage V_{REF} derived from the on-chip bandgap reference; V_{REF} is approximately 2.8 V. The device switches to the V_{BACK} supply when V_{CC} is less than the lesser of V_{BACK} or V_{REF}. Similarly, the device switches to the V_{CC} supply when V_{CC} is greater than either V_{BACK} or V_{REF}.

Some registers are reset to default values when the RTC switches from main power supply to backup power supply. Please see the register definitions to determine what register bits are effected by a backup switchover (effected bits have their reset value (1/0) shown for 'Cycle', bits that are unchanged by backup are marked 'UC').

The time keeping registers can take up to 1 second to update after the RTC switches from backup power supply to main power supply.

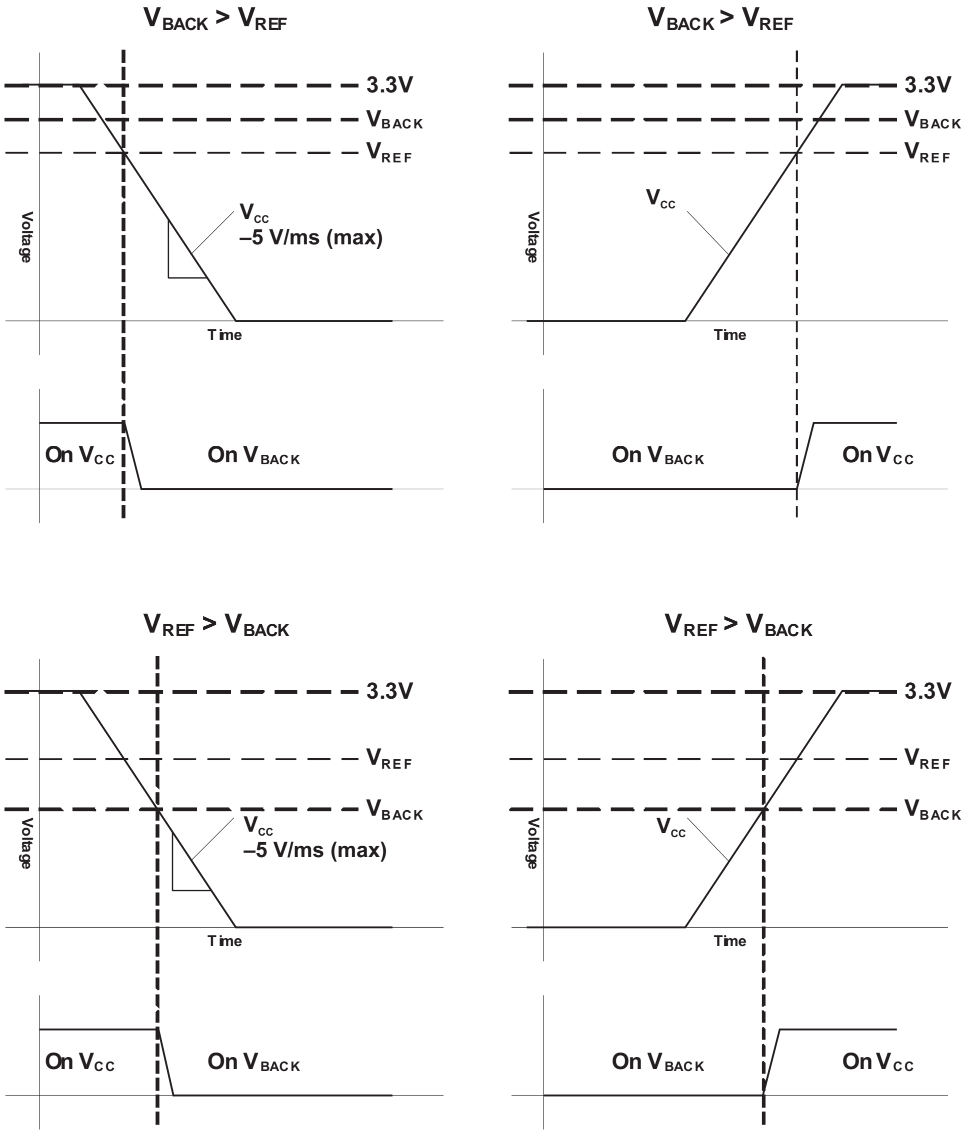


Figure 5. Switchover Diagram

7.3.3 Trickle Charge

The bq32000 includes a trickle charge circuit to maintain the charge of the backup supply when a super capacitor is used. The trickle charge circuit is implemented as a series of three switches that are independently controlled by setting the TCHE[3:0], TCH2, and TCFE bits in the register space.

TCHE[3:0] must be written as 0x5h and TCH2 as 1 to close the trickle charge switches and enable charging of the backup supply from V_{CC}. Additionally, TCFE can be set to 1 to bypass the internal diode and boost the charge voltage of the backup supply. All trickle charge switches are opened when the device is initially powered on and each time the device switches from the main supply to the backup supply. The trickle charge circuit is intended for use with super capacitors; however, it can be used with a rechargeable battery under certain conditions. Care must be taken not to overcharge a rechargeable battery when enabling trickle charge. Follow all charging guidelines specific to the rechargeable battery or super capacitor when enabling trickle charge.

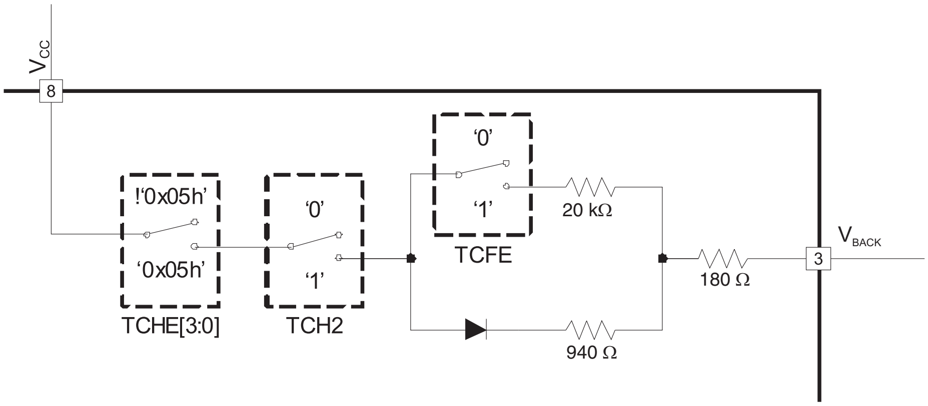


Figure 6. Trickle Charge Switch Functional Diagram

7.4 Device Functional Modes

When the device switches from the main power supply to backup supply, the Time keeping register Registers [0-9] cannot be accessed via the I2C. The access to these registers are only when $V_{CC} > V_{ref}$.

The Time keeping registers can take up to 1 second to update after the device switches from backup power supply to main power supply.

7.5 Programming

7.5.1 I^{2}C Serial Interface

The I^{2}C interface allows control and monitoring of the RTC by a microcontroller. I^{2}C is a two-wire serial interface developed by Philips Semiconductor (see I^{2}C-Bus Specification, Version 2.1, January 2000).

The bus consists of a data line (SDA) and a clock line (SCL) with off-chip pullup resistors. When the bus is idle, both SDA and SCL lines are pulled high.

A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer.

A slave device receives and/or transmits data on the bus under control of the master device. This device operates only as a slave device.

I^{2}C communication is initiated by a master sending a start condition, a high-to-low transition on the SDA I/O while SCL is held high. After the start condition, the device address byte is sent, most-significant bit (MSB) first, including the data direction bit ($R/\overline{W}$). After receiving a valid address byte, this device responds with an acknowledge, a low on the SDA I/O during the high of the acknowledge-related clock pulse. This device responds to the I^{2}C slave address 11010000b for write commands and slave address 11010001b for read commands.

This device does not respond to the general call address.

Programming (continued)

A data byte follows the address acknowledge. If the $R/\overline{W}$ bit is low, the data is written from the master. If the $R/\overline{W}$ bit is high, the data from this device are the values read from the register previously selected by a write to the subaddress register. The data byte is followed by an acknowledge sent from this device. Data is output only if complete bytes are received and acknowledged.

A stop condition, which is a low-to-high transition on the SDA I/O while the SCL input is high, is sent by the master to terminate the transfer. A master device must wait at least 60 μs after the RTC exits backup mode to generate a START condition.

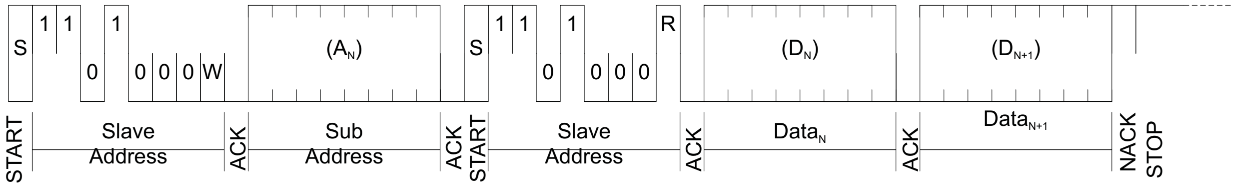


Figure 7. I^{2}C Read Mode

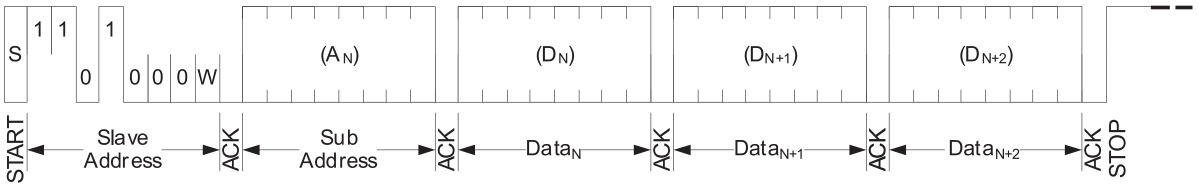


Figure 8. I^{2}C Write Mode

7.6 Register Maps

Table 2. Normal Registers

REGISTER	ADDRESS (HEX)	REGISTER NAME	DESCRIPTION
0	0x00	SECONDS	Clock seconds and STOP bit
1	0x01	MINUTES	Clock minutes
2	0x02	CENT_HOURS	Clock hours, century, and CENT_EN bit
3	0x03	DAY	Clock day
4	0x04	DATE	Clock date
5	0x05	MONTH	Clock month
6	0x06	YEARS	Clock years
7	0x07	CAL_CFG1	Calibration and configuration
8	0x08	TCH2	Trickle charge enable
9	0x09	CFG2	Configuration 2

Table 3. Special Function Registers

REGISTER	ADDRESS (HEX)	REGISTER NAME	DESCRIPTION
32	0x20	SF KEY 1	Special function key 1
33	0x21	SF KEY 2	Special function key 2
34	0x22	SFR	Special function register

7.6.1 I^{2}C Read After Backup Mode

The time keeping registers can take up to 1 second to update after the RTC switches from backup power supply to main power supply. An I^{2}C read of the RTC that starts before the update has completed will return the time when the RTC enters backup mode. To ensure that the correct time is read after backup mode, the host should wait longer than 1 second after the main supply is greater than 2.8 V and V_{BACK}.

7.6.2 Normal Register Descriptions

7.6.2.1 SECONDS Register (address = 0x00) [reset = 0XXXXXXXb]

Description – Clock seconds and STOP bit

Figure 9. SECONDS Register

7	6	5	4	3	2	1	0	BIT(S)
STOP	10_SECOND			1_SECOND				Name
r/w	r/w			r/w				Read/Write
0	X	X	X	X	X	X	X	Initial
UC	UC	UC	UC	UC	UC	UC	UC	Cycle

STOP	Oscillator stop. The STOP bit is used to force the oscillator to stop oscillating. STOP is set to 0 on initial application of power, on all subsequent power cycles STOP remains unchanged. On initial power application STOP can be written to 1 and then written to 0 to force start the oscillator. 0 Normal 1 Stop
10_SECOND	BCD of tens of seconds. The 10_SECOND bits are the BCD representation of the number of tens of seconds on the clock. Valid values are 0 to 5. If invalid data is written to 10_SECOND, the clock will update with invalid data in 10_SECOND until the counter rolls over; thereafter, the data in 10_SECOND is valid. Time keeping registers can take up to 1 second to update after the RTC switches from backup power supply to main power supply.
1_SECOND	BCD of seconds. The 1_SECOND bits are the BCD representation of the number of seconds on the clock. Valid values are 0 to 9. If invalid data is written to 1_SECOND, the clock will update with invalid data in 1_SECOND until the counter rolls over; thereafter, the data in 1_SECOND is valid. Time keeping registers can take up to 1 second to update after the RTC switches from backup power supply to main power supply.

7.6.2.2 MINUTES Register (address = 0x01) [reset = 1XXXXXXb]

Description – Clock minutes

Figure 10. MINUTES Register

7	6	5	4	3	2	1	0	BIT(S)
OF	10_MINUTE			1_MINUTE				Name
r/w	r/w			r/w				Read/Write
1	X	X	X	X	X	X	X	Initial
0	UC	UC	UC	UC	UC	UC	UC	Cycle

OF	Oscillator fail flag. The OF bit is a latched flag indicating when the 32.768-kHz oscillator has dropped at least four consecutive pulses. The OF flag is always set on initial power-up, and it can be cleared through the serial interface. When OF is 0, no oscillator failure has been detected. When OF is 1, the oscillator fail detect circuit has detected at least four consecutive dropped pulses. 0 No failure detected 1 Failure detected
10_MINUTE	BCD of tens of minutes. The 10_MINUTE bits are the BCD representation of the number of tens of minutes on the clock. Valid values are 0 to 5. If invalid data is written to 10_MINUTE, the clock will update with invalid data in 10_MINUTE until the counter rolls over; thereafter, the data in 10_MINUTE is valid. Time keeping registers can take up to 1 second to update after the RTC switches from backup power supply to main power supply.
1_MINUTE	BCD of minutes. The 1_MINUTE bits are the BCD representation of the number of minutes on the clock. Valid values are 0 to 9. If invalid data is written to 1_MINUTE, the clock will update with invalid data in 1_MINUTE until the counter rolls over; thereafter, the data in 1_MINUTE is valid. Time keeping registers can take up to 1 second to update after the RTC switches from backup power supply to main power supply.

7.6.2.3 CENT_HOURS Register (address = 0x02) [reset = XXXXXXXXb]

Description – Clock hours, century, and CENT_EN bit

Figure 11. CENT_HOURS Register

7	6	5	4	3	2	1	0	BIT(S)
CENT_EN	CENT	10_HOUR		1_HOUR				Name
r/w	r/w	r/w		r/w				Read/Write
X	X	X	X	X	X	X	X	Initial
UC	UC	UC	UC	UC	UC	UC	UC	Cycle

CENT_EN	Century enable. The CENT_EN bit enables the century timekeeping feature. If CENT_EN is set to 1, then the clock tracks the century using the CENT bit. If CENT_EN is set to 0, the clock ignores the CENT bit. 0 Century disabled 1 Century enabled
CENT	Century. The CENT bit tracks the century when century timekeeping is enabled. The clock toggles the CENT bit when the year count rolls from 99 to 00. Because the clock compliments the CENT bit, the user can define the meaning of CENT (1 for current century and 0 for next century, or 0 for current century and 1 for next century).
10_HOUR	BCD of tens of hours (24-hour format). The 10_HOUR bits are the BCD representation of the number of tens of hours on the clock, in 24-hour format. Valid values are 0 to 2. If invalid data is written to 10_HOUR, the clock will update with invalid data in 10_HOUR until the counter rolls over; thereafter, the data in 10_HOUR is valid. Time keeping registers can take up to 1 second to update after the RTC switches from backup power supply to main power supply.
1_HOUR	BCD of hours (24-hour format). The 1_HOUR bits are the BCD representation of the number of hours on the clock, in 24-hour format. Valid values are 0 to 9. If invalid data is written to 1_HOUR, the clock will update with invalid data in 1_HOUR until the counter rolls over; thereafter, the data in 1_HOUR is valid. Time keeping registers can take up to 1 second to update after the RTC switches from backup power supply to main power supply.

7.6.2.4 DAY Register (address = 0x03) [reset = 00000XXXb]

Description – Clock day

Figure 12. DAY Register

7	6	5	4	3	2	1	0	BIT(S)
RSVD					DAY			Name
r/w					r/w			Read/Write
0	0	0	0	0	X	X	X	Initial
0	0	0	0	0	UC	UC	UC	Cycle

RSVD	Reserved. The RSVD bits should always be written as 0.
DAY	BCD of the day of the week. The DAY bits are the BCD representation of the day of the week. Valid values are 1 to 7 and represent the days from Sunday to Saturday. DAY updates if set to 0 until the counter rolls over; thereafter, the data in DAY is valid. Time keeping registers can take up to 1 second to update after the RTC switches from backup power supply to main power supply.

1	Sunday
2	Monday
3	Tuesday
4	Wednesday
5	Thursday
6	Friday
7	Saturday

7.6.2.5 DATE Register (address = 0x04) [reset = 00XXXXXXb]

Description – Clock date

Figure 13. DATE Register

7	6	5	4	3	2	1	0	BIT(S)
RSVD		10_DATE		1_DATE				Name
r/w		r/w		r/w				Read/Write
0	0	X	X	X	X	X	X	Initial
0	0	UC	UC	UC	UC	UC	UC	Cycle

RSVD	Reserved. The RSVD bits should always be written as 0.
10_DATE	BCD of tens of date. The 10_DATE bits are the BCD representation of the tens of date on the clock. Valid values are 0 to 3(1). If invalid data is written to 10_DATE, the clock will update with invalid data in 10_DATE until the counter rolls over; thereafter, the data in 10_DATE is valid. Time keeping registers can take up to 1 second to update after the RTC switches from backup power supply to main power supply.
1_DATE	BCD of date. The 1_DATE bits are the BCD representation of the date on the clock. Valid values are 0 to 9(1). If invalid data is written to 1_DATE, the clock will update with invalid data in 1_DATE until the counter rolls over; thereafter, the data in 1_DATE is valid. Time keeping registers can take up to 1 second to update after the RTC switches from backup power supply to main power supply.

---

(1) 10_DATE and 1_DATE must form a valid date, 01 to 31, dependent on month and year.

7.6.2.6 MONTH Register (address = 0x05) [reset = 000XXXXXb]

Description – Clock month

Figure 14. MONTH Register

7	6	5	4	3	2	1	0	BIT(S)
RSVD			10_MONTH	1_MONTH				Name
r/w			r/w	r/w				Read/Write
0	0	0	X	X	X	X	X	Initial
0	0	0	UC	UC	UC	UC	UC	Cycle

RSVD	Reserved. The RSVD bits should always be written as 0.
10_MONTH	BCD of tens of month. The 10_MONTH bits are the BCD representation of the tens of month on the clock. Valid values are 0 to 1 (1). If invalid data is written to 10_MONTH, the clock will update with invalid data in 10_MONTH until the counter rolls over; thereafter, the data in 10_MONTH is valid.
1_MONTH	BCD of month. The 1_MONTH bits are the BCD representation of the month on the clock. Valid values are 0 to 9 (1). If invalid data is written to 1_MONTH, the clock will update with invalid data in 1_MONTH until the counter rolls over; thereafter, the data in 1_MONTH is valid.

(1) 10_MONTH and 1_MONTH must form a valid date, 01 to 12.

7.6.2.7 YEARS Register (address = 0x06) [reset = XXXXXXXXb]

Description – Clock year

Figure 15. YEARS Register

7	6	5	4	3	2	1	0	BIT(S)
10_YEAR				1_YEAR				Name
r/w				r/w				Read/Write
X	X	X	X	X	X	X	X	Initial
UC	UC	UC	UC	UC	UC	UC	UC	Cycle

10_YEAR	BCD of tens of years. The 10_YEAR bits are the BCD representation of the tens of years on the clock. Valid values are 0 to 9. If invalid data is written to 10_YEAR, the clock will update with invalid data in 10_YEAR until the counter rolls over; thereafter, the data in 10_YEAR is valid. Time keeping registers can take up to 1 second to update after the RTC switches from backup power supply to main power supply.
1_YEAR	BCD of year. The 1_YEAR bits are the BCD representation of the years on the clock. Valid values are 0 to 9. If invalid data is written to 1_YEAR, the clock will update with invalid data in 1_YEAR until the counter rolls over; thereafter, the data in 1_YEAR is valid. Time keeping registers can take up to 1 second to update after the RTC switches from backup power supply to main power supply.

7.6.2.8 CAL_CFG1 Register (address = 0x07) [reset = 10000000b]

Description – Calibration and control

Figure 16. CAL_CFG1 Register

7	6	5	4	3	2	1	0	BIT(S)
OUT	FT	S	CAL					Name
r/w	r/w	r/w	r/w					Read/Write
1	0	0	0	0	0	0	0	Initial
UC	UC	UC	UC	UC	UC	UC	UC	Cycle

OUT	Logic output, when FT = 0. When FT is zero, the logic output of $\overline{\text{IRQ}}$ pin reflects the value of OUT. 0 $\overline{\text{IRQ}}$ is logic 0 1 $\overline{\text{IRQ}}$ is logic 1
FT	Frequency test. The FT bit is used to enable the frequency test signal on the $\overline{\text{IRQ}}$ pin. When FT is 1, a square wave is produced on the $\overline{\text{IRQ}}$ pin. The FTF bit in the SFR register determines the frequency of the test signal. 0 Disable 1 Enable
S	Calibration sign. The S bit determines the polarity of the calibration applied to the oscillator. If S is 0, then the calibration slows the RTC. If S is 1, then the calibration speeds the RTC. 0 Slowing (+) 1 Speeding (–)
CAL	Calibration. The CAL bits along with S determine the calibration amount as shown in Table 4.

Table 4. Calibration

CAL (DEC)	S = 0	S = 1
0	+0 ppm	–0 ppm
1	+2 ppm	–4 ppm
N	+N / 491520 (per minute)	–N / 245760 (per minute)
30	+61 ppm	–122 ppm
31	+63 ppm	–126 ppm

7.6.2.9 TCH2 Register (address = 0x08) [reset = 10010000b]

Description – Trickle charge TCH2 control

Figure 17. TCH2 Register

7	6	5	4	3	2	1	0	BIT(S)
RSVD		TCH2	RSVD					Name
r/w		r/w	r/w					Read/Write
1	0	0	1	0	0	0	0	Initial
UC	0	0	1	UC	UC	UC	UC	Cycle

RSVD	Reserved. The RSVD bits should always be written as 0.
TCH2	Trickle charge switch two. The TCH2 bit determines if the internal trickle charge switch is closed or open. All the trickle charge switches must be closed in order for trickle charging to occur. If TCH2 is 0, then the TCH2 switch is open. If TCH2 is 1, then the TCH2 switch is closed. 0 Open 1 Closed

7.6.2.10 CFG2 Register (address = 0x09) [reset = 10101010b]

Description – Configuration 2

Figure 18. CFG2 Register

7	6	5	4	3	2	1	0	BIT(S)
RSVD	TCFE	RSVD		TCHE				Name
r/w	r/w	r/w		r/w				Read/Write
1	0	1	0	1	0	1	0	Initial
1	0	UC	UC	1	0	1	0	Cycle

RSVD	Reserved. The RSVD bits should always be written as 0.
TCFE	Trickle charge FET bypass. The TCFE bit is used to enable the trickle charge FET. When TCFE is 0, the FET is off. When TCFE is 1, the FET is on. 0 Open 1 Closed
TCHE	Trickle charge enable. The TCHE bits determine if the trickle charger is active. If TCHE is 0x5, then the trickle charger is active, otherwise, the trickle charger is inactive.

7.6.3 Special Function Registers

7.6.3.1 SF KEY 1 Register (address = 0x20) [reset = 00000000b]

Description – Special function key 1

Figure 19. SF KEY 1 Register

7	6	5	4	3	2	1	0	BIT(S)
SF KEY B1								Name
r/w								Read/Write
0	0	0	0	0	0	0	0	Initial
0	0	0	0	0	0	0	0	Cycle

SF KEY B1	Special function access key byte 1. Reads as 0x00, and key is 0x5E. The SF KEY 1 and SF KEY 2 registers are used to enable access to the main special function register (SFR). Access to SFR is granted only after the special function keys are written sequentially to SF KEY 1 and SF KEY 2. Each write to the SFR must be preceded by writing the SF keys to the SF key registers, in order, SF KEY 1 then SF KEY 2.

7.6.3.2 SF KEY 2 Register (address = 0x21) [reset = 00000000b]

Description – Special function key 2

Figure 20. SF KEY 2 Register

7	6	5	4	3	2	1	0	BIT(S)
SF KEY 2								Name
r/w								Read/Write
0	0	0	0	0	0	0	0	Initial
0	0	0	0	0	0	0	0	Cycle

SF KEY 2	Special function access key byte 2. Reads as 0x00, and key is 0xC7. The SF KEY 1 and SF KEY 2 registers are used to enable access to the main special function register (SFR). Access to SFR is granted only after the special function keys are written sequentially to SF KEY 1 and SF KEY 2. Each write to the SFR must be preceded by writing the SF keys to the SF key registers, in order, SF KEY 1 then SF KEY 2.

7.6.3.3 SFR Register (address = 0x22) [reset = 00000000b]

Description – Special function register 1

Figure 21. SFR Register

7	6	5	4	3	2	1	0	BIT(S)
RSVD							FTF	Name
r/w							r/w	Read/Write
0	0	0	0	0	0	0	0	Initial
0	0	0	0	0	0	0	0	Cycle

RSVD	Reserved. The RSVD bits should always be written as 0.
FTF	Force calibration to 1 Hz. FTF allows the frequency of the calibration output to be changed from 512 Hz to 1 Hz. By default, FTF is cleared, and the RTC outputs a 512-Hz calibration signal. Setting FTF forces the calibration signal to 1 Hz, and the calibration tracks the internal ppm adjustment. Note: The default 512-Hz calibration signal does not include the effect of the ppm adjustment.

0	Normal 512-Hz calibration
1	1-Hz calibration

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The typical application for the bq32000 is to provide precise time and date to a system. The backup power supply provides additional reliability by automatically switching over from the main supply when it drops under the voltage threshold.

8.2 Typical Application

The following design is a common application of the bq32000.

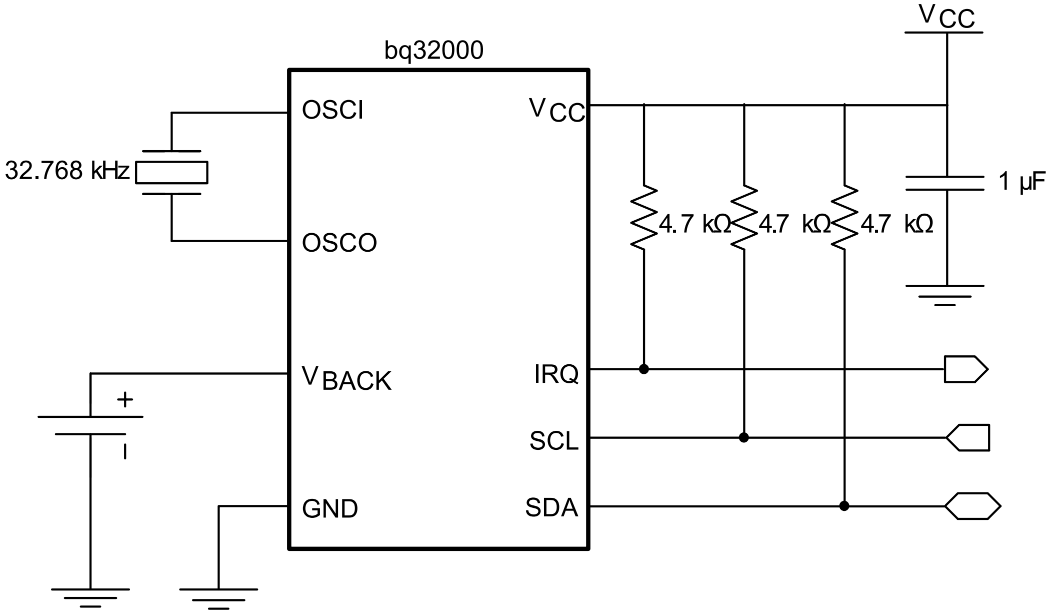


Figure 22. Typical Application Schematic

8.2.1 Design Requirements

The design requirement parameters are listed in the following table.

Table 5. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply Voltage	V_{CC}	3.3 V
Backup Supply	V_{BACK}	BR1225
Crystal Oscillator	XT	32.768 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Reading From a Register

The report details the read-back of the SECONDS register. Figure 23 depicts the first condition that will be used as a benchmark to compare the values taken from the SECONDS register in the bq32000, to the oscilloscope's internal PC time. In this example two modes of operation are demonstrated.

Condition 1. The main power supply, V_{CC}, is greater than the backup power supply, V_{BACK}, and the internal reference voltage, V_{REF}. In this mode, the device's internal registers are fully operational with READ and WRITE access. Analyzing Figure 23, the known register values are compared to the system clock; in this case, the PC clock which is shown at the bottom of the screen capture.

> The bq32000 during this condition is reading back [101][0010]= [5][2], which corresponds to 52 seconds at PC time of 2:22:43 PM.

Condition 2. V_{CC} is now lowered to 2 V (V_{BACK} > V_{CC}). In this mode, the I2C communications are halted. However, the internal time keeping registers maintain full functional operation and accuracy which will be available to be reliably read by the controller 1 second after the RTC switches from V_{BACK} to V_{CC} supply.

Condition 3. During this final test condition, the RTC is restored to operate from the main power supply and I2C communications are now fully functional.

> Figure 24 demonstrates a read-back value from the SECONDS register of [100][0101]= [4][5], or 45 seconds at PC time of 2:23:36 PM. This proves that the bq32000 managed to accurately maintain the time keeping registers functional while the V_{CC} dropped below V_{BACK}.

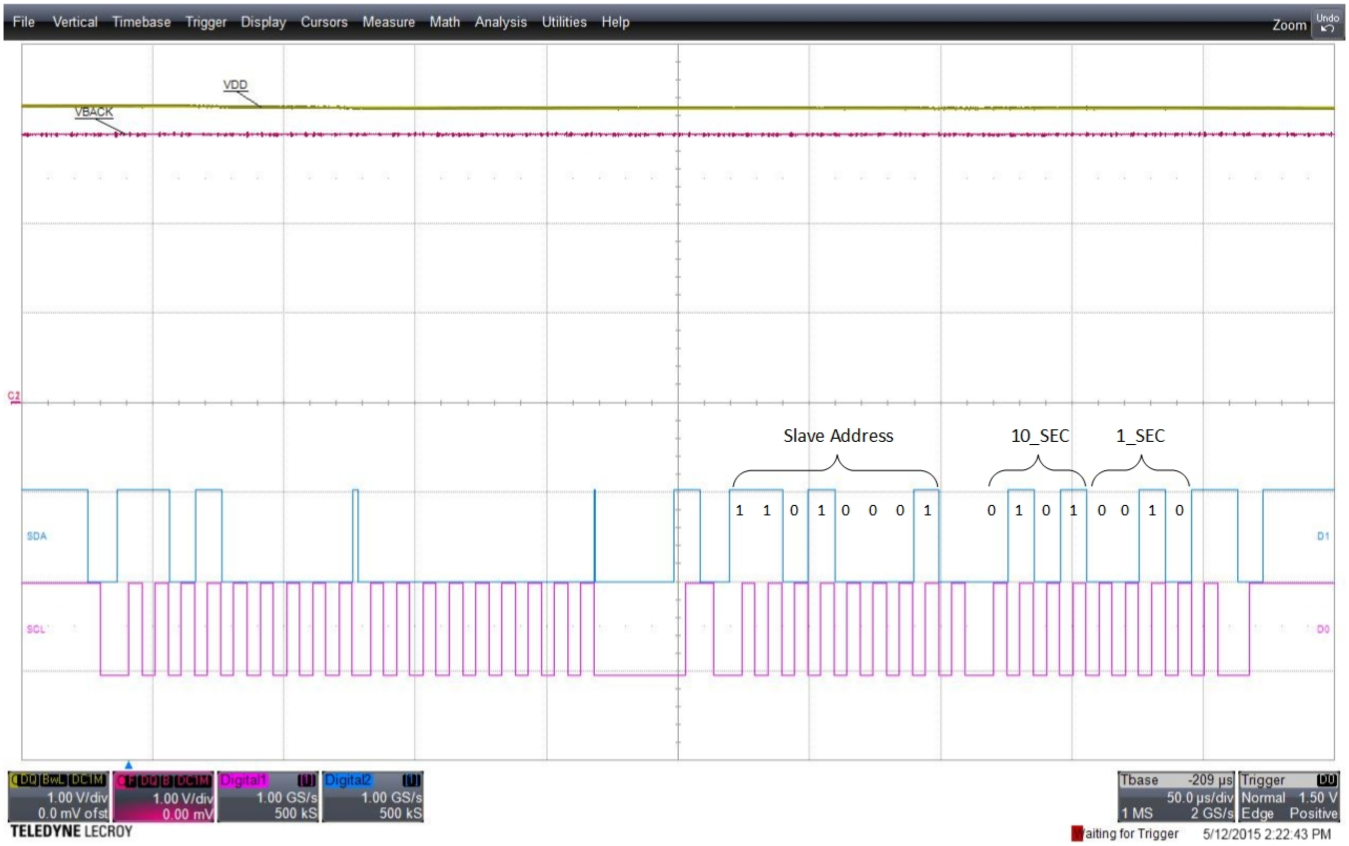
8.2.2.2 Leap Year Compensation

The BQ32000 classifies a leap year as any year that is evenly divisible by 4. Using this rule allows for reliable leap year compensation until 2100. Years that fall outside this rule will need to be compensated for by the external controller.

8.2.2.3 Utilizing the Backup Supply

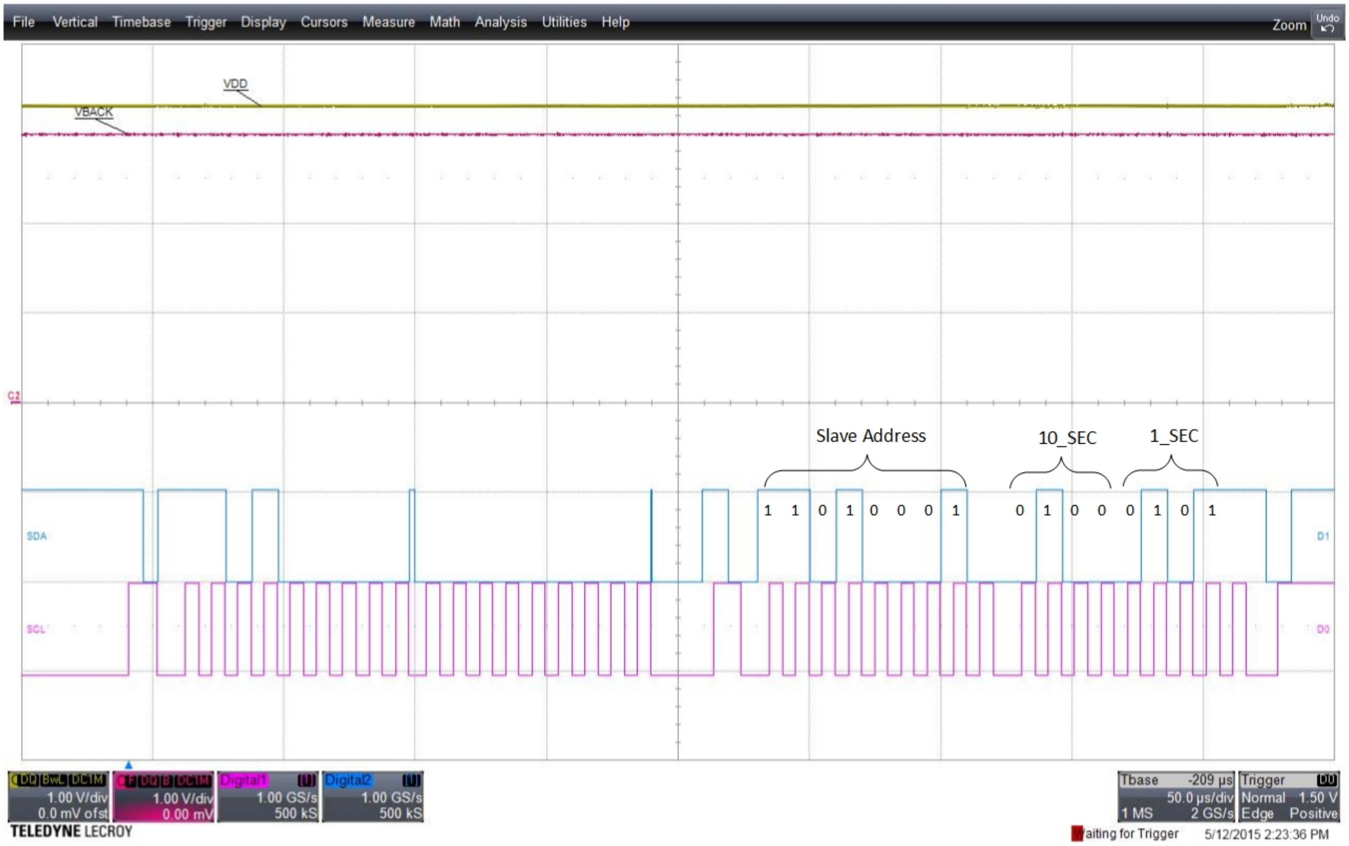
In order for the bq32000 to achieve a low backup supply current as specified in the *Electrical Characteristics*, the V_{CC} pin must be initialized after every total power loss situation. Initialization Is achieved by powering on V_{CC} with a voltage between 3 to 3.6 V for at least 1 ms immediately after the backup supply is connected. If the V_{CC} is not powered on while connecting the backup supply, then the expected leakage current from V_{BACK} will be much greater than specified.

8.2.3 Application Curves



C1 DQ BwL DC1M 1.00 V/div 0.0 mV ofst
C F DQ B DC1M 1.00 V/div 0.00 mV
Digital1 1.00 GS/s 500 kS
Digital2 1.00 GS/s 500 kS
Tbase -209 µs 50.0 µs/div 1 MS 2 GS/s
Trigger D0 Normal 1.50 V Edge Positive
Waiting for Trigger 5/12/2015 2:22:43 PM

Figure 23. Master and Slave I^{2}C Communication for the SECONDS Register



C1 DQ BwL DC1M 1.00 V/div 0.0 mV ofst
C F DQ B DC1M 1.00 V/div 0.00 mV
Digital1 1.00 GS/s 500 kS
Digital2 1.00 GS/s 500 kS
Tbase -209 µs 50.0 µs/div 1 MS 2 GS/s
Trigger D0 Normal 1.50 V Edge Positive
Waiting for Trigger 5/12/2015 2:23:36 PM

Figure 24. Master and Slave I^2C Communication for the SECONDS Register After Recovering From the Backup Supply

9 Power Supply Recommendations

The bq32000 is designed to operate from an input voltage supply, V_{CC}, range between 3.0 and 3.6 V. The user must place a minimum of 1-µF ceramic bypass capacitor rated for at least the maximum voltage as close as possible to V_{CC} and GND pin.

10 Layout

10.1 Layout Guidelines

The V_{CC} pin should be bypassed to GND using a low-ESR ceramic bypass capacitor with a minimum recommended value of 1-µF. This capacitor should be placed as close to the V_{CC} and GND pins as possible with thick trace or ground plane connection to the device GND pin.

Locate the 32.768-kHz crystal oscillator as close as possible to the OSCI and OSCO pins. This will minimize stray capacitance.

10.2 Layout Example

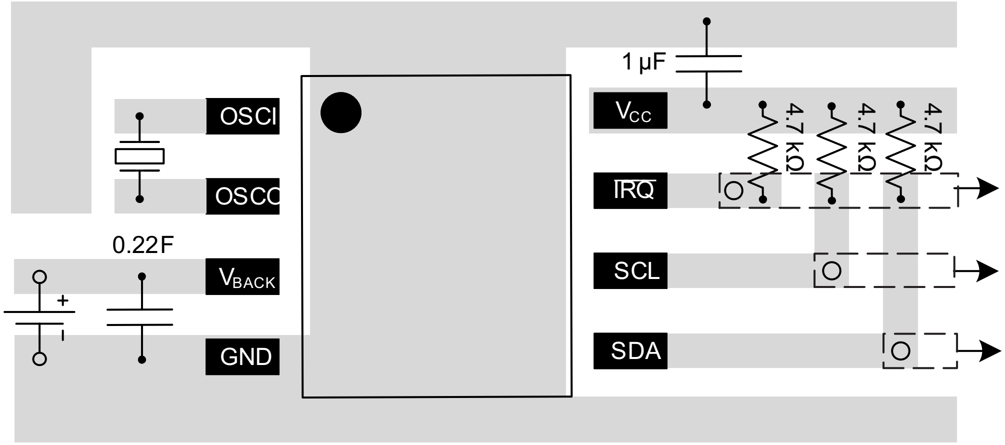


Figure 25. Recommended PCB Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Community Resources

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

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11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
BQ32000D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	32000	Samples
BQ32000DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	32000	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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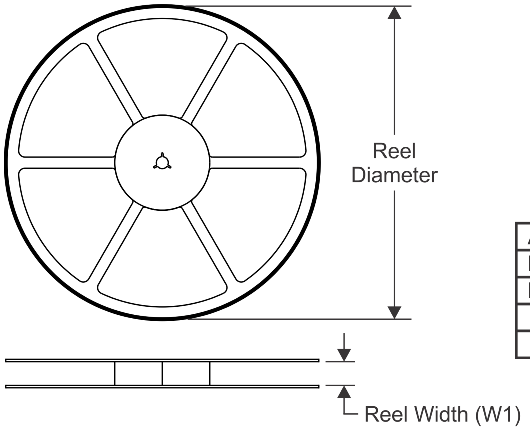
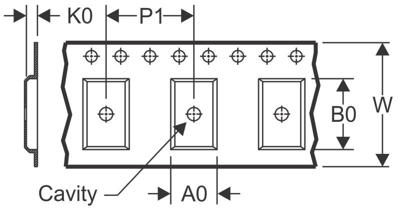
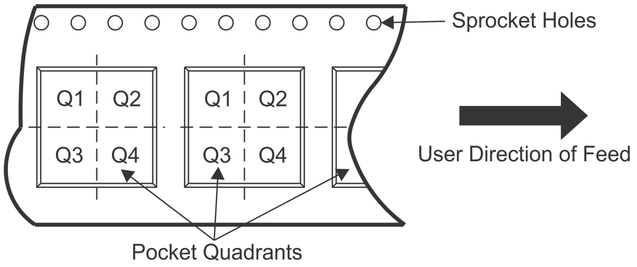


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

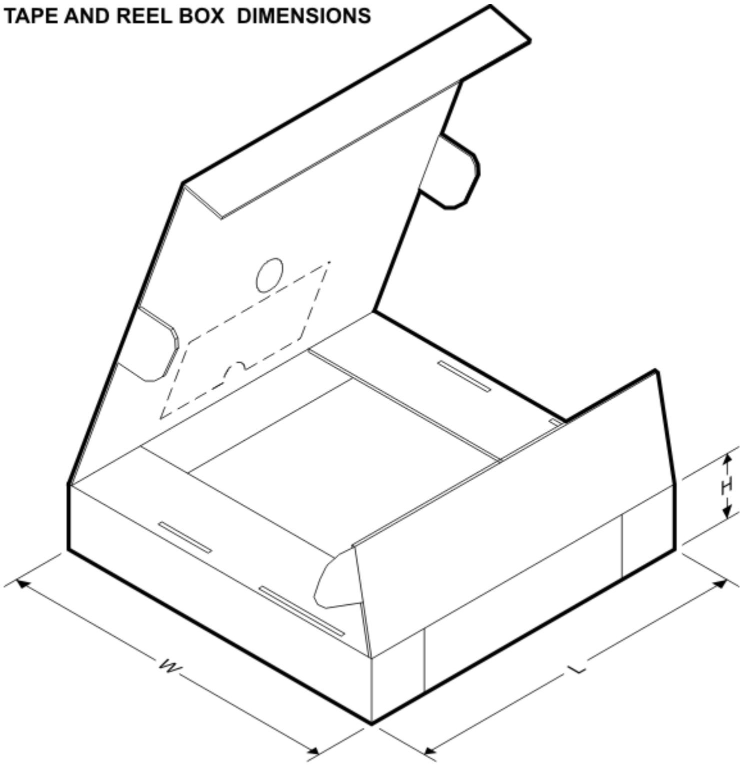
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ32000DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

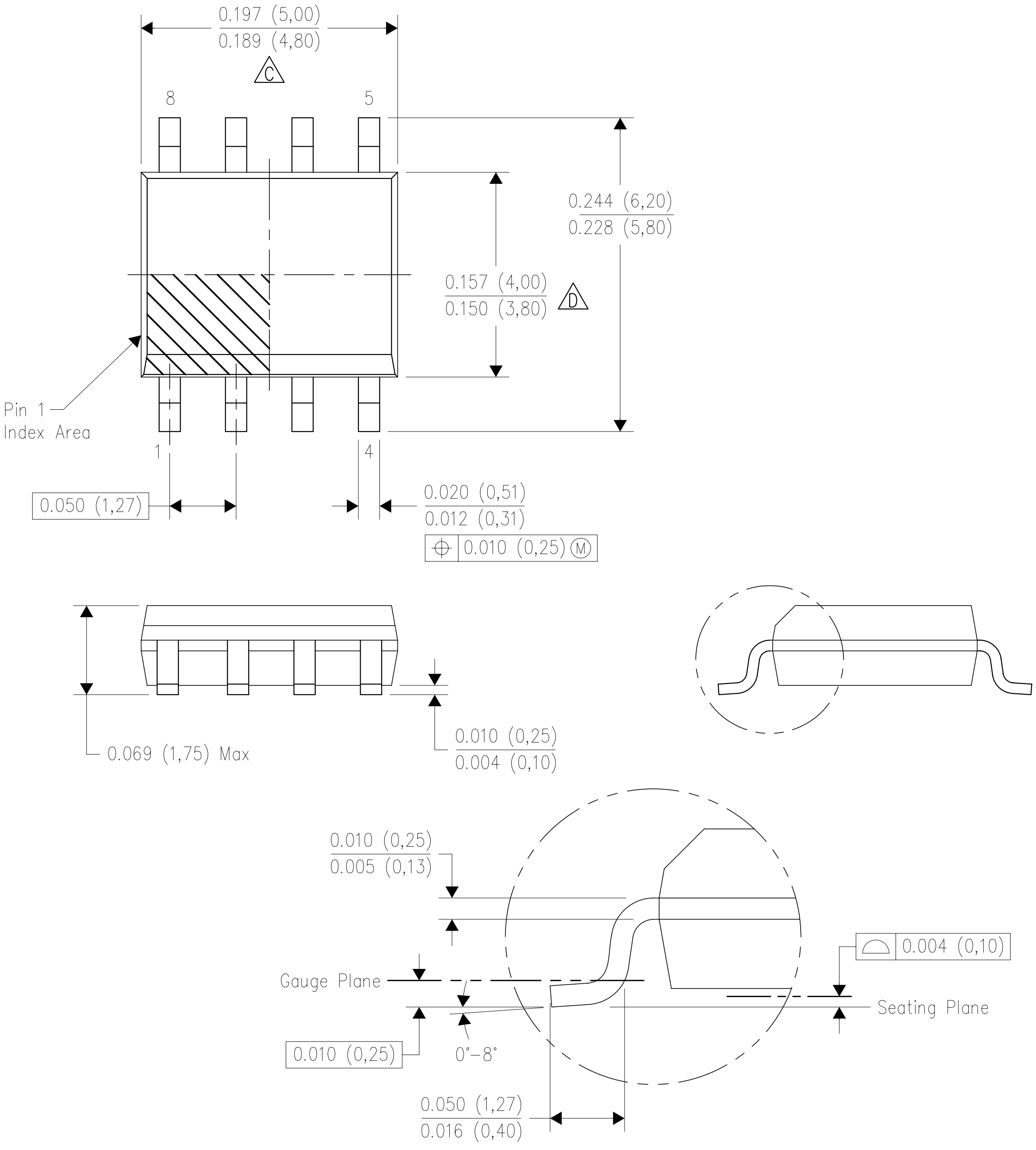
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ32000DR	SOIC	D	8	2500	367.0	367.0	35.0

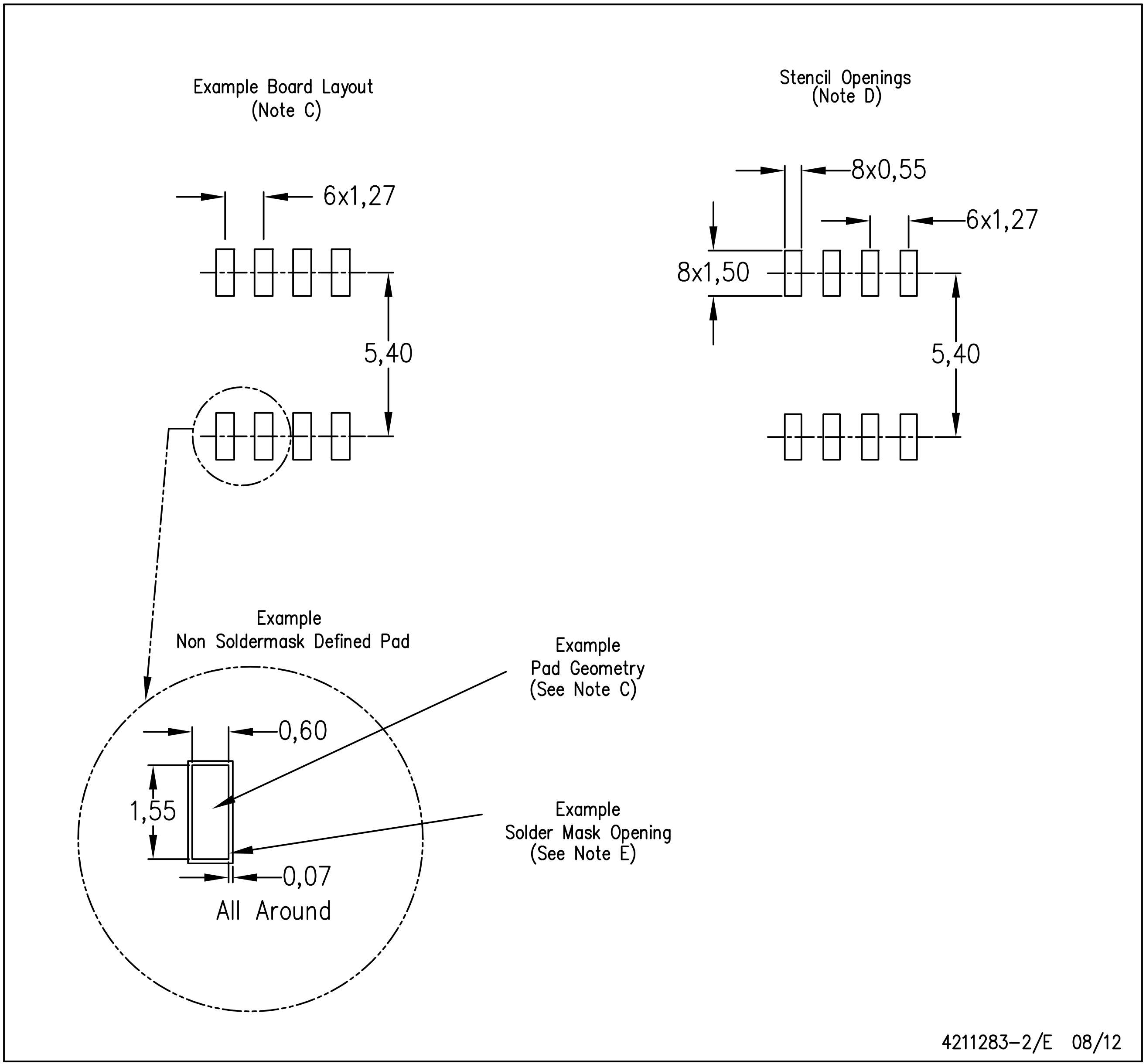
D (R–PDSO–G8) PLASTIC SMALL OUTLINE



4040047–3/M 06/11

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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